Preliminary Datasheet

OVERVIEW

The EV10AS940 is a 10-bit Ka-band capable single channel Analog-to-Digital Converter (ADC) allowing a sampling rate up to 12.8GSps. It features Digital Down Conversion (DDC) and Frequency Hopping (FH) capabilities with multiple digital channels thanks to the integration of multiple NCOs. The EV10AS940 is packaged with an organic substrate to allow high speed and high bandwidth operations.

FEATURES

- 33GHz (-3dB) analog bandwidth
- Up to 12.8GSps
- 10-bit resolution
- 2.5W power consumption
- 500mVpp full scale input dynamic range
- Single-Ended RF and clock inputs with on-chip DC block and 50Ω adaptation
- On-Chip background calibration
- Digital Down Conversion (DDC)
  - I/Q down conversion, with 2 to 1024 ratios
  - 1 coarse or up to 4 fine selectable channels
  - 4 independent NCOs per channel
- Fast Frequency Hopping, with dedicated deterministic controls and 3 hop options:
  - RTZ
  - Phase Continuous
  - Coherent on 4 frequencies
- Digital Delays : integer and fractional
- 11 synchronous HSSLs
- ESIstream 62/64b protocol
- Multi-ADC synchronization capability
- 3.3V / 1.8V / 1.2V / 0.9V power supplies
- Flexible 1.2V to 1.8V SPI supply
- 16.0x17.6mm² organic FCBGA
- 350 balls (SAC305) with 0.8mm pitch
- Temperature range: -55°C (T_{case}) to 125°C (T_j)
- RoHS (Pb-Free)

PERFORMANCE

- ENOB: 7.0 bits
- Fs=6.6GHz, Fin=14.1GHz, Pout=-6dBFS
  - SFDR = -52dBc
  - H2 = -61.8dBc / H3 = -52dBc
- Fs=6.6GHz, Fin=17.4GHz, Pout=-6dBFS
  - SFDR = -54.1dBc
  - H2 = -54.1dBc / H3 = -55.1dBc
- Fs=10.3GHz, Fin=28.4GHz, Pout=-6dBFS
  - SFDR = -47.5dBc
  - H2 = -47.5dBc / H3 = -50.2dBc
- Fs=12.8GHz, Fin=4.1GHz, Pout=-6dBFS
  - SFDR = -54.5dBc
  - H2 = -61dBc / H3 = -54.6dBc
- Fs=12.8GHz, Fin=14.1GHz, Pout=-6dBFS
  - SFDR = -50.2dBc
  - H2 = -58.5dBc / H3 = -50.2dBc
- Fs=12.8GHz, Fin=17.4GHz, Pout=-6dBFS
  - SFDR = -50.4dBc
  - H2 = -59.8dBc / H3 = -50.4dBc
- Fs=12.8GHz, Fin=28.4GHz, Pout=-6dBFS
  - SFDR = -50.5dBc
  - H2 = -50.5dBc / H3 = -54dBc
- Fs=12.8GHz, Fin=40.5GHz, Pout=-6dBFS
  - SFDR = -32.1dBc
  - H2 = -32.1dBc / H3 = -43.4dBc
- RF input S11 < -18dB up to 32GHz
- RF input S11 < -15dB up to 40GHz
- Clock input S11 < -18dB up to 19GHz

APPLICATION

- HTS Satellite Communication
- Radar
- SAR
- 5G
- P2P communications

Table of Content

1. DOCUMENT HISTORY

Issue	Date	Comments
A	June 2022	Document creation
B	April 2023	Added register map Added register description Added theory of operation Added ESIstream description

2. BLOCK DIAGRAMS

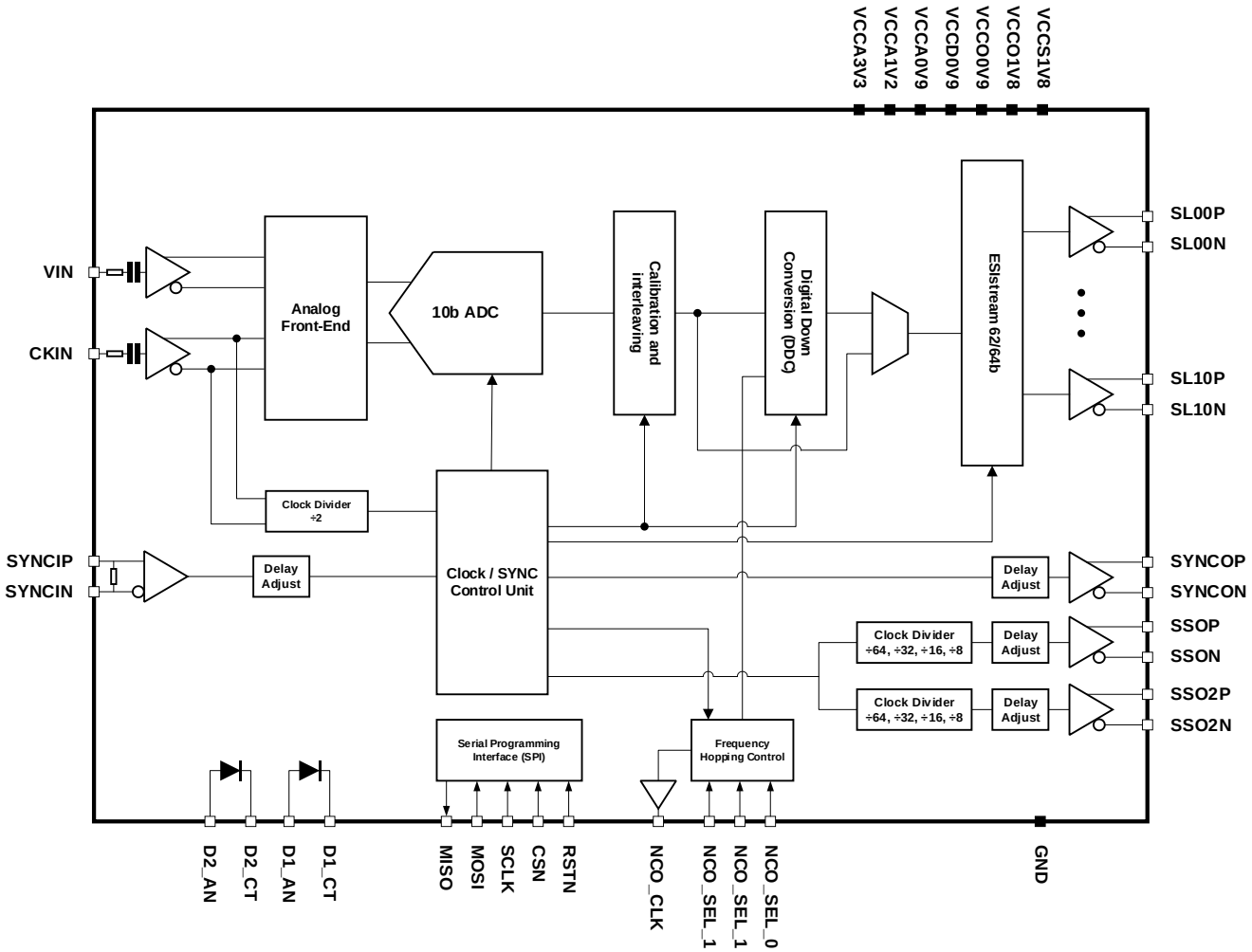


Figure 1 : EV10AS940 Block Diagram.

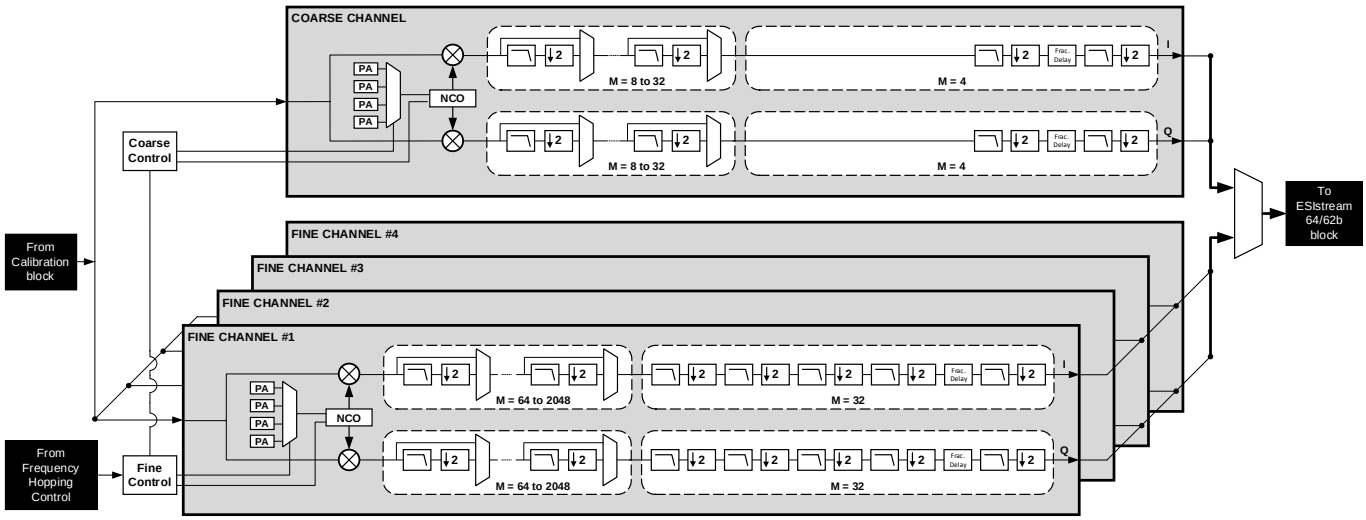


Figure 2 : Digital Down Conversion (DDC) Block Diagram.

3. DESCRIPTION

EV10AS940 is a high-performance single channel, 10-bit, 12.8GSps Analog-to-Digital Converter (ADC) that allows sampling of RF signals up to the Ka-band. The high analog input bandwidth (33GHz) makes the EV10AS940 the best candidate to address RF direct conversion architectures, as it allows optimizing the signal chain by eliminating the need to integrate a dedicated mixer.

The device operates at a very efficient power consumption as low as 2.5W, while it features 11 ESIstream serial links that operate synchronously with the sampling clock to help achieving a deterministic data transfer.

Both signal and clock inputs are single ended to ease board and system design.

EV10AS940 also features Digital Down Conversion (DDC) functionality with multiple options for decimation rates and up to 4 independent NCOs to support Frequency Hopping in multiband operations. Coherent Frequency Hopping is possible thanks to multiple phase accumulators on each NCO and deterministic dedicated hopping trigger I/Os.

Digital integer and fractional delays enable Beam Forming capability allowing the EV10AS940 to be used in Phased Arrays applications.

Main features:

- 4 DDC channels
- I/Q decimation ratios from 2 to 1024
- Deterministic Frequency Hopping with RTZ, Continuous and Coherent modes
- Dedicated Frequency Hopping I/Os
- Beam forming capabilities, with fractional delay
- Background calibration
- Temperature calibration
- ESIstream 62/64b
- HSSL reach selection
- HSSL Impedance control (2 x 50Ω+/- 20%)

4. SPECIFICATION

4.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values withstand individually, while other parameters are within specified operating conditions (1). **Long exposure to maximum rating may affect device reliability**.

Table 1: Absolute Maximum Ratings.

Parameter	Symbol	Min	Max	Unit
Analog supply voltage 3.3V	V_{CCA3V3} (2)	-0.3	3.6	V
Analog supply voltage 1.2V	V_{CCA1V2} (2)	-0.3	1.32	V
Analog supply voltage 0.9V	V_{CCA0V9} (2)	-0.3	1.00	V
Digital supply voltage 0.9V	V_{CCD0V9} (3)	-0.3	1.00	V
Serial Link IO supply voltage 0.9V	V_{CCO0V9} (4)	-0.3	1.00	V
GPIO supply voltage 1.8V	V_{CCO1V8} (4)	-0.3	2.00	V
SPI supply voltage 1.2 to 1.8V	V_{CCS1V8} (4)	-0.3	2.00	V
Analog input peak voltage	V_{IN}	-0.3	V_{CCA3V3} + 0.3	V
Clock input voltage	V_{CLK}	-0.3	V_{CCA3V3} + 0.3	V
SPI input voltage	CSN, SCLK, RSTN, MOSI	-0.3	V_{CCS1V8} + 0.3	V
GPIO input voltage	NCO_SEL1,2,3	-0.3	V_{CCO1V8} + 0.3	V
SYNC input voltage	V_{SYNCP} or V_{SYNCN}	-0.3	V_{CC01V8} + 0.3	V
Maximum difference between V_{SYNCP} and V_{SYNCN}	$\|V_{SYNCP} - V_{SYNCN}\|$		1.5	Vppdiff
Maximum Swing V_{IN} (AC signal)	V_{IN}		2	Vpp
Maximum Swing V_{CLK} (AC signal)	V_{CLK}		2	Vpp
Max Junction Temperature	T_j	-	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Input voltage on to prevent leakage (D1_C=GND)	DIODE 1	TBD	TBD	V
Input voltage on D2_A to prevent leakage (D2_C=GND)	DIODE 2	TBD	TBD	V
Maximum input current on DIODE	DIODE ADC		TBD	mA

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Lifetime Qualification Ratings.
(2) Measured to AGND.
(3) Measured to DGND.
(4) Measured to GNDIO.

4.2 ESD and Latchup Ratings

All integrated circuits must be handled with appropriate care to avoid damages due to ESD. Damages caused by inappropriate handling or storage could range from performance degradation to complete failure.

Table 2: ESD and Latchup Ratings.

Parameter	Symbol	Value	Unit
Human-body model (HBM), per ESDA/JEDEC JS-001-2017	HBM	1000	V
Charged-device model (CDM), per ESDA/JEDEC JS-002-2018	CDM	250	V
Latch-Up, per JEDEC J78E	LU	±100	mA

4.3 Radiation Tolerance Ratings

The EV10AS940 targets space, military, and industrial applications. To be compliant with space requirements, the component should be tolerant to radiation effects, and thus should comply with the following conditions:

Table 3: Radiation Tolerance Ratings.

Parameter	Symbol	Value	Unit
Total Ionizing Dose (1)	TID	100	krad
SEL and SEFI immune up to a LET	SEE	80	MeV.cm^2/mg

(1) At low dose rate of 36 rad/h (Si)

4.4 Lifetime Qualification Ratings

EV10AS940 is designed, manufactured, and will be qualified to be compliant with space requirements (ESCC9000P and MIL-PRF 38535 with amendments).

Table 4 : Recommended Junction (Tj) Temperature Conditions of Use

Parameter	Symbol	Value	Unit
Operating life at Tj = +125 °C	HTOL	10	Years
Operating life at Tj = +110 °C	HTOL	15	Years

4.5 Recommended Conditions of Use

AGND, DGND and GNDIO must be tied to a common ground plane (GND) on the circuit board.

Table 5: Recommended Conditions of Use

Parameter	Symbol	Comments	Value	Unit
Positive Analogue supply voltage 3.3V	V_{CCA3V3}	Analog part	3.3	V
Positive Analogue supply voltage 1.2V	V_{CCA1V2}	Analog part	1.2	V
Positive Analogue supply voltage 0.9V	V_{CCA0V9}	Analog part	0.9	V
Positive Digital supply voltage 0.9V	V_{CCD0V9}	Digital part	0.9	V
Positive Serial link IO supply voltage 0.9V	V_{CCO0V9}	CML buffers	0.9	V
Positive GPIO supply voltage 1.8V	V_{CCO1V8}	LVDS buffers	1.8	V
Positive SPI supply voltage 1.2 to 1.8V	V_{CCS1V8}	SPI buffers	1.2 / 1.5 / 1.8	V
Analog input power (Full Scale)	P_{IN}		-2	dBm
Clock input power	P_{CLK}		2	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0 1.2 / 1.5 / 1.8	V
External Clock frequency	F_{CLK}		$6.4 \le F_{CLK} \le 12.8$	GHz
External Clock duty-cycle	DC		$45 \le DC \le 55$	%
Operating Temperature Range	T_{case} T_j		$-55 \le T_{case}$ $T_j \le 125$	°C
Clock Jitter (max. allowed on clock source) for 35GHz sinewave analog input	Jitter	To achieve the listed performance	30	fs_{rms}

4.6 Explanation of test levels

Table 6 : Explanation of Test Levels.

Test Level	Comment
1A	100% tested over specified temperature range and specified power supply range
1B	100% tested over specified temperature range at typical power supplies
1C	100% tested at +25°C, over specified supply range
1D	100% tested at +25°C, at typical power supplies
2	100% production tested at +25°C and samples tested at specified temperatures
3	Samples tested only at specified temperatures
4	Parameter value is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design

4.7 Electrical Characteristics for Supplies, Inputs and Outputs

Unless otherwise specified, typical values are given at Tj=50°C with Fs=12.8GSps, no DDC activated, no background calibration, HSSL in Reduced Swing (RS) mode, NCO_CLK, SSO2 and SYNCO disabled, and for the following typical supplies V_{CCA3V3} = 3.3V, V_{CCA1V2} = 1.2V, V_{CCA0V9} = 0.9V, V_{CCD0V9} = 0.9V, V_{CCO0V9} = 0.9V, V_{CCO1V8} = 1.8V, V_{CCS1V8} = 1.8V The considered junction temperature T_j is that of the hotspot. Minimum and Maximum values are given over temperature.

Table 7 : Electrical Characteristics for Supplies, Inputs and Outputs.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
RESOLUTION	5			10		bit
POWER REQUIREMENTS						
Power Supply voltage						
- Analog 3.3V	4	V_{CCA3V3}	3.2	3.3	3.4	V
- Analog 1.2V		V_{CCA1V2}	1.15	1.2	1.25	V
- Analog 0.9V		V_{CCA0V9}	0.85	0.9	0.95	V
- Digital 0.9V		V_{CCD0V9}	0.85	0.9	0.95	V
- HSSL 0.9V		V_{CCO0V9}	0.85	0.9	0.95	V
- GPIO 1.8V		V_{CCO1V8}	1.70	1.8	1.90	V
- SPI 1.8V		V_{CCS1V8}	1.15	1.2/1.5/1.8	1.90	V
Power Supply current						
- Analog 3.3V	4	I_{CCA3V3}		425	430	mA
- Analog 1.2V		I_{CCA1V2}		475	512	mA
- Analog 0.9V		I_{CCA0V9}		120	150	mA
- Digital 0.9V		I_{CCD0V9}		280	345	mA
- HSSL 0.9V		I_{CCO0V9}		120	128	mA
- GPIO 1.8V		I_{CCO1V8}		30	30	mA
- SPI 1.8V		I_{CCS1V8}		1	2	mA
Power dissipation (standby mode)						
- Analog 3.3V						
• Partial stand-by mode (clock path ON)		P_{CCA3V3}		0.42	0.43	W
• Full stand-by mode		P_{CCA3V3}		0.15	0.16	W
- Analog 1.2V		P_{CCA1V2}		TBD	TBD	W
- Analog 0.9V		P_{CCA0V9}		TBD	TBD	W
- Digital 0.9V		P_{CCD0V9}		TBD	TBD	W
- HSSL 0.9V		P_{CCO0V9}		TBD	TBD	W
- GPIO 1.8V		P_{CCO0V9}		TBD	TBD	W
- SPI 1.8V		P_{CCO1V8}		TBD	TBD	W
		P_{CCS1V8}		TBD	TBD	W
Power dissipation						
Full analog power mode	4	P_D		2.50	2.65	W
Standby mode				TBD	TBD	W
ANALOG INPUT (VIN)						
Common mode compatibility for analog inputs				AC		
Full-Scale input voltage range		V_{IN-pp}			500	mVpp
Analog input power level (in 50Ω termination)		P_{IN}			-2	dBm
Input leakage current		I_{IN}		TBD		µA
Input resistance (single)	4	R_{IN}	40	50	60	Ω
CLOCK INPUT (CKIN)						
Common mode compatibility for clock input				AC		
Intrinsic clock jitter (1)				28		fs_{rms}
Clock input power level in 50Ω	4	P_{CLK}		2		dBm
Clock single input voltage	4	$\lvert V_{CLK} \rvert$		800		mVpp
Clock input slew rate (square or sinewave clock)		SR_{CLK}		40		GV/s
Clock input capacitance (die + package)		C_{CLK}		TBD		pF
Clock input resistance (single)		R_{CLK}	40	50	60	Ω
Clock duty cycle		Duty Cycle	45	50	55	%

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
CMOS INPUTS SPI (CSN, RSTN, SCLK, MOSI), FREQUENCY HOPPING (NCO_SEL0, NCO_SEL1, NCO_SEL2)						
Low level threshold of Schmitt trigger		$V_{TminusC}$			0.30*V_{CCS1V8}	V
High level threshold of Schmitt trigger		V_{TplusC}	0.70*V_{CCS1V8}			V
CMOS Schmitt trigger hysteresis		V_{HYSTC}	0.10*V_{CCS1V8}			V
CMOS low level input current (Vinc=0 V)		I_{ILC}			0.3	µA
CMOS high level input current (Vinc= V_{CCS1V8} max)		I_{IHC}			15	µA
CMOS OUTPUTS SPI (MISO), FREQUENCY HOPPING (NCO_CLK)						
CMOS low level output voltage (Iolc = 3 mA)		V_{OLC}			0.20*V_{CCS1V8}	V
CMOS high level output voltage (Iohc = 3 mA)		V_{OHC}	0.8*V_{CCS1V8}			V
SYNC INPUT (SYNCIN/P)						
Logic compatibility				LVDS		
Input voltages to be applied • Swing • Common mode (DC Coupled)		 V_{IH}-V_{IL} V_{ICM}	 100 1.00	 350 1.25	 600 1.50	 mV V
Input capacitance		CSYNC		0.5		pF
Input resistance		RSYNC	80	100	120	Ω
SYNC OUTPUTS (SYNCON/P, SSON/P, SSO2N/P)						
Logic compatibility				LVDS		
Output levels (full swing) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination) • Logic low • Logic high • Differential output • Common mode (2)		 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}	 1.25 250 1.025	 350 1.25	 1.25 450 1.375	 V V mV V
Outputs levels in power down mode		Outp/Outn		1.8		V
High Speed Serial Links OUTPUTS (SLxN/P with x = 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 10)						
Logic compatibility	5			CML		
Operating mode	5			Synchronous		
Output levels in full swing (FS) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination • Logic low • Logic high • Differential output • Common mode	 3	 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}		 V_{CCO0V9}-0,55 V_{CCO0V9}-0.21 780 V_{CCO0V9}-0,38		 V V mVpp-diff V
Output levels in reduced swing (RS) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination • Logic low • Logic high • Differential output • Common mode	 3	 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}		 V_{CCO0V9}-0,41 V_{CCO0V9}-0.16 500 V_{CCO0V9}-0.28		 V V mVpp-diff V
Output levels in short distance (SD) 50Ω transmission lines, 100Ω (2 x 50Ω differential termination • Logic low • Logic high • Differential output • Common mode	 3	 V_{OL} V_{OH} V_{OH}-V_{OL} V_{OCM}		 V_{CCO0V9}-0,33 V_{CCO0V9}-0.13 400 V_{CCO0V9}-0.23		 V V mVpp-diff V

(1) Intrinsic jitter integrated from 1Hz to 29GHz.
(2) DC coupled mandatory for SYNCON/P.

4.8 Converter's Characteristics

Unless otherwise specified, typical values are given at Tj=50°C with Fs=12.8GSps, P_{CLK} = +2dBm, no DDC activated, no background calibration, HSSL in Reduced Swing (RS) mode, NCO_CLK, SSO2 and SYNCO disabled, and for the following typical supplies V_{CCA3V3} = 3.3V, V_{CCA1V2} = 1.2V, V_{CCA0V9} = 0.9V, V_{CCD0V9} = 0.9V, V_{CCO0V9} = 0.9V, V_{CCO1V8} = 1.8V, V_{CCS1V8} = 1.8V
Minimum and Maximum values are given over temperature.

Table 8 : Low Frequency Characteristics.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
DC ACCURACY						
Gain variation versus temperature		G(T)	- 0.5		+0.5	dB
Gain variation versus process		GAINVAR	- 0.1		+0.1	dB

Table 9 : Dynamic Characteristics.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC ANALOG INPUT						
Full power input bandwidth (-3dB)	4	FPBW		33		GHz
Input Voltage Standing Wave Ratio • 900MHz up to 5GHz • 5GHz up to 18GHz • 18GHz up to 32GHz • 32GHz up to 40GHz		VSWR		 1.43:1 1.19:1 1.23:1 1.43:1		
Return Loss • 900MHz up to 5GHz • 5GHz up to 18GHz • 18GHz up to 32GHz • 32GHz up to 40GHz	4	S11	 -15 -16 -12 -10		 -16 -27 -18 -19	dB
AC CLOCK INPUT						
Return Loss • 900MHz – 19GHz		S11	 -14		 -19	dB
DYNAMIC PERFORMANCE						
Spurious Free Dynamic Range (Single Tone) Fin=1.1 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin=6.7 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin=15.6 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 28,2 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 34.5 GHz • -1 dBFS • -3 dBFS • -6 dBFS Fin= 40.5 GHz • -1 dBFS • -3 dBFS • -6 dBFS		SFDR		 40 45 50 40 45 49 40 45 50 43 47 50 - - 41 - - 32		dBc

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
2nd Harmonic (Single Tone)						
Fin=1.1 GHz						
• -1 dBFS				-49		
• -3 dBFS				-53		
• -6 dBFS				-59		
Fin=6.7 GHz						
• -1 dBFS				-49		
• -3 dBFS				-53		
• -6 dBFS				-59		
Fin=15.6 GHz						
• -1 dBFS				-50		
• -3 dBFS				-54		
• -6 dBFS		H2		-60		dBc
Fin= 28.2 GHz						
• -1 dBFS				-43		
• -3 dBFS				-47		
• -6 dBFS				-50		
Fin= 34.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-41		
Fin= 40.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-32		
3rd Harmonic (Single Tone)						
Fin=1.1 GHz						
• -1 dBFS				-41		
• -3 dBFS				-45		
• -6 dBFS				-49		
Fin=6.7 GHz						
• -1 dBFS				-46		
• -3 dBFS				-50		
• -6 dBFS				-54		
Fin=15.6 GHz						
• -1 dBFS				-42		
• -3 dBFS				-46		
• -6 dBFS		H3		-50		dBc
Fin= 28.2 GHz						
• -1 dBFS				-46		
• -3 dBFS				-50		
• -6 dBFS				-54		
Fin= 34.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-44		
Fin= 40.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-43		

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
THD (Single Tone)						
Fin=1.1 GHz						
• -1 dBFS				-39		
• -3 dBFS				-44		
• -6 dBFS				-49		
Fin=6.7 GHz						
• -1 dBFS				-39		
• -3 dBFS				-44		
• -6 dBFS				-48		
Fin=15.6 GHz						
• -1 dBFS				-39		
• -3 dBFS				-44		
• -6 dBFS		THD		-49		dBc
Fin= 28.2 GHz						
• -1 dBFS				-40		
• -3 dBFS				-45		
• -6 dBFS				-49		
Fin= 34.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-40		
Fin= 40.5 GHz						
• -1 dBFS				-		
• -3 dBFS				-		
• -6 dBFS				-32		
SNR						
Fin=1.1 GHz						
• -1 dBFS				46		
• -3 dBFS				46		
• -6 dBFS				46		
Fin=6.7 GHz						
• -1 dBFS				45		
• -3 dBFS				46		
• -6 dBFS				46		
Fin=15.6 GHz						
• -1 dBFS				42		
• -3 dBFS				43		
• -6 dBFS		SNR		45		dBFS
Fin= 28.2 GHz						
• -1 dBFS				40		
• -3 dBFS				42		
• -6 dBFS				45		
Fin= 34.5 GHz						
• -1 dBFS				39		
• -3 dBFS				41		
• -6 dBFS				44		
Fin= 40.5 GHz						
• -1 dBFS				38		
• -3 dBFS				40		
• -6 dBFS				43		

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
SINAD						
Fin=1.1 GHz						
• -1 dBFS				43		
• -3 dBFS				44.5		
• -6 dBFS				46		
Fin=6.7 GHz						
• -1 dBFS				39.5		
• -3 dBFS				43		
• -6 dBFS				46		
Fin=15.6 GHz						
• -1 dBFS				40		
• -3 dBFS				42		
• -6 dBFS		SINAD		45		dBFS
Fin= 28.2 GHz						
• -1 dBFS				40		
• -3 dBFS				42		
• -6 dBFS				45		
Fin= 34.5 GHz						
• -1 dBFS				39		
• -3 dBFS				41		
• -6 dBFS				44		
Fin= 40.5 GHz						
• -1 dBFS				37		
• -3 dBFS				40		
• -6 dBFS				43		
ENOB						
Fin=1.1 GHz						
• -1 dBFS				6.8		
• -3 dBFS				7.1		
• -6 dBFS				7.3		
Fin=6.7GHz						
• -1 dBFS				6.3		
• -3 dBFS				6.8		
• -6 dBFS				7.3		
Fin=15.6 GHz						
• -1 dBFS				6.3		
• -3 dBFS				6.8		
• -6 dBFS		ENOB		7.2		bits
Fin= 28.2GHz						
• -1 dBFS				6.4		
• -3 dBFS				6.7		
• -6 dBFS				7.2		
Fin= 34.5GHz						
• -1 dBFS				6.2		
• -3 dBFS				6.5		
• -6 dBFS				7.0		
Fin= 40.5GHz						
• -1 dBFS				5.9		
• -3 dBFS				6.3		
• -6 dBFS				6.8		
Noise Spectral Density						
• **@ -1 dBFS**						
2nd Nyquist (6.4GHz – 12.8GHz)				-145		
3rd Nyquist (12.8GHz – 19.2GHz)				-145		
4th Nyquist (19.2GHz – 25.6GHz)				-144		
5th Nyquist (25.6GHZ – 32.0GHz)				-140		
6th Nyquist (32.0GHz – 38.4GHz)		NSD		-139		dBFS/Hz
• **@ -6 dBFS**						
2nd Nyquist (6.4GHz – 12.8GHz)				-146		
3rd Nyquist (12.8GHz – 19.2GHz)				-146		
4th Nyquist (19.2GHz – 25.6GHz)				-145.5		
5th Nyquist (25.6GHZ – 32.0GHz)				-145		
6th Nyquist (32.0GHz – 38.4GHz)				-144		

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Noise Power Ratio (NPR) @ -14 dB LF (5.1GHz input pattern, 50MHz notch folded at $F_s/4$)						
2nd Nyquist (6.4GHz – 12.8GHz)		NPR		35.0		dB
3rd Nyquist (12.8GHz – 19.2GHz)				35.0		
4th Nyquist (19.2GHz – 25.6GHz)				34.5		
5th Nyquist (25.6GHZ – 32.0GHz)				34.0		
6th Nyquist (32.0GHz – 38.4GHz)				33.5		

4.9 Transient and Switching Characteristics

Table 10: Transient characteristics.

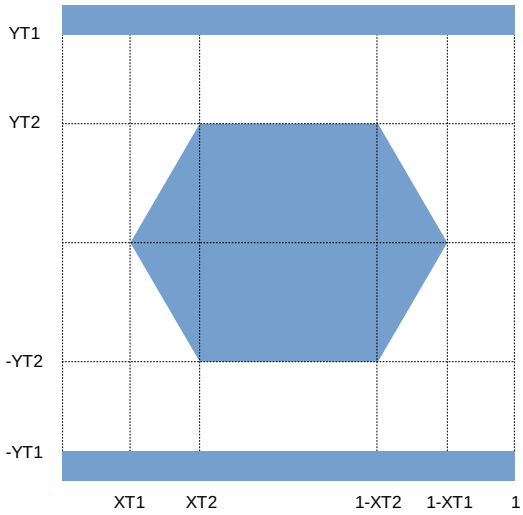
Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Conversion Error Rate at 12.8GSps less than 128 LSB (TBC) (1)		CER			10^{-14}	Error/ Sample
Serial link Bit Error Rate at 12.8Gbps		BER			10^{-15}	Error/ Sample

(1) F_{CLK} = 12.8 GHz, T_J = 110 °C

Table 11: Switching characteristics.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
COMMON CHARACTERISTICS						
External clock frequency		F_{CLK}	6.4		12.8	GHz
Sampling frequency		F_S	6.4		12.8	GHz
Aperture Jitter		Jitter		TBD		fs_{RMS}
CML OUTPUTS						
Output rise time (20%-80%) (1)		TR			30 (TBC)	ps
Output fall time (20%-80%) (1)		TF			30 (TBC)	ps
Total jitter @ 12.8Gbps (1)		2XT1			23.4	ps
Time to reach 100% amplitude @ 12.8Gbps (1)		XT2			31.2	ps
Maximum amplitude @ 12.8Gbps (1)		YT1			450	mV
Minimum amplitude @ 12.8Gbps (1)		YT2	140			mV
Skew between serial output signal P and N (1)		Tskew			0.6 (TBC)	ps
Crosstalk from SLx+1 on SLx @ 12.8Gbps (1)		XTALK_SL2SL			-40 (TBC)	dB
Max crosstalk from SLx on analog input signal @ 12.8Gbps (1)		XTALK_SL2IN			-80 (TBC)	dB
LVDS INPUTS AND OUTPUTS (SSO, SSO2, SYNCI, SYNCO)						
Output rise time (20%-80%)		RT				
Output fall time (20%-80%)		FT				
SSO jitter		Jitter				
SSO2 jitter		Jitter				
SYNCIN pulse width		T_{SYNC}	TBD			
SYNCIN to data pipeline delay (DDC disabled)		TPD				
SYNCI sampling delay tuning range			0		434	ps
SYNCO sampling delay tuning range			0		434	ps
SSO sampling delay tuning range			0		434	ps
SSO2 sampling delay tuning range			0		434	ps
CKIN to SYNCO pipeline delay						
CKIN to SYNCO delay						
CKIN to SSO delay						
CKIN to SSO2 delay						

(1) 100Ω load + PCB line 17cm.



(2) Figure 3: Serial link eye diagram. Blue areas are forbidden.

Table 12 : SPI Timing Characteristics.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
RSTN pulse length		T_{RSTN}	10			µs
SCLK frequency		F_{SCLK}			50	MHz
CSN to SCLK delay		$T_{CSN-SCLK}$				T_{SCLK}
MOSI setup time		T_{setup}				ns
MOSI hold time		T_{hold}				ns
MISO output delay		T_{delay}				ns

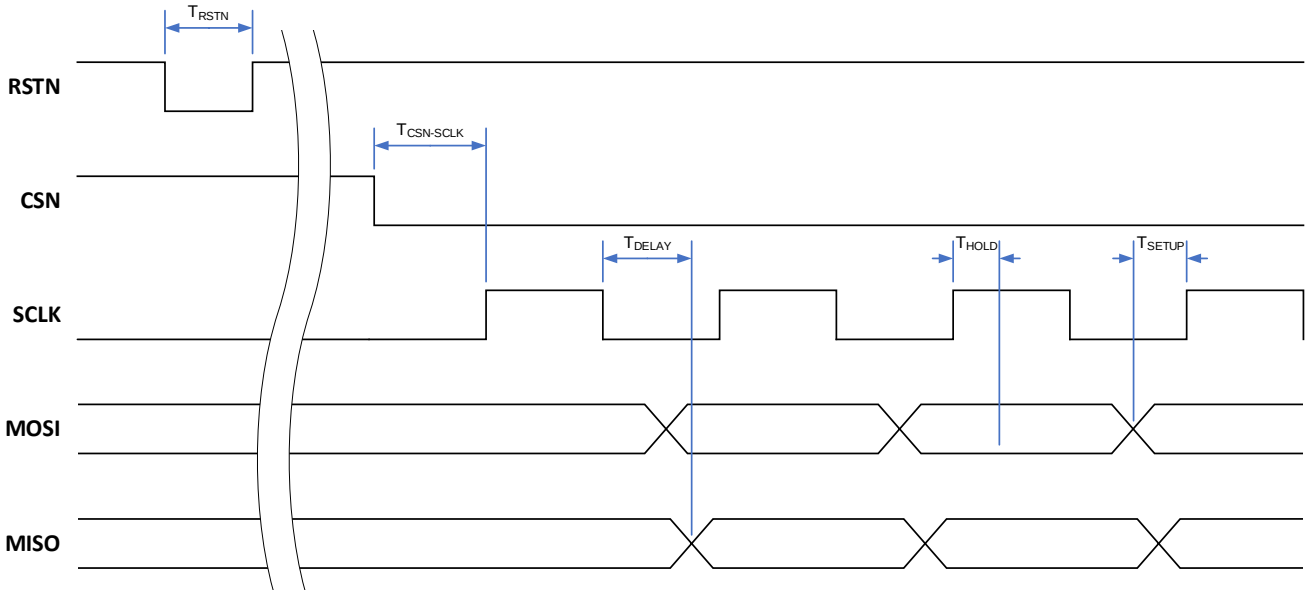


Figure 4 : SPI Timing Diagram.

5. PIN CONFIGURATION AND FUNCTIONS

5.1 Pinout Top View

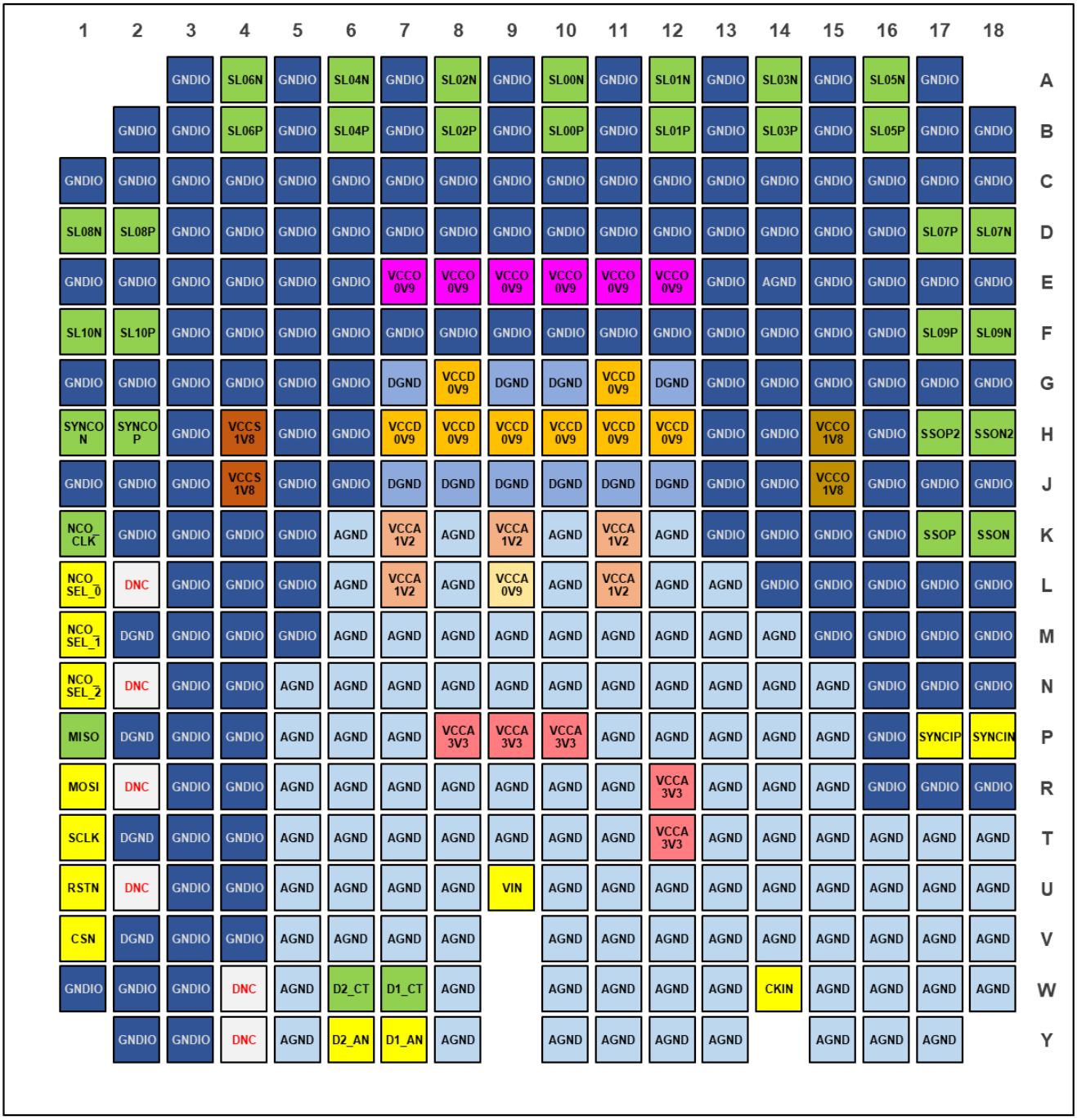


Figure 5 : EV10AS940 Pinout.

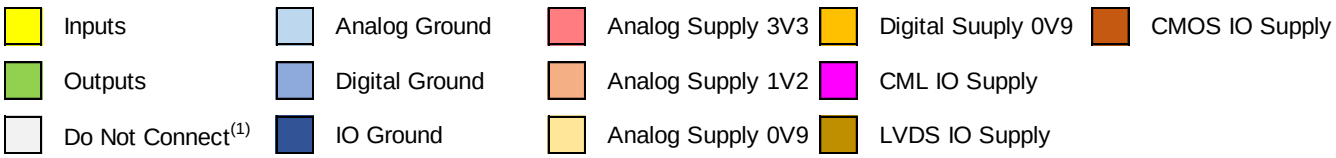


Figure 6 : Pinout Color Description.

(1) Note that “Do Not Connect” pins should be left floating.

5.2 Pin Function Description

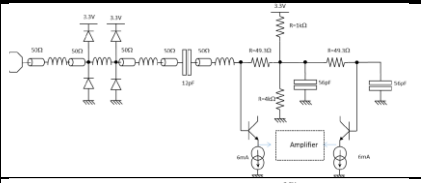
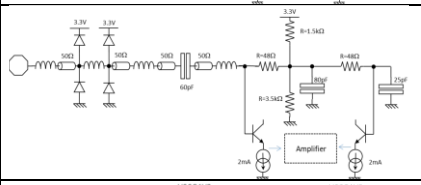
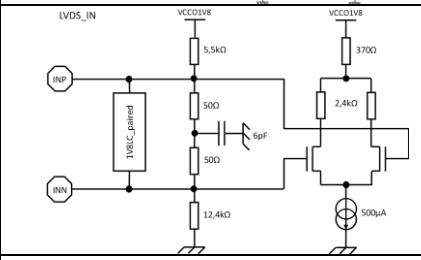
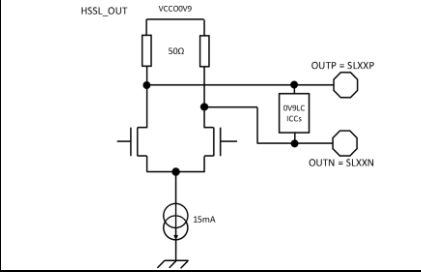
Table 13 : Pin Function Description.

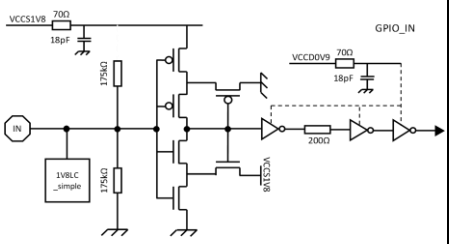
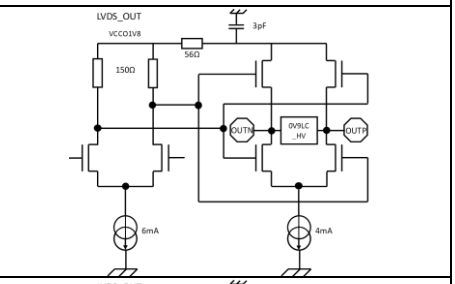
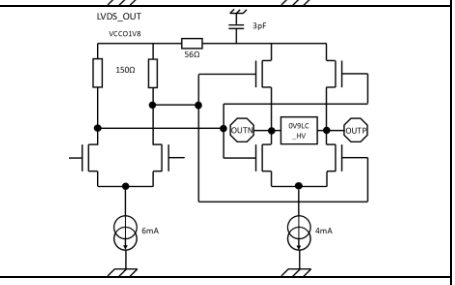
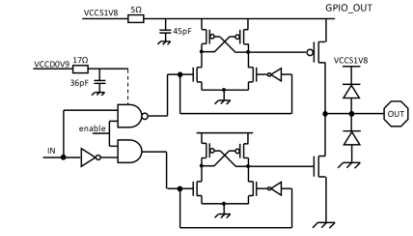
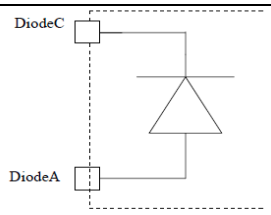
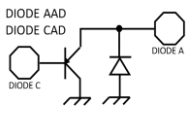
Pin No.	Mnemonic	Type	Description
POWER SUPPLIES			
8P, 9P, 10P, 12R, 12T	VCCA3V3	S	Analog 3.3V Supply
7K, 9K, 11K, 7L, 11L	VCCA1V2	S	Analog 1.2V Supply
9L	VCCA0V9	S	Analog 0.9V Supply
8G, 11G, 7H, 8H, 9H, 10H, 11H, 12H	VCCD0V9	S	Digital 0.9V Supply
15H, 15J	VCCO1V8	S	I/O (LVDS) 1.8V Supply
7E, 8E, 9E, 10E, 11E, 12E	VCCO0V9	S	I/O (CML) 0.9V Supply
4H, 4J	VCCS1V8	S	I/O (CMOS) Supply
GROUNDS			
6K, 8K, 10K, 12K, 6L, 8L, 10L, 12L, 13L, 6M, 7M, 8M, 9M, 10M, 11M, 12M, 13M, 14M, 5N, 6N, 7N, 8N, 9N, 10N, 11N, 12N, 13N, 14N, 15N, 5P, 6P, 7P, 11P, 12P, 13P, 14P, 15P, 5R, 6R, 7R, 8R, 9R, 10R, 11R, 13R, 14R, 15R, 5T, 6T, 7T, 8T, 9T, 10T, 11T, 13T, 14T, 15T, 16T, 17T, 18T, 5U, 6U, 7U, 8U, 10U, 11U, 12U, 13U, 14U, 15U, 16U, 17U, 18U, 5V, 6V, 7V, 8V, 10V, 11V, 12V, 13V, 14V, 15V, 16V, 17V, 18V, 5W, 8W, 10W, 11W, 12W, 13W, 15W, 16W, 17W, 18W, 5Y, 8Y, 10Y, 11Y, 12Y, 13Y, 15Y, 16Y, 17Y	AGND	G	Analog Ground Reference. Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board
7G, 9G, 10G, 12G, 7J, 8J, 9J, 10J, 11J, 12J	DGND	G	Digital Ground Reference. Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board
3A, 5A, 7A, 9A, 11A, 13A, 15A, 17A, 2B, 3B, 5B, 7B, 9B, 11B, 13B, 15B, 17B, 18B, 1C, 2C, 3C, 4C, 5C, 6C, 7C, 8C, 9C, 10C, 11C, 12C, 13C, 14C, 15C, 16C, 17C, 18C, 3D, 4D, 5D, 6D, 7D, 8D, 9D, 10D, 11D, 12D, 13D, 14D, 15D, 16D, 1E, 2E, 3E, 4E, 5E, 6E, 13E, 14E, 15E, 16E, 17E, 18E, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 10F, 11F, 12F, 13F, 14F, 15F, 16F, 1G, 2G, 3G, 4G, 5G, 6G, 13G, 14G, 15G, 16G, 17G, 18G, 3H, 5H, 6H, 13H, 14H, 16H, 1J, 2J, 3J, 5J, 6J, 13J, 14J, 16J, 17J, 18J, 2K, 3K, 4K, 5K, 13K, 14K, 15K, 16K, 3L, 4L, 5L, 14L, 15L, 16L, 17L, 18L, 2M, 3M, 4M, 5M, 15M, 16M, 17M, 18M, 3N, 4N, 16N, 17N, 18N, 2P, 3P, 4P, 16P, 3R, 4R, 16R, 17R, 18R, 2T, 3T, 4T, 3U, 4U, 2V, 3V, 4V, 1W, 2W, 3W, 2Y, 3Y	GNDIO	G	I/O Ground Reference. Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board
ESISTEAM OUTPUTS			
10A, 10B	SL00N, SL00P	O	Tx Lane 0 Outputs, (N/P)
12A, 12B	SL01N, SL01P	O	Tx Lane 1 Outputs, (N/P)
8A, 8B	SL02N, SL02P	O	Tx Lane 2 Outputs, (N/P)
14A, 14B	SL03N, SL03P	O	Tx Lane 3 Outputs, (N/P)
6A, 6B	SL04N, SL04P	O	Tx Lane 4 Outputs, (N/P)
16A, 16B	SL05N, SL05P	O	Tx Lane 5 Outputs, (N/P)
4A, 4B	SL06N, SL06P	O	Tx Lane 6 Outputs, (N/P)
18D, 17D	SL07N, SL07P	O	Tx Lane 7 Outputs, (N/P)
1D, 2D	SL08N, SL08P	O	Tx Lane 8 Outputs, (N/P)
18F, 17F	SL09N, SL09P	O	Tx Lane 9 Outputs, (N/P)
1F, 2F	SL10N, SL10P	O	Tx Lane 10 Outputs, (N/P)
LVDS INPUTS/OUTPUTS			
18P, 17P	SYNCIN, SYNCIP	I	Sync Inputs
18K, 17K	SYNCON, SYNCOP	O	Sync Outputs
1H, 2H	SSON, SSOP	O	System Reference Clock 1

Pin No.	Mnemonic	Type	Description
18H, 17H	SSON2, SSOP2	O	System Reference Clock 2
CMOS INPUTS/OUTPUTS			
1T	SCLK	I	SPI Clock Input
1P	MISO	O	SPI Data Output
1R	MOSI	I	SPI Data Input
1V	CSN	I	SPI Enable Input
1U	RSTN	I	SPI Active Low Reset Input
1K	NCO_CLK	O	NCO Synchronization Clock Output
1L, 1M, 1N	NCO_SEL_0, NCO_SEL_1, NCO_SEL_2	I	NCO Mode Selection Inputs
ANALOG INPUTS/OUTPUTS			
14W	CKIN	I	Clock Input
9U	VIN	I	RF Input
6Y, 7Y	D1_AN, D2_AN	I	Anode of Temperature Diodes 1 and 2
6W, 7W	D1_CT D2_CT	O	Cathode of Temperature Diodes 1 and 2
UNCONNECTED			
2L, 2N, 2R, 2U, 4W, 4Y	DNC	N/A	DO NOT CONNECT

5.3 Electrical Characteristics for Supplies, Inputs and Outputs

Table 14 : Pins Electrical Characteristics.

Signal	Function	Description	Supply/ Ground	Simplified Electrical Schematic
VIN	RF input	Single Ended Input. 50Ω termination	VCCA3V3/ AGND	
CKIN	Clock input	Single Ended Input. 50Ω termination	VCCA3V3/ AGND	
SYNCIP/ SYNCIN	SYNC LVDS input	Differential Input DC-coupled Common mode: 1.25V Diff: 350mVpp-diff Vmax/min: 1.6/0.6V Freq: 800MHz max	VCCO1V8/ GNDIO	
SL00P/SL00N SL01P/SL01N SL02P/SL02N SL03P/SL03N SL04P/SL04N SL05P/SL05N SL06P/SL06N SL07P/SL07N SL08P/SL08N SL09P/SL09N SL10P/SL10N	CML output buffer	Differential Output AC-coupled Common mode: 520mV Diff: 680mVpp-diff Vmax/min: 690mV/350mV Freq: 12.8GHz max Load: 1.3pF max	VCCO0V9/ GNDIO	

Signal	Function	Description	Supply/ Ground	Simplified Electrical Schematic
NCO_SEL_0 NCO_SEL_1 NCO_SEL_2	NCO Mode Selection Inputs	Single Ended Input Vhmin: VCCS1V8-0.1V Vlmax: 0.1V Freq: 100MHz max Load: 1.5pF PD/PU Res: 175kΩ Pull-down if not driven	VCCS1V8/ GNDIO	
CSN SCLK MOSI RSTN	SPI programming inputs	Single Ended Input Vhmin: VCCS1V8-0.1V Vlmax: 0.1V Freq: 50MHz max Load: 1.5pF Pull Down/Pull Up Resistance: 175kΩ SCLK, MOSI Pull-Down CSN, RSTN Pull-Up if not driven	VCCS1V8/ GNDIO	
SSOP/SSON	LVDS output clock	Differential Output AC-coupled Common mode: 1.25V Diff: 350mVpp-diff Vmax/min: 1.6/0.9V Freq: 800MHz max Load: 500fF max	VCCO1V8/ GNDIO	
SSO2P/SSO2N	LVDS output clock		VCCO1V8/ GNDIO	
SYNCOP/ SYNCON	SYNC LVDS output	Differential Output DC-coupled Common mode: 1.25V Diff: 350mVpp-diff Vmax/min: 1.6/0.9V Freq: 800MHz max Load: 500fF max	VCCO1V8/ GNDIO	
MISO	SPI output buffer, with high-R state	Single Ended Vhmin: 0.8*VCCS1V8 Vlmax: 0.2*VCCS1V8 Freq: 100MHz max Load: 24pF max Undefined before Reset	VCCS1V8/ GNDIO	
NCO_CLK	Output clock for frequency hopping, with high-R state	Single Ended Vhmin: 0.8*VCCS1V8 Vlmax: 0.2*VCCS1V8 Freq: 100MHz max Load: 24pF max	VCCS1V8/ GNDIO	
D1_AN D1_CT	Anode and Cathode of first temperature junction diode		AGND	
D2_AN D2_CT	Anode and Cathode of second temperature junction diode		AGND	
VCCA0V9	Analog core power supply	0.9V supply max consumption: 150mA	AGND	
VCCA1V2	Analog core power supply	1.2V supply max consumption: 800mA	AGND	

Signal	Function	Description	Supply/ Ground	Simplified Electrical Schematic
VCCA3V3	Analog core power supply	3.3V supply max consumption: 420mA	AGND	
VCCD0V9	Digital core power supply	0.9V supply max consumption: 1.6A	DGND	
VCCO0V9	HSSL power supply	0.9V supply max consumption: 180mA	GNDIO	
VCCO1V8	LVDS power supply	1.8V supply max consumption: 40mA	GNDIO	
VCCS1V8	SPI power supply	1.2/1.5/1.8V supply max consumption: 30mA	GNDIO	
AGND	Analog core ground	Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board		
DGND	Digital core ground	Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board		
GNDIO	I/O ground	Tie AGND, DGND and GNDIO to a common ground plane (GND) on the circuit board		

6. DEFINITION OF TERMS

Table 15 : Definition of Terms.

Abbreviation	Term	Definition
BER	Bit Error Rate	Percentage of bits with errors divided by the total number of bits that have been transmitted, received or processed over a given time period.
CER	Code Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling Rate.
DDC	Digital Down Conversion	Signal data rate decrease through successive data rate division by two and half band filters to avoid aliasing
DNL	Differential nonlinearity	The Differential Non-Linearity for a given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there is no missing point and that the transfer function is monotonic.
ENOB	Effective Number Of Bits	$ENOB = \frac{SINAD - 1.76}{6.02}$
FPBW	Full Power Output Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at -1dBFS (Full scale – 1dB).
Fs	Sampling Frequency	Input sampling frequency
HSL	Highest Spur Level	Power of the highest spurious spectral component expressed in dBm
IMD3	Intermodulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
INL	Integral Nonlinearity	The Integral Non-Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs and is the maximum value of all |INL (i)|.
Jitter	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
LF	Loading Factor	The loading factor is 20log(1/k), where k is the rms value of the broadband signal. This parameter relates to the NPR measurement. The optimum loading factor for a 10bits converter is k = 4.5 corresponding to a loading factor of -13dB.
NCO	Numerically Controlled Oscillator	I/Q based oscillator generated by mixing the digital signal with sin/cosin patterns.
NPR	Noise Power Ratio	The NPR is measured to characterize the DAC performance with broadband output signals. When applying a notch-filtered broadband gaussian-noise pattern as the input to the DAC under test, the Noise Power Ratio is defined as the ratio of the average noise measured on the shoulder of the notch and inside the notch on the same integration bandwidth.
NSD	Noise Spectral Density	The NSD is the power spectral density magnitude of the ADC expressed in dBm/Hz.
OTP	One Time Programmable	OTP are fuses used to set circuit default configuration and calibrations.
SFDR	Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, set at Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It is reported in dBc (i.e., related to output signal level).
SINAD	Signal to Noise And Distortion ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SNR	Signal to Noise Ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the 10 first harmonics.
THD	Total Harmonic Distortion	Ratio expressed in dB of the RMS sum up to 10th harmonic components, to the RMS input signal amplitude. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).

VSWR	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e., 99% power transmitted and 1% reflected).

7. PACKAGE DESCRIPTION

7.1 Package Substrate Description

EV10AS940 package consists of a Flip-Chip Ball Grid Array (FC-BGA) organic substrate and Copper lid with Nickel finishing. The details of the package are:

- Package Technology: FC-BGA
- Package Dimensions: 16.0x17.6mm²
- Ball Count: 350
- Ball Pitch: 0.8mm
- Ball Diameter: 0.5mm
- Ball Material: SAC305
- MSL as per J-STD-033: TBD
- RoHS: Pb-Free

7.2 Package Outline

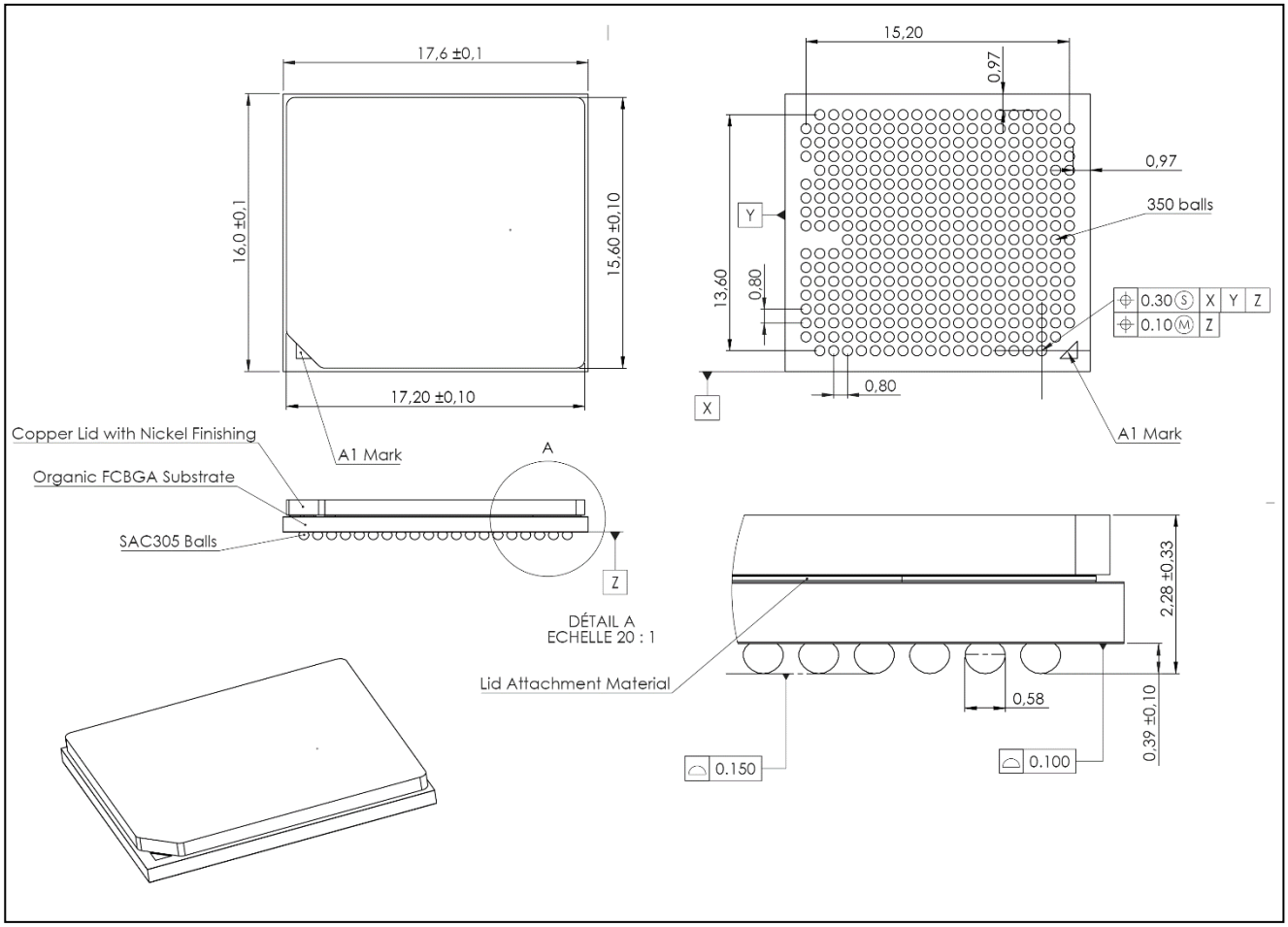


Figure 7 : EV10AS940 BGA Package Outline. (1)

(1) All dimensions in mm.

7.3 Thermal Characteristics

Table 16 :Thermal Characteristics.

Parameter	Symbol	Description	Value	Unit
Thermal resistance from junction to ambient (JEDEC JESD51-1/2/5/6/7/9) (1)(3)(5)	θ_{JA}	Rth Junction – Ambient	15.1	°C/W
Thermal resistance from junction to board (JEDEC JESD51-8) (1)(2)(4)(5)	θ_{JB}	Rth Junction - Board	7.2	°C/W
Thermal resistance from junction to top of lid (1)(2)(6)	θ_{JC}	Rth Junction – Top of lid	4.3	°C/W
Thermal resistance from junction to bottom of balls (1)(2)(6)	θ_{JBb}	Rth Junction - Bottom of balls	6.3	°C/W
Delta temperature Hot spot – temperature from diode (1)(6)			4.7	°C

(1) Thermal resistance (Rth) figures are calculated from hot spot, not from average temperature. These figures are thermal simulation results with nominal case assuming:
- 2.6W power consumption,
- Nominal supplies,
- SSO2 & SYNCO outputs OFF,
- No DDC activated.

(2) No air, pure conduction, no radiation.
(3) Convection according to JEDEC JESD51-1/2/5/6/7/9.
- Still air,
- Horizontal 2s2p board,
- Board size 101.5 x 114.5 mm, 1.6 mm thickness.

(4) 2s2p board.
(5) Ambient temperature specified at 25°C.
(6) Ambient temperature specified at 80°C.

8. THEORY OF OPERATION

The EV10AS940 is a single channel, 10bit, 12.8GSps sampling rate, 33GHz analog bandwidth ADC. The EV10AS940 samples the input signal on a single ended RF input and uses a single ended clock input. No balun is therefore needed in front of the ADC.

The digital data stream is output through a high-speed serial interface, running at up to 12.8Gbps. It uses the ESIstream serial interface protocol. ESIstream is an open license free, high efficiency serial interface protocol based on 62/64b encoding. Its main benefits are ability to have deterministic latency and low hardware overhead easing the FPGA implementation.

The EV10AS940 can be used in a wide range of application thanks to its easy-to-use and versatile features combined with a low power consumption of 2.5W. It is designed for space environment and protected against radiation effects.

The on-chip calibration provides excellent linearity across wide temperature and frequency range. It corrects the gain and offset mismatch between the ADC cores. The on-chip calibration adjusts automatically to the input signal frequency range. It can optionally be turned off.

The EV10AS940 has x4 on-chip NCOs, allowing up to x4 frequency channels. This is particularly useful for multi-band systems. Those systems work over several frequency bands ; they benefit from the 33GHz analog bandwidth (L-Band to Ka-Band) of the EV10AS940. The NCOs frequency can also hop quickly and deterministically thanks to the Fast Frequency Hopping feature. The frequency hops are controlled through high speed dedicated GPIOs.

The EV10AS940 is designed to work in multi-channel systems. Digital fractional digital delays provide options for phase mismatch correction in the RF front end and digital beamforming. The synchronization of multiple EV10AS940 is easy thanks to the ‘Multi-Chip Synchronization’ process. This synchronization process is robust across wide temperature ranges.

8.1.1 Initial start-up procedure

The following section describes the initialization and start-up procedure of the EV10AS940.

8.1.1.1 Ramp-up

These steps are simply dedicated to the circuit stabilization before effective and clean start-up. The SYNC performed during this ramp-up phase acts on the cadencing functions (Timer) to set internal clocks in a known condition and correctly initialize the internal phases, but not on the digital functions because the digital clock is not active yet. This procedure is needed only once after supplies are switched on.

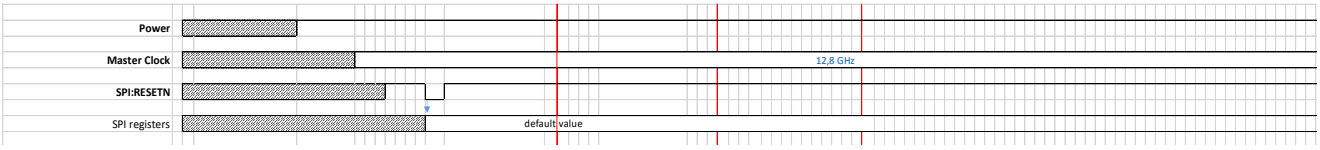
STEP1: ramp-up supply and activate master clock. No precise order is requested for the supplies ramp-up. The clock (Fs=12.8GHz maximum) is applied on the single-ended CML input **CKIN** pin.

1	supplies ramp-up		
1	CKIN	(pin)	12.8GHz clock

STEP2: SPI and registers reset. The reset is performed by the **RESETN** input GPIO pin. After this step, all registers are set to their default values.

2	RESETN	(pin)	active-low state pulse, 50us min

Before passing to the following step, one needs to wait at least 64 sampling clock periods, to ensure that the shift-register generating the SYNCDIG signal is reset to the right value. The digital block contains a state-machine that filters the 64 first samples of SYNCDIG, to avoid false synchronization during this lap of time.



8.1.1.2 External SYNC

This is the default procedure: the SPI register TIMER_SYNC_BY_SPI_ENA (12.2.29) is at '0' by default, meaning that the SYNC signal is expected from the LVDS pins.

STEP3:

- Send SYNC pulse on **SYNCIN/P** pins

3	SYNCIP/SYNCIN	(pins)	pulse

The internal phases will be correctly aligned AND deterministic versus the external SYNC.

8.1.1.3 Internal SYNC

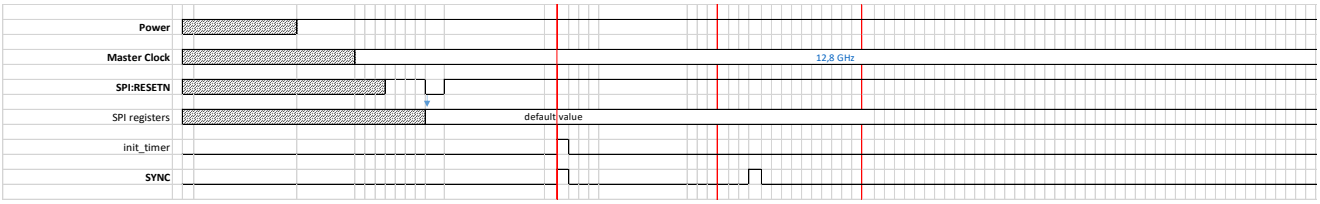
The SYNC can be sent through an SPI instruction

STEP3: First, the SYNC selection mux must be set through the following fields:

- SPI write **TIMER_SYNC_BY_SPI_ENA** = 1 (12.2.29)
- SPI write **TIMER_SYNC_BY_SPI** = 1 (12.2.30)

3	WRITE @ TIMER_SYNC_BY_SPI_ENA	12.2.29		1
3	WRITE @ TIMER_SYNC_BY_SPI	12.2.30		1

The internal phases will be correctly aligned, but not deterministic versus an external reference.



8.1.1.4 Start-up procedure

The previous steps initiated the correct internal sequencing.

STEP4: Even though the digital functions are not correctly started-up after this first SYNC, one needs to start the ESIstream signal generation and send to serial links the PRBS codes:

- SPI write **ESI_CFG/FLASH_ENA** = '1'. (12.2.11)

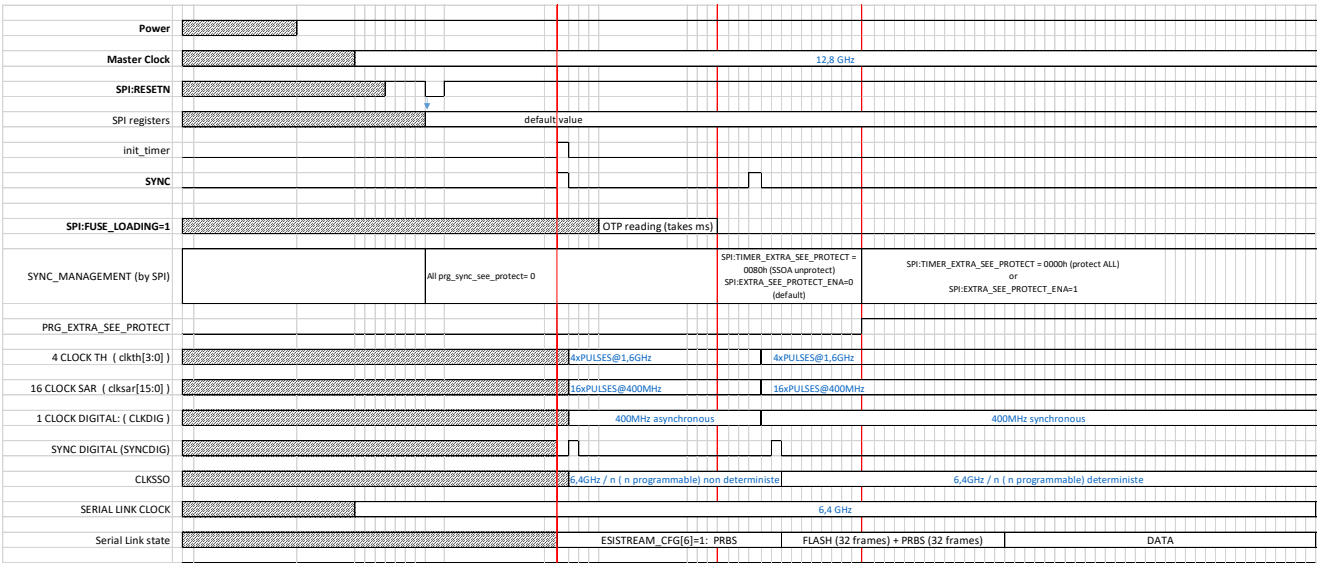
The benefit of starting the emission of HSSL signals is to pre-charge the lines and be ready for the transmission of the useful signals (after the second SYNC). Before this step, the HSSL were sending a (programmable) FLASH code.

STEP5: (optional). A second SYNC will be sent at step 7. By default, this SYNC will resynchronize all the internal clocks including the SSO clock reference for the FPGA. This could be an issue if this clock is used as reference for a PLL. In this case, it is preferable to mask the SYNC sent to the shift-register generating the SSO (and SSOB, if used):

- SPI write **TIMER_SYNC_FINE_DIS/SSOA** (12.2.53) = '1'

STEP6: Send a second SYNC signal to correctly synchronize all the digital functions (now receiving a correct clock). It is recommended to send an external SYNC to definitely make the internal phases deterministic (8.1.1.3), but in some cases an SPI SYNC (see 8.1.1.2) can be sent as well.

4	WRITE @ ESI_CFG/FLASH_ENA	12.2.11		1
5	*wait 10ms*			
6	WRITE @ TIMER_SYNC_FINE_DIS/SSOA (optional)	12.2.53		1
7	SYNCIP/SYNCIN (or internal sync, see 8.1.1.3)	(pins)	pulse	SYNCIP/SYNCIN



8.1.2 On-working start-up procedure

As explained at paragraph 8.1.1, the initial start-up procedure is made complex by the need to both synchronize the clocks and the contents of the shift-registers used to produce the clocks.

Once this ramp-up done, the following product synchronizations are simpler:

STEP1: (optional): **RESETN** to reset register at their default values. If the RESETN is sent, the OTP must be reloaded (SPI read or write FUSE_LOADING, 12.2.3). All the previous (non-default) SPI registers must be re-written.

STEP2: **SYNC** to apply the changed registers (if STEP1) and synchronize the internal control signals. If no reset has been done, one needs to ensure that the SYNC is not disabled: TIMER_SYNC_HSSL_DIS (12.2.5) and/or TIMER_SYNC_FINE_DIS, (12.2.53).

1	RESETN	(pin)	active-low state pulse, 50us min
2	SYNCIP/SYNCIN (or internal sync, see 8.1.1.3)	(pins)	pulse

or

2	WRITE @ TIMER_SYNC_HSSL_DIS/HSSL_PROTECT	12.2.5		0
2	WRITE @ TIMER_SYNC_FINE_DIS/SSOA	12.2.53		1
2	SYNCIP/SYNCIN (or internal sync, see 8.1.1.3)	(pins)	pulse	

8.2 SYNC sampling, delaying and acknowledgement

The SYNC pulse applied on **SYNCIN/P** pins is internally latched with an internal clock at half the sampling frequency (Fs/2). No matter the direction of edges, the first edge is considered. It is then directly sent to **SYNCON/P** for the chaining.

The synchronization system detects the correct reception of the SYNC signal on registers: **TIMER_A_SYNC_FLAG** (12.2.17) and **TIMER_B_SYNC_FLAG** (12.2.22). The flag signal is controlled by the ADC and indicates if the SYNC arrived in a forbidden zone. This register is automatically reset after its reading.

	reg name	reference
	FALL_EDGE_SYNC_FLAG	12.2.17
	FALL_EDGE _SYNC_CLEAR_FLAG	12.2.18
	FALL_EDGE _SYNC_DELAY	12.2.19
	RISE_EDGE_SYNC_FLAG	12.2.22
	RISE_EDGE _SYNC_CLEAR_FLAG	12.2.23
	RISE_EDGE _SYNC_DELAY	12.2.24

The SYNC pulse can be delayed by steps of the 12.8GHz clock, using the SPI register **TIMER_SYNC_SHIFT_FINE** (12.2.27). It is used to add a programmable shift to the internal path of the SYNC signal (between 1 to 16 clock periods). This is used for multi-chip synchronizations.

	reg name	reference
	TIMER_SYNC_SHIFT_FINE	12.2.27
	SYNC_SHIFT_COARSE	12.2.28

8.2.1 Enable SYNC out (for multi-ADC synchronization)

	reg name	reference
	TIMER_SYNCOUT_CFG	12.2.9
	TIMER_SYNC_DELAY	12.2.54

8.2.2 Serial links controls

The register settings for configure the HSSL protocol and data emission are described in chapter 11. We describe here the settings for the physical layer.

	reg name	reference
	SL_CFG	12.2.14
	SL_ROUT	12.2.15
	SL_POWER_ON	12.2.16

8.3 Digital temperature measurement

The EV10AS940 integrates a digital temperature measurement mean in addition to the analog measurement that can be done directly by measuring the temperature diodes.

The TEMP_ENA register (12.2.31) instruction trigs the temperature measurement and ends with the differential measurement available in the corresponding registers, as explained in the following paragraphs.

8.3.1 Temperature reading

Two temperature measures are available: an instantaneous value and an average over the last NBR samples, NBR being set by register TEMP_AVERAGE_NBR (12.2.32). Default is NBR=16. The average measurement is correct after NBR acquisitions.

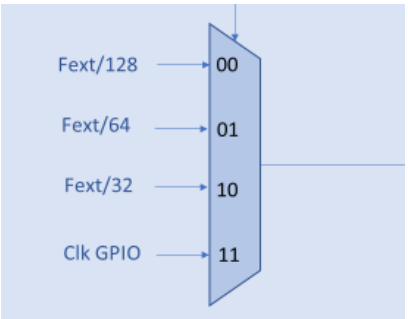
2	WRITE @ ADC_TEMP_ENA (default)	12.2.40		1
2	WRITE @ TEMP_ENA	12.2.31		1
2	*wait 1.84us = 128/Fs*(128+56))*			
2	READ @ TEMP_AVG/AVG_VAL (1)	12.2.34		TEMP_AVG
	READ @ TEMP_AVG/OUT_OF_RANGE (2)			Out-of-range flag
2	READ @ TEMP_INST/INST_VAL (1)	12.2.35		TEMP_INST
	READ @ TEMP_INST/OUT_OF_RANGE (2)			Out-of-range flag

Note:

(1) The temperature format is 2's complement 8.2 (8 integer bits, 2 decimal bits).
(2) If out-of-range flag is raised, the temperature measurement must not be considered.

Both measurements (instantaneous and average) are updated any 128/56/Fs sampling frequency clock periods, when TEMP_ENA=1 (12.2.31).

Note that the temperature sensor is expected to work at a nominal frequency of 100MHz and the working range is [100:200] MHz. This means that when Fs=12.8GHz, this clock must be divided by 128, which is the default value. If the Fs is less than 12.8GHz, the division by 128 makes the temperature sense clock too slow (less than 100MHz). In this case, the division can be changed to 64 and further to 32 (if Fs < 6.4GHz). The selection is made by register TEMP_CLOCK_CFG/CLK_SEL (12.2.33).



The GPIO clock can also be chosen, but this option is not recommended, because the temperature sensor clock would be asynchronous versus the digital clock.

Other temperature settings:

	reg name	reference
	TEMP_AVERAGE_NBR	12.2.32
	TEMP_CLOCK_CFG	12.2.33

8.4 Calibration

EV10AS940 is based on time interleaved ADCs which introduce offset and gain mismatch if left uncalibrated. An on-chip calibration system is used to estimate and compensate the two mismatch sources. Note that timing mismatch and bandwidth unbalance of the interleaved ADCs, are addressed with the analog front-end.

Two types of calibration are available in the EV10AS940:

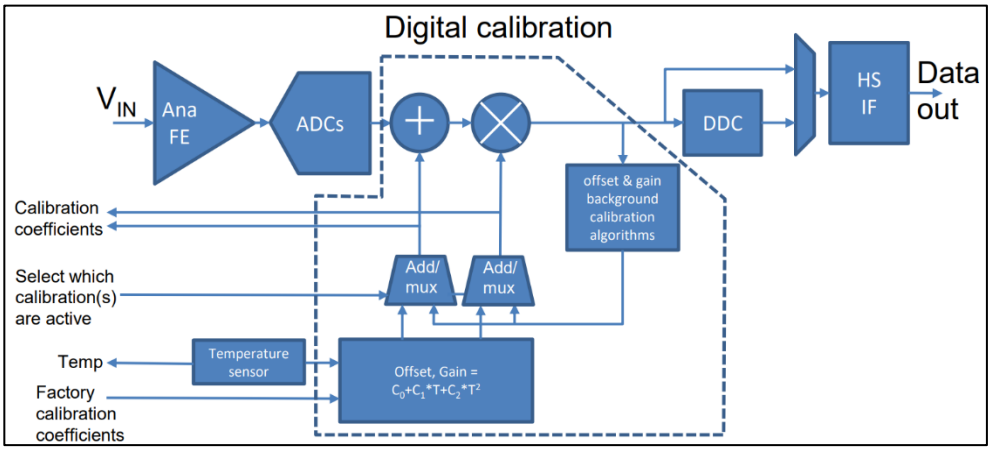


Figure 8 : Calibration functional diagram.

- The **background** calibration is based on a continuous calculation that can run at the same time as the component is converting input data. For each one of the interleaved ADCs, the average and RMS values of the output are estimated on a sliding time window. These values are compared to the global average (for offset) and RMS (for gain), and the deviations are extracted by subtraction and division respectively.
  The only conditions are that:
  - An input signal MUST be present, otherwise the gain cannot be estimated
  - The input signal can be a sinewave, a modulated signal, or a wide-band signal. If sinewave, its frequency MUST NOT be a multiple of Fs/64, otherwise the signal at the conversion core level is interpreted as offset and the local calculations are misleading (1).

  The drawback of this calibration, apart the conditions on the input signal, is that the average and RMS calculations are power consuming. This calibration can be run periodically to save power.
  Note that the coefficient stored in the OTP memory for the factory calibration can be used as starting point for the back-ground calibration.
  The advantage of the back-ground calibration is that it tracks the circuit evolution versus time (aging).

- In some applications, the back-ground calibration cannot be used, for power-saving reasons or because the conditions on the input signal cannot be warrantied. In this case, one can use the calibration coefficients stored in the OTP memory during **factory calibration** procedure.

Note that the two calibrations can run separately or together. By default, only the factory calibration is activated.

	reg name	reference	
	CAL_OFFSET_ENA	12.2.36	BCKGND_UPDATE_ENA: Enable background offset calibration update (default disabled) LOCAL_UPDATE_ENA: Enable factory local offset calibration update (default enabled) GLOBAL_UPDATE_ENA: Enable factory global offset calibration update (default enabled) BCKGND_ENA: Select background offset calibration source (default disabled) LOCAL_ENA: Select factory local offset calibration source (default enabled) GLOBAL_ENA: Select factory global offset calibration source (default enabled)
	CAL_GAIN_ENA	12.2.37	BCKGND_UPDATE_ENA: Enable background gain calibration update (default disabled) LOCAL_UPDATE_ENA: Enable factory local gain calibration update (default enabled) GLOBAL_UPDATE_ENA: Enable factory global gain calibration update (default enabled) BCKGND_ENA: Select background gain calibration source (default disabled) LOCAL_ENA: Select factory local gain calibration source (default enabled) GLOBAL_ENA: Select factory global gain calibration source (default enabled)

By default, the factory calibration (both local and global) only is enabled, because the background calibration expects an input signal that cannot be warrantied for all user conditions.

10. SERIAL PERIPHERAL INTERFACE (SPI)

The digital interface will be a standard SPI with:

- 16 bits for the address A[15] to A[0] including a R/W bit (A[15] = R/W, with A[15] being the MSB),
- 16 bits of data D[15] to D[0] with D[15] the MSB.

5 signals are required:

- RSTN for the SPI Reset (Active Low),
- SCLK for the SPI Clock,
- CSN for the Chip Select (Active Low),
- MISO for the Master In Slave Out SPI Output,
- MOSI for the Master Out Slave In SPI Input.

The MOSI sequence should start with one R/W bit (A[15])

- R/W = 0 is a read command
- R/W = 1 is a write command

10.1 SPI logic Compatibility

Digital SPI CMOS input levels have logic compatibility with voltage level between 1.2V and 1.8V.
Digital SPI CMOS output levels have logic compatibility with voltage level between 1.2V and 1.8V.
Digital SPI CMOS input and output levels must have the same voltage compatibility level.

10.2 SPI Read / Write Commands

All SPI registers must be addressed with 16-bit address followed by 16-bit data.
See section Table 12 for SPI timing characteristics.

10.2.1 Write command

Writing instruction on a 16-bit register (R/W = 1)

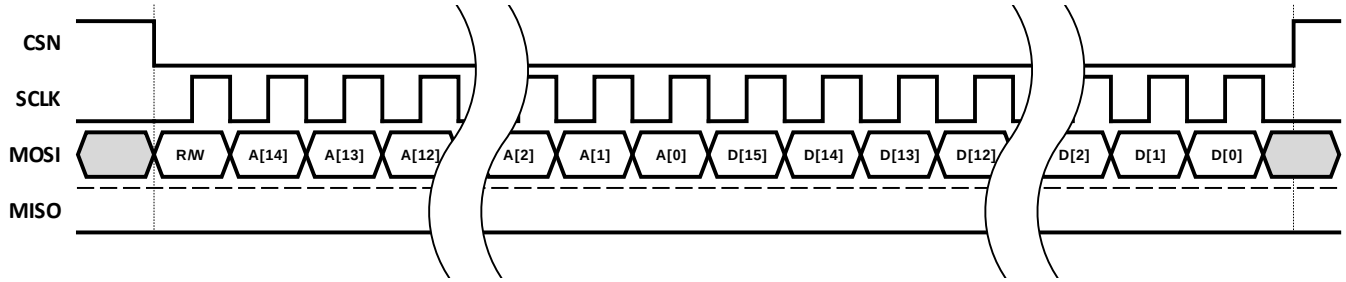


Figure 9 : SPI Write Sequence.

10.2.2 Read command

Reading instruction on a 16-bit register (R/W = 0):

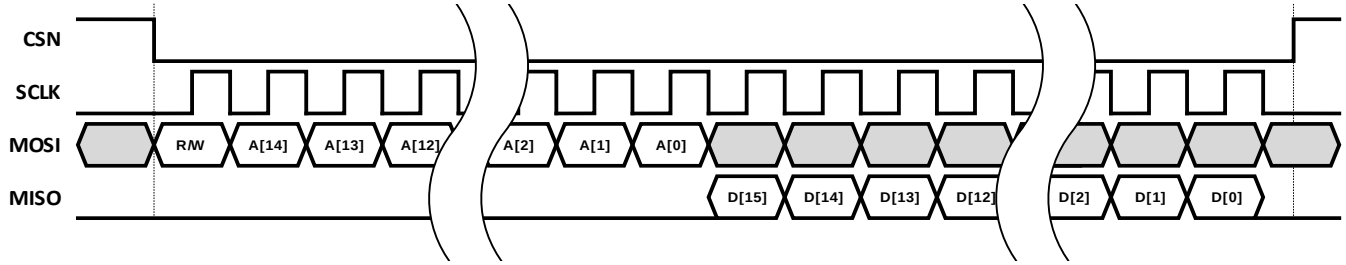


Figure 10 : SPI Read sequence.

11. ESISTREAM SERIAL DATA INTERFACE

11.1 ESIstream 62B/64B protocol

11.1.1 Overview

ESIstream provides an efficient High-Speed serial interface based on a 62B/64B encoding using a Linear Feedback Shift Register (LFSR) scrambling unit, a Disparity Bit (DB) to ensure deterministic DC balance transmission and a toggling bit, the Clock Bit (CB), to enable synchronization monitoring.
It is **license-free** and supports serial communication between FPGAs and High-Speed data converters.

An ESIstream system is made up of the following elements.

- A transmitter (TX) can be an ADC or any Logic Devices (LD) such as a FPGA or an ASIC.
- A receiver (RX) can be a DAC or any Logic Devices such as a FPGA or an ASIC.
- High-Speed Serial Lanes (HSSLs) to transmit serial data.
- A synchronization signal (sync) used to initialize the communication and synchronize the transmitter and receiver.

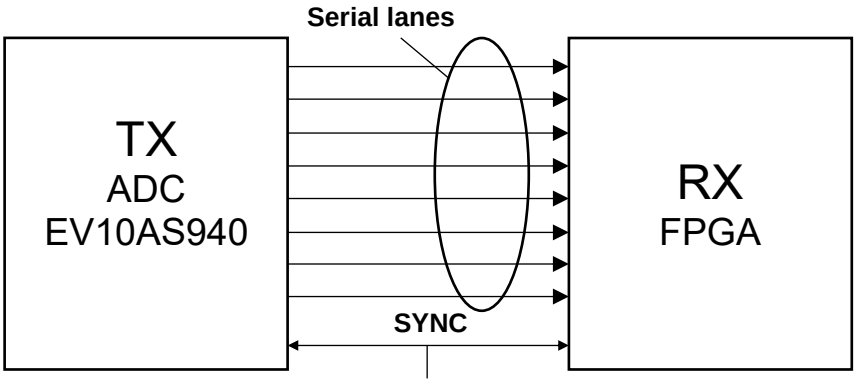


Figure 11: Basic ESIstream system between an ADC EV10AS940 and a FPGA

11.1.2 ESIstream TX and RX architecture

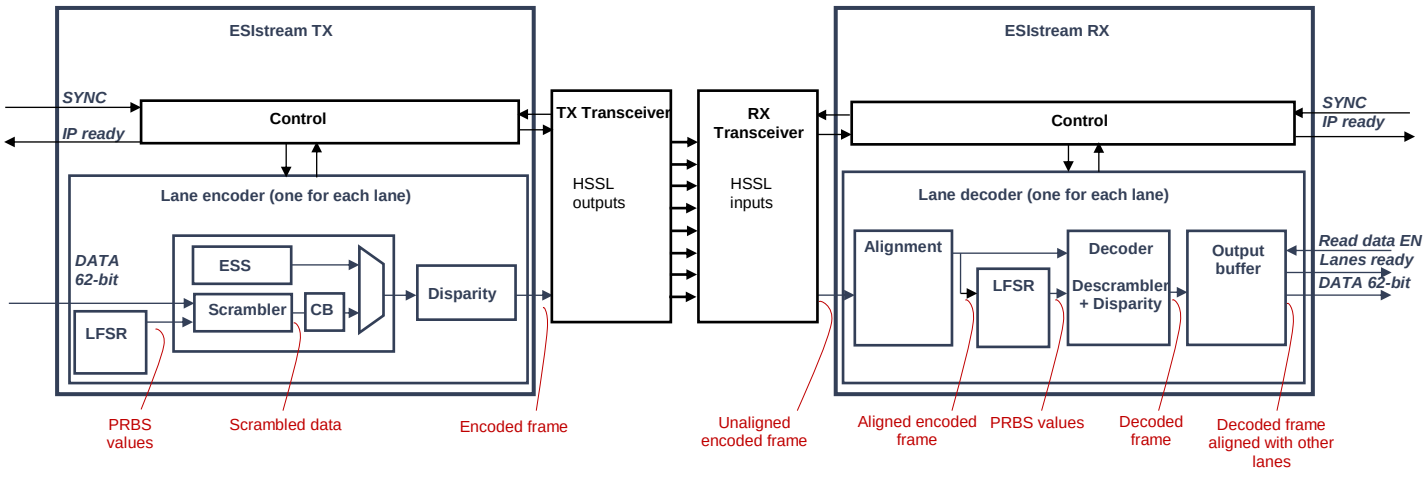


Figure 12: ESIstream TX and RX architecture overview

Different stages of encoding/decoding are implemented to manage the limitations of a serial interface.

An AC coupled interface requires a DC balance, otherwise the AC coupling link will tend to drift and the received data will be corrupted.

The Clock Data Recovery (CDR) in the RX transceiver stage, which usually contains a Phased Locked Loop (PLL), specifies a maximum number of Unit Interval (UI, time to send a bit through the serial lane) without transition on the serial lane, the maximum run length. Otherwise, the PLL can lose its lock.

11.1.3 ESIstream Frame

An ESIstream 62B/64B frame is 64-bit wide. The frame is **transmitted**, **LSB first**, between the transmitter and the receiver.
62-bit of useful data are scrambled and then **2-bit of header** are concatenated to create the **64-bit** ESIstream frame. The **header** is composed of:

- The Clock Bit (CB), which is toggling between each consecutive frame sent through a single serial lane. The Clock bit can be used to monitor the synchronization of a single lane.
  The Clock Bit can be disabled and set to 1 to reduce the maximum run length to 64.
- The Disparity Bit (DB), which is the result of a calculation, the disparity processing, done on the 62-bit data and on the Clock Bit.

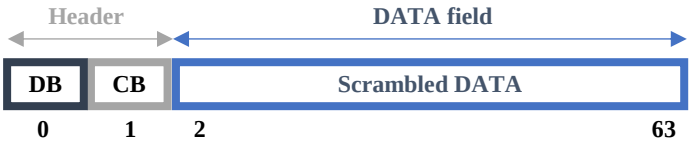


Figure 13: ESIstream 62/64b encoded frame

These different stages of encoding are realized to manage the limitations of a serial interface. First, an AC coupled interface between transmitter and receiver implies that the transmission be DC balance, otherwise the AC coupling capacitor will drift and the received data will be corrupted. Secondly the CDR in the reception stage usually contains a PLL. This means that there must be transitions in the transmission otherwise this PLL will lose its lock.

- When the Clock bit is toggling, the scrambling, the Clock bit and the disparity processing ensure a deterministic transmission with a DC balance between **+/- 64** and a max run length of the transmission of **128.**
- When the Clock bit is set to 1, the scrambling, the Clock bit and the disparity processing ensure a deterministic transmission with a DC balance between **+/- 64** and a max run length of the transmission of **64.**

Most FPGA CDR can work with a maximum run length of 200 and above.

11.1.4 ESIstream Scrambling

Scrambling ensures a statistical DC balanced transmission. It also statistically ensures that there are transitions in serial data stream.
ESIstream uses an additive scrambling to avoid error propagation in case of a single bit error. A Linear Feedback Shift Register (LSFR) generates a Pseudo Random Binary Sequence (PRBS) and is based on a Fibonacci architecture using polynomial $X^{31}+X^{28}+1$. It has a length of $2^{31} - 1$.

ESIstream LFSR is characterized by the following equations:

X30 = X27 xor X30
X29 = X26 xor X29
X28 = X25 xor X28
X27 = X24 xor X27
X26 = X23 xor X26
X25 = X22 xor X25
X24 = X21 xor X24
X23 = X20 xor X23
X22 = X19 xor X22
X21 = X18 xor X21
X20 = X17 xor X20
X19 = X16 xor X19
X18 = X15 xor X18
X17 = X14 xor X17
X16 = X13 xor X16
X15 = X12 xor X15
X14 = X11 xor X14
X13 = X10 xor X13

X12 = X9 xor X12
X11 = X8 xor X11
X10 = X7 xor X10
X9 = X6 xor X9
X8 = X5 xor X8
X7 = X4 xor X7
X6 = X3 xor X6
X5 = X2 xor X5
X4 = X1 xor X4
X3 = X0 xor X3
X2 = X27 xor X30 xor X2
X1 = X26 xor X29 xor X1
X0 = X25 xor X28 xor X0

PRBS is applied to data with a bitwise XOR binary operation:

DATA[61:0] **XOR** (PRBS2[61:0] & PRBS1[61:0]) = DATA_SCRAMBLED[61:0]

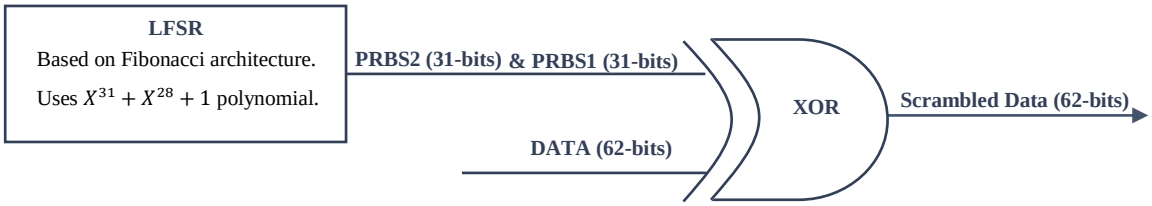


Figure 14: Scrambling principle, bitwise XOR binary operation

In case of a multi-lane interface and to reduce correlation between lanes, each lane should have different initial values for scrambling units.

11.1.5 ESIstream Encoding

Scrambled data (62-bit) are encoded into a 64-bit frame adding two header bits, the Clock Bit (CB) and the Disparity Bit (DB).

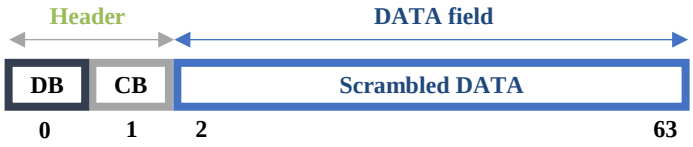


Figure 15: ESIstream 62/64b encoded frame

11.1.5.1 Clock Bit (CB)

On each serial lane, Clock Bit (CB) toggles at every ESIstream frame sent through one serial lane.
The receiver uses Clock Bit to monitor the link synchronization. If the receiver does not detect that the Clock Bit is toggling properly, then it can state that the link is not synchronous or has lost its synchronization and restart the synchronization process.

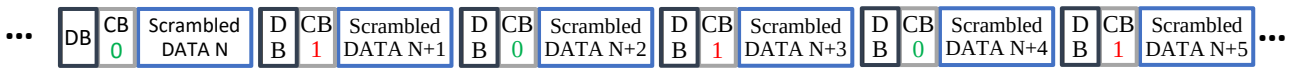


Figure 16: Clock Bit toggling properly on one serial lane.

11.1.5.2 ESIstream Disparity Bit (DB)

The Disparity Bit ensures deterministically advantages brought statistically by scrambling process.

Even with scrambling process, a large running disparity can still occur with very low probability and could produce excessive eye shifts. These eye shifts could be balanced by a more complicated equalization stage in the receiver if the running disparity was still limited. However, a PRBS does not bind the running disparity deterministically, thus the data could be corrupted on the reception end, and it could eventually cause the PLL in the CDR to lose its lock. The implementation of the Disparity Bit process prevents from this eventuality.

The transmitter constantly monitors the disparity of the transmission.
For each frame, the running disparity is calculated, and 2 cases can occur:

- The running disparity of the transmission **does not** increase above ±64 (+64 and -64 included). In this case, the disparity bit is set to '0' and the 63 bits composed of the scrambled data and of the Clock Bit are transmitted as is.
- The running disparity of the transmission **does** increase above ±64 (+64 and -64 excluded). In this case, the 63 bits composed of the scrambled data and of the Clock Bit are inverted and the disparity bit is set to '1'.

In normal operating mode, the receiver will check the disparity bit first.
If the disparity bit is high, then the received data are inverted (including the Clock Bit), then the data are descrambled.
If the disparity bit is low, then data are descrambled only.

11.1.6 ESIstream 62/64b Synchronization Sequence (ESS)

Each serial lane must be synchronized to realign frames sent by transmitter at receiver side and to initialize receiver scrambler to be synchronized with transmitter scrambler.

Synchronization is triggered on synchronization signal (SYNC) sent to the receiver and to the transmitter.
The transmitter generates the ESS when receiving the SYNC signal.
The receiver must receive SYNC signal prior to receive the ESIstream 62/64b Synchronization Sequence (**ESS**).

The ESS is composed of two parts:

- The Frame Alignment Sequence (**FAS**) is composed of 32 frames of a 64-bit programmable COMMA, 0x00FFFF0000FFFF00 or 0xACF0FF00FFFF0000 (default). This sequence bypasses the scrambling, the Clock Bit and the Disparity Bit processing (the sequence is DC balanced). This alignment pattern (COMMA or FLASH pattern) is used by the receiver to align its data on the transmitter output data.

- The PRBS Alignment Sequence (**PAS**), 32 additional frames containing the scrambling PRBS alone. These frames contain 62 bits of the PRBS plus the Clock Bit and the Disparity Bit. These frames go through the disparity processing, as the PRBS value will start to impact the running disparity of the transmission.

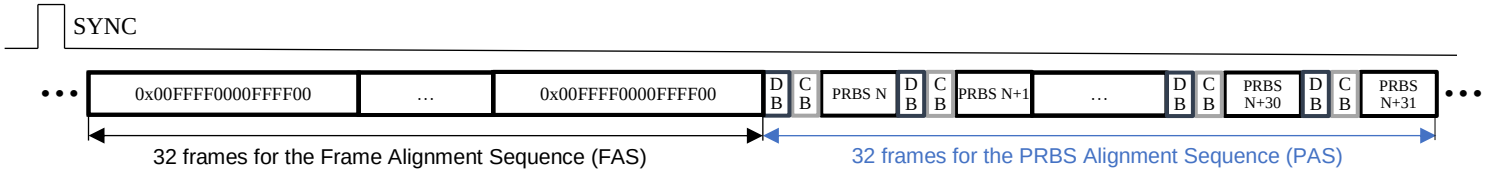


Figure 17: ESIstream Synchronization Sequence (ESS) with COMMA = 0x00FFFF0000FFFF00

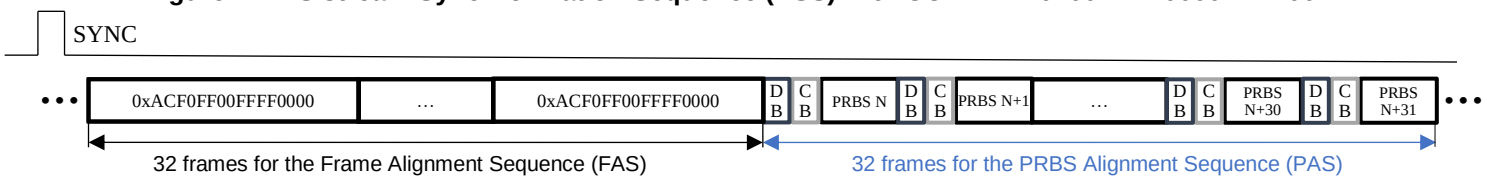


Figure 18: ESIstream Synchronization Sequence (ESS) with COMMA = 0xACF0FF00FFFF0000

When transmitter (**TX**) receives the SYNC, the TX sends the FAS bypassing the scrambling and disparity processing (the sequence is DC balanced). After the FAS, the transmitter sends the PAS.

Figure 19: PRBS frames sent during the PRBS Alignment Sequence (PAS).

The receiver will detect the transition from the FAS to the PAS. The PRBS is reset by the transmitter when receiving the SYNC to avoid the first frame of the PRBS initialization being the COMMA; this to ensure that passive detection is precise to the frame.
The receiver will determine its PRBS initial value after receiving 1 valid frame of the PAS. After that, the synchronization of the link is complete.

11.1.7 FPGA Design example

For FPGA design examples, contact us at GRE-HOTLINE-BDC@Teledyne.com

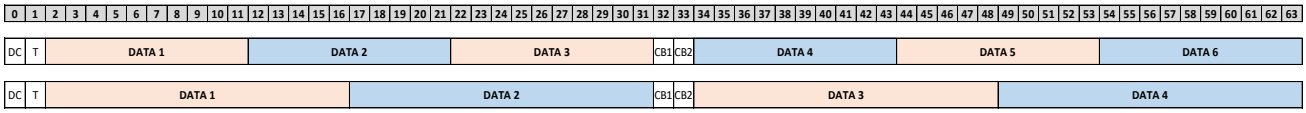
11.2 EV10AS940 ESIstream Frame Organization

The EV10AS940 uses the ESIstream protocol for the serial data on the serial links. The frame size is 64 bits organized as follow:

- 60 bits for DATA
- 2 control bits CB1 and CB2
- 1 Toggle bit, enabled by ESI_CFG/TOGGLE_ENA (12.2.11)
- 1 DC-balance bit, enabled by ESI_CFG/DC_BAL_ENA and selected by /CB_SEL (12.2.11)

There are 2 possible ESIstream frames:

- frame with 10 bits DATA when DDC is bypassed (real data mode)
- frame with 15 bits DATA when DDC is activated (I/Q data mode)



- DC : DC balance bit (‘1’: data must be reversed, ‘0’ non action non data)
- CB : Toggle bit, toggles every frame
- CB1 : User defined Control Bit 1. Example of use : check PRBS error at Rx
- CB2 : User defined Control Bit 2. Example of use : identify empty frames for high decimation ratios

The PRBS is the **X31 + X28 + 1**. Note that the PRBS on applied on bits 2 to 63.

The main ESIstream settings are available on registers:

	reg name	reference
	ESI_CFG	12.2.11
	SL_TEST_MODE_CFG	12.2.12
	SL_INV_DATA	12.2.52

11.2.1 Data in real mode (10 bit)

In the 64-bit word, six 10-bit data fits, plus the four protocol-bit (DC-balance, Toggle, ant the two control bits CB1 and CB2). Note that the 11th HSSL on not filled.

DECIMATION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	HSSL number	Total HSSL number
0	DC	T	10													21																	0	CB1	CB2	42													53																	0	10	11
	DC	T	9													20																	31	CB1	CB2	41													52																	63	9	
	DC	T	8													19																	30	CB1	CB2	40													51																	62	8	
	DC	T	7													18																	29	CB1	CB2	39													50																	61	7	
	DC	T	6													17																	28	CB1	CB2	38													49																	60	6	
	DC	T	5													16																	27	CB1	CB2	37													48																	59	5	
	DC	T	4													15																	26	CB1	CB2	36													47																	58	4	
	DC	T	3													14																	25	CB1	CB2	35													46																	57	3	
	DC	T	2													13																	24	CB1	CB2	34													45																	56	2	
	DC	T	1													12																	23	CB1	CB2	33													44																	55	1	
	DC	T	0													11																	22	CB1	CB2	32													43																	54	0	

11.2.2 Data in decimation mode (15 bit)

Considering that one bit of resolution adds when the bandwidth is decimated by 4, and starting from a 10-bit resolution, the 15-bit coding is necessary only when the signal is decimated by 4^5=1024.
The theoretical coding is listed in the following table:

Decimation	Nb bit coding	
	theoretical	used
none	10	10
2	11	15
4	11	15
8	12	15

16	12	15
32	13	15
64	13	15
128	14	15
256	14	15
512	15	15
1024	15	15

To avoid a too complex coding protocol, the 15-bit coding is used for all the decimations.

The following table summarizes the links distribution for the coarse-channel decimations (/2 to /16):

DECIMATION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	HSSL number	Total HSSL number
2	DC	T	I7															Q7															CB1	CB2	I15															Q15																7	8
	DC	T	I6															Q6															CB1	CB2	I14															Q14																6	
	DC	T	I5															Q5															CB1	CB2	I13															Q13																5	
	DC	T	I4															Q4															CB1	CB2	I12															Q12																4	
	DC	T	I3															Q3															CB1	CB2	I11															Q11																3	
	DC	T	I2															Q2															CB1	CB2	I10															Q10																2	
	DC	T	I1															Q1															CB1	CB2	I9															Q9																1	
	DC	T	I0															Q0															CB1	CB2	I8															Q8																0	
4	DC	T	I3															Q3															CB1	CB2	I7															Q7																3	4
	DC	T	I2															Q2															CB1	CB2	I6															Q6																2	
	DC	T	I1															Q1															CB1	CB2	I5															Q5																1	
	DC	T	I0															Q0															CB1	CB2	I4															Q4																0	
8	DC	T	I1															Q1															CB1	CB2	I3															Q3																1	2
	DC	T	I0															Q0															CB1	CB2	I2															Q2																0	
16	DC	T	I0															Q0															CB1	CB2	I1															Q1																0	1

The fine-channels decimations (/16 to /1024) can be performed over one to four channels. The following table summarizes the data distributions over the HSSLs:

DECIMATION	total CHANNELS	CHANNEL nbr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	HSSL number
16	1	1	DC	T	I0															Q0															CB1	CB2	I1															Q1																0
	2	2	DC	T	I0															Q0															CB1	CB2	I1															Q1																1
		1	DC	T	I0															Q0															CB1	CB2	I1															Q1																0
	4	4	DC	T	I0															Q0															CB1	CB2	I1															Q1																3
		3	DC	T	I0															Q0															CB1	CB2	I1															Q1																2
		2	DC	T	I0															Q0															CB1	CB2	I1															Q1																1
		1	DC	T	I0															Q0															CB1	CB2	I1															Q1																0
32	1	1	DC	T	I															Q															CB1	CB2	empty															empty																0
	2	1 & 2	DC	T	I (channel N°1)															Q (channel N°1)															CB1	CB2	I (channel N°2)															Q (channel N°2)																0
	4	3 & 4	DC	T	I (channel N°3)															Q (channel N°3)															CB1	CB2	I (channel N°4)															Q (channel N°4)																1
		1 & 2	DC	T	I (channel N°1)															Q (channel N°1)															CB1	CB2	I (channel N°2)															Q (channel N°2)																0
64	1	1	DC	T	I															Q															CB1	1	empty															empty																0
			DC	T	empty																														CB1	0	empty																													
	2	1 & 2	DC	T	I (channel N°1)															Q (channel N°1)															CB1	1	I (channel N°2)															Q (channel N°2)																
			DC	T	empty																														CB1	0	empty																													
	4	3 & 4	DC	T=0	I (channel N°3)															Q (channel N°3)															CB1	1	I (channel N°4)															Q (channel N°4)																
		1 & 2	DC	T=1	I (channel N°1)															Q (channel N°1)															CB1	1	I (channel N°2)															Q (channel N°2)																
>128	1	1	DC	T	I															Q															CB1	1	empty															empty																0
			DC	T	empty																														CB1	0	empty																													
	2	1 & 2	DC	T	I (channel N°1)															Q (channel N°1)															CB1	1	I (channel N°2)															Q (channel N°2)																
			DC	T	empty																														CB1	0	empty																													
	4	3 & 4	DC	T=0	I (channel N°3)															Q (channel N°3)															CB1	1	I (channel N°4)															Q (channel N°4)																
		1 & 2	DC	T=1	I (channel N°1)															Q (channel N°1)															CB1	1	I (channel N°2)															Q (channel N°2)																
		empty	DC	T	empty																														CB1	0	empty																													

The decimation by 64 is the first where two different information need to be inserted in the frame, because a frame can contain channels 1&2 (Toggle=1), channels 3&4 (Toggle=0), or can be empty (CB2=0).
But these three frame states never arise all together for a given number of channels:

- if the transmitted channels are one or two, only empty/full frame occur
- if channels are four, frame are always full and only the channel identity (1&2 or 3&4) need to be informed

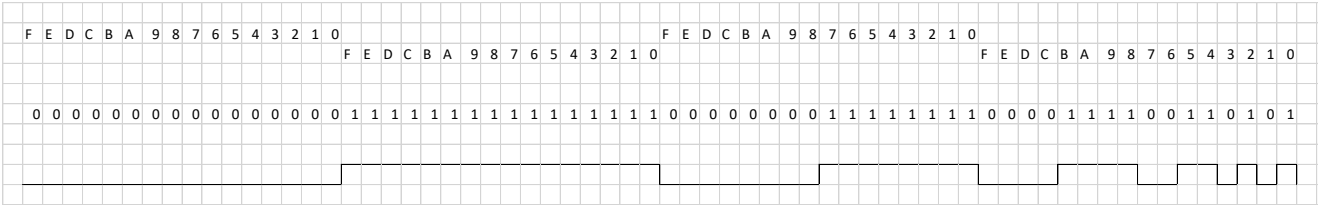
For this reason, the use of two bits to identify the frame states is redundant. On the other hand, this coding becomes essential for decimations of 128 or greater and four channels are active: in this case the three frame state states (empty, channels 1&2, channels 3&4) can occur.
For consistency, the coding of the emitted data in decimation by 64 is then identical (by default) to the coding of the decimation by 128 and greater, even if this is somehow redundant.

Through register SL_TEST_MODE_CFG/TESTER_CB2_TRUE =1 (12.2.12), it is possible to choose a more compact coding, where the Toggle bit is used to identify empty/full frame when the transmitted channels are one or two and is used to identify the channels when the transmitted channels are four:

DECIMATION	total CHANNELS	CHANNEL nbr	0	1	2 … 31	32	33	34 … 63	HSSL number
64 compact	1	1	DC	T=1	I … Q	CB1	CB2	empty … empty	0
			DC	T=0	empty	CB1	CB2	empty	
	2	1 & 2	DC	T=1	I (channel N°1) … Q (channel N°1)	CB1	CB2	I (channel N°2) … Q (channel N°2)	
			DC	T=0	empty	CB1	CB2	empty	
	4	3 & 4	DC	T=0	I (channel N°3) … Q (channel N°3)	CB1	CB2	I (channel N°4) … Q (channel N°4)	
		1 & 2	DC	T=1	I (channel N°1) … Q (channel N°1)	CB1	CB2	I (channel N°2) … Q (channel N°2)	

11.2.3 Flash behavior

The default Flash code is ACF0 FF00 FFFF 0000, corresponding to the following output sequence:



By default, the Flash word is read from right to left (LSB first). This convention can be inverted by setting ESI_CFG/LSB_FIRST = 0 (12.2.11).

	reg name	reference
	FLASH_MOTIF1_15_0	12.2.51
	FLASH_MOTIF1_31_16	
	FLASH_MOTIF1_47_32	
	FLASH_MOTIF1_63_48	

11.2.4 Debug modes

Different test modes are available to debug the links, all together or individually. A 64-bit sequence can be forced, or different ramp signals:

	reg name	reference	fields
	SL_TEST_MODE_CFG	12.2.12	FORCE ENA: force HSSL to a repeated sequence of 64bits. The sequence value is set by SL_FORCE_VALUE_X_X registers (12.2.13).
			RAMP_MODE_SEL 101: 1 ramp 15 bits for 1 SL (1 ramp for 1 SL, the same ramp on all SL) 011: 1 ramp 10 bits for 1 SL (1 ramp for 1 SL, the same ramp on all SL) 001: 1 ramp spreads on x serial links (x depends on the functional mode) => 11 SL for decimation by 0 => 8 SL for decimation by 4 => 4 SL for decimation by 8 => 2 SL for decimation by 16 => 1 SL for decimation by 32 and more 000: test mode ramp disabled

	SL_FORCE_VALUE_15_0	12.2.13	constant value forced on all serial link. The 16 bits are forced at [15:0] position
	SL_FORCE_VALUE_31_16		constant value forced on all serial link. The 16 bits are forced at [31:16] position
	SL_FORCE_VALUE_47_32		constant value forced on all serial link. The 16 bits are forced at [47:32] position
	SL_FORCE_VALUE_63_48		constant value forced on all serial link. The 16 bits are forced at [63:48] position

Forced mode has priority on Ramp mode.

Setting SL_TEST_MODE_CFG/RAMP_MODE_SEL= ‘011’ or ‘101’ generates a 10 or 15-bits ramp identical on all the HSSLs:

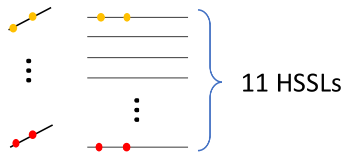


Figure 20 : Repeated ramps.

The 10-bits ramp :

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	LIEN SERIE NUMERO

DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	10
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	9
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	8
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	7
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	6
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	5
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	4
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	3
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	2
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	1
DC	T	n	n+1	n+2	CB1	CB2	n+3	n+4	n+5	0

The 15-bits ramp :

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	LIEN SERIE NUMERO

DC	T	n	n+1	CB1	CB2	n+2	n+3	10
DC	T	n	n+1	CB1	CB2	n+2	n+3	9
DC	T	n	n+1	CB1	CB2	n+2	n+3	8
DC	T	n	n+1	CB1	CB2	n+2	n+3	7
DC	T	n	n+1	CB1	CB2	n+2	n+3	6
DC	T	n	n+1	CB1	CB2	n+2	n+3	5
DC	T	n	n+1	CB1	CB2	n+2	n+3	4
DC	T	n	n+1	CB1	CB2	n+2	n+3	3
DC	T	n	n+1	CB1	CB2	n+2	n+3	2
DC	T	n	n+1	CB1	CB2	n+2	n+3	1
DC	T	n	n+1	CB1	CB2	n+2	n+3	0

Setting SL_TEST_MODE_CFG/RAMP_MODE_SEL= ‘001’generates a ramp distributed on the number of HSSL corresponding to the selected decimation factor:

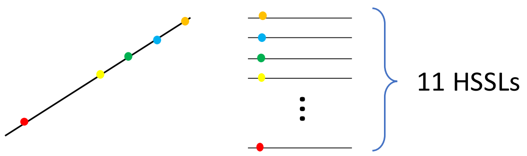


Figure 21 : Distributed ramps.

Distributed ramp for non-decimated HSSL (10-bits):

DC	T	10	21	0	CB1	CB2	42	53	0	10
DC	T	9	20	31	CB1	CB2	41	52	63	9
DC	T	8	19	30	CB1	CB2	40	51	62	8
DC	T	7	18	29	CB1	CB2	39	50	61	7
DC	T	6	17	28	CB1	CB2	38	49	60	6
DC	T	5	16	27	CB1	CB2	37	48	59	5
DC	T	4	15	26	CB1	CB2	36	47	58	4
DC	T	3	14	25	CB1	CB2	35	46	57	3
DC	T	2	13	24	CB1	CB2	34	45	56	2
DC	T	1	12	23	CB1	CB2	33	44	55	1
DC	T	0	11	22	CB1	CB2	32	43	54	0

Distributed ramp for /2 decimated HSSL (15-bits):

DC	T	I7 = n+14	Q7 = n+15	CB1	CB2	I15 = n+30	Q15 = n+31	7
DC	T	I6 = n+12	Q6 = n+13	CB1	CB2	I14 = n+28	Q14 = n+29	6
DC	T	I5 = n+10	Q5 = n+11	CB1	CB2	I13 = n+26	Q13 = n+27	5
DC	T	I4 = n+8	Q4 = n+9	CB1	CB2	I12 = n+24	Q12 = n+25	4
DC	T	I3 = n+6	Q3 = n+7	CB1	CB2	I11 = n+22	Q11 = n+23	3
DC	T	I2 = n+4	Q2 = n+5	CB1	CB2	I10 = n+20	Q10 = n+21	2
DC	T	I1 = n+2	Q1 = n+3	CB1	CB2	I9 = n+18	Q9 = n+19	1
DC	T	I0 = n	Q0 = n+1	CB1	CB2	I8 = n+16	Q8 = n+17	0

Distributed ramp for /4 decimated HSSL (15-bits):

DC	T	I3 = n+6	Q3 = n+7	CB1	CB2	I11 = n+22	Q11 = n+23	3
DC	T	I2 = n+4	Q2 = n+5	CB1	CB2	I10 = n+20	Q10 = n+21	2
DC	T	I1 = n+2	Q1 = n+3	CB1	CB2	I9 = n+18	Q9 = n+19	1
DC	T	I0 = n	Q0 = n+1	CB1	CB2	I8 = n+16	Q8 = n+17	0

Distributed ramp for /8 decimated HSSL (15-bits):

DC	T	I1 = n+2	Q1 = n+3	CB1	CB2	I3 = n+6	Q3 = n+7	1
DC	T	I0 = n	Q0 = n+1	CB1	CB2	I2 = n+4	Q2 = n+5	0

For decimations over 16, the distributed ramp (over one only HSSL) becomes identical to the ‘101’ mode: 15-bits ramp identical on all HSSL.

12. REGISTER MAP

12.1 Register Summary

Address	Reset	Acronym	Description	Section
0x0001	0x0000	CHIP_ID	Chip ID number	12.2.1
0x0002	0x0000	SERIAL_NUMBER	Serial number	12.2.2
0x0003	0x0000	FUSE_LOADING	NOT AVAILABLE	12.2.3
0x0004	0x0000	FUSE_STATUS	NOT AVAILABLE	12.2.4
0x0005	0x0000	TIMER_SYNC_HSSL_DIS	HSSL protect against SET events	12.2.5
0x0006	0x0001	TIMER_SSO_CFG	SSO clocks enable	12.2.6
0x0007	0x0000	GPIO_OUT_CFG	Frequency Hopping output clock enable	12.2.7
0x0008	0x0020	TH_CFG	Analog Front-End configuration	12.2.8
0x0009	0x0000	TIMER_SYNCOUT_CFG	LVDS SYNC output enable	12.2.9
0x000C	0x0000	DDC_CH_POWER_ENA	DDC fine channels enable	12.2.10
0x000E	0x001F	ESI_CFG	ESIstream configuration	12.2.11
0x000F	0x0020	SL_TEST_MODE_CFG	HSSL debug modes	12.2.12
0x0010	0x0001	SL_FORCE_VALUE_15_0	HSSL repeated sequence in Force mode	12.2.13
0x0011	0x0002	SL_FORCE_VALUE_31_16		
0x0012	0x0003	SL_FORCE_VALUE_47_32		
0x0013	0x0004	SL_FORCE_VALUE_63_33		
0x0015	0x0001	SL_CFG	HSSL output buffer drive	12.2.14
0x0016	0x0001	SL_ROUT	HSSL output buffer impedance	12.2.15
0x0017	0x07FF	SL_POWER_ON	HSSL output buffer enable	12.2.16
0x0040	0x0000	FALL_EDGE_SYNC_FLAG	SYNC correctly latched on falling edge	12.2.17
0x0041	0x0000	FALL_EDGE _SYNC_CLEAR_FLAG	Clear previous SYNC flag	12.2.18
0x0042	0x0000	FALL_EDGE _SYNC_DELAY	Delay on SYNC for falling edge latch	12.2.19
0x0043	0x0000	SSO_DIV2	Extra SSO divide by 2	12.2.20
0x0044	0x00FF	SSO_INIT	SSO shape (16 Fs periods)	12.2.21
0x004B	0x0000	RISE EDGE_SYNC_FLAG	SYNC correctly latched on rising edge	12.2.22
0x004C	0x0000	RISE EDGE_SYNC_CLEAR_FLAG	Clear previous SYNC flag	12.2.23
0x004D	0x0000	RISE EDGE_SYNC_DELAY	Delay on SYNC for rising edge latch	12.2.24
0x004E	0x0000	SSO2_DIV2	Extra SSO2 divide by 2	12.2.25
0x004F	0x00FF	SSO2_INIT	SSO2 shape (16 Fs periods)	12.2.26
0x0058	0x0000	SYNC_SHIFT_FINE	SYNC delay for multi-synchronization (Fs steps)	12.2.27
0x0060	0x0040	SYNC_SHIFT_COARSE	SYNC delay for multi- synchronization (Fdig steps)	12.2.28
0x0082	0x0000	TIMER_SYNC_BY_SPI_ENA	Enable SYNC signal by SPI	12.2.29
0x0083	0x0000	TIMER_SYNC_BY_SPI	SYNC signal by SPI	12.2.30
0x0100	0x0000	TEMP_ENA	Temperature monitoring enable	12.2.31
0x0102	0x0008	TEMP_AVERAGE_NBR	Number of averaged Temp measurements	12.2.32
0x0103	0x0000	TEMP_CLOCK_CFG	Temp measure state machine clock	12.2.33
0x0108	0x0000	TEMP_AVG	Averaged Temp measurement	12.2.34
0x0109	0x0000	TEMP_INST	Instantaneous Temp measurement	12.2.35
0x01B0	0x0033	CAL_OFFSET_ENA	Enable offset calibration modes	12.2.36
0x01B1	0x0033	CAL_GAIN_ENA	Enable gain calibration modes	12.2.37
0x01B2	0x00FF	CAL_BG_MAVG_STEP_SIZE	Background calibration convergence step sizes	12.2.38
0x01B3	0x0FFF	CAL_BG_CORR_CLIP	Background calibration clipping	12.2.39
0x02AB	0x0001	ADC_TEMP_ENA	Temperature ADC enable	12.2.40
0x0300	0x0000	DDC_CFG	DDC channels selections and decimation ratio	12.2.41
0x0301	0x0000	DDC_COARSE_INT_DELAY	Coarse channel integer delay	12.2.42
0x0302	0x0000	DDC_FINE_INT_DELAY	Fine channels integer delays	12.2.43
0x0303	0x0000	DDC_COARSE_FRAC_DELAY	Coarse channel fractional delay	12.2.44
0x0304	0x0000	DDC_FINE0_FRAC_DELAY	Fine channel 0 fractional delay	12.2.45
0x0305	0x0000	DDC_FINE1_FRAC_DELAY	Fine channel 1 fractional delay	
0x0306	0x0000	DDC_FINE2_FRAC_DELAY	Fine channel 2 fractional delay	
0x0307	0x0000	DDC_FINE3_FRAC_DELAY	Fine channel 3 fractional delay	
0x0308	0x136E	DDC_COARSE_GAIN	Coarse channel gain	12.2.46

0x0309	0x136E	DDC_FINE0_GAIN	Fine channel 0 gain	12.2.47
0x030A	0x136E	DDC_FINE1_GAIN	Fine channel 1 gain	
0x030B	0x136E	DDC_FINE2_GAIN	Fine channel 2 gain	
0x030C	0x136E	DDC_FINE3_GAIN	Fine channel 3 gain	
0x030F	0x0000	DDC_FH_MODE	Frequency hopping mode sections	12.2.48
0x0310	0x0000	DDC_CH0_PHASE_INIT_0_LSB	Initial phase of setting 0 of channel 0	12.2.49
0x0311	0x0000	DDC_CH0_PHASE_INIT_0_MSB		
0x0312	0x0000	DDC_CH0_PHASE_INIT_1_LSB	Initial phase of setting 1 of channel 0	
0x0313	0x0000	DDC_CH0_PHASE_INIT_1_MSB		
0x0314	0x0000	DDC_CH0_PHASE_INIT_2_LSB	Initial phase of setting 2 of channel 0	
0x0315	0x0000	DDC_CH0_PHASE_INIT_2_MSB		
0x0316	0x0000	DDC_CH0_PHASE_INIT_3_LSB	Initial phase of setting 3 of channel 0	
0x0317	0x0000	DDC_CH0_PHASE_INIT_3_MSB		
0x0318	0x0000	DDC_CH0_PHASE_INIT_4_LSB	Initial phase of setting 4 of channel 0	
0x0319	0x0000	DDC_CH0_PHASE_INIT_4_MSB		
0x031A	0x0000	DDC_CH0_PHASE_INIT_5_LSB	Initial phase of setting 5 of channel 0	
0x031B	0x0000	DDC_CH0_PHASE_INIT_5_MSB		
0x031C	0x0000	DDC_CH0_PHASE_INIT_6_LSB	Initial phase of setting 6 of channel 0	
0x031D	0x0000	DDC_CH0_PHASE_INIT_6_MSB		
0x031E	0x0000	DDC_CH0_PHASE_INIT_7_LSB	Initial phase of setting 7 of channel 0	
0x031F	0x0000	DDC_CH0_PHASE_INIT_7_MSB		
0x0320	0x0000	DDC_CH0_PHASE_INCR_0_LSB	Phase increment of setting 0 of channel 0	12.2.50
0x0321	0x8000	DDC_CH0_PHASE_INCR_0_MSB		
0x0322	0x0000	DDC_CH0_PHASE_INCR_1_LSB	Phase increment of setting 1 of channel 0	
0x0323	0x8000	DDC_CH0_PHASE_INCR_1_MSB		
0x0324	0x0000	DDC_CH0_PHASE_INCR_2_LSB	Phase increment of setting 2 of channel 0	
0x0325	0x8000	DDC_CH0_PHASE_INCR_2_MSB		
0x0326	0x0000	DDC_CH0_PHASE_INCR_3_LSB	Phase increment of setting 3 of channel 0	
0x0327	0x8000	DDC_CH0_PHASE_INCR_3_MSB		
0x0328	0x0000	DDC_CH0_PHASE_INCR_4_LSB	Phase increment of setting 4 of channel 0	
0x0329	0x8000	DDC_CH0_PHASE_INCR_4_MSB		
0x032A	0x0000	DDC_CH0_PHASE_INCR_5_LSB	Phase increment of setting 5 of channel 0	
0x032B	0x8000	DDC_CH0_PHASE_INCR_5_MSB		
0x032C	0x0000	DDC_CH0_PHASE_INCR_6_LSB	Phase increment of setting 6 of channel 0	
0x032D	0x8000	DDC_CH0_PHASE_INCR_6_MSB		
0x032E	0x0000	DDC_CH0_PHASE_INCR_7_LSB	Phase increment of setting 7 of channel 0	
0x032F	0x8000	DDC_CH0_PHASE_INCR_7_MSB		
0x0330	0x0000	DDC_CH1_PHASE_INIT_0_LSB	Initial phase of setting 0 of channel 1	12.2.49
0x0331	0x0000	DDC_CH1_PHASE_INIT_0_MSB		
0x0332	0x0000	DDC_CH1_PHASE_INIT_1_LSB	Initial phase of setting 1 of channel 1	
0x0333	0x0000	DDC_CH1_PHASE_INIT_1_MSB		
0x0334	0x0000	DDC_CH1_PHASE_INIT_2_LSB	Initial phase of setting 2 of channel 1	
0x0335	0x0000	DDC_CH1_PHASE_INIT_2_MSB		
0x0336	0x0000	DDC_CH1_PHASE_INIT_3_LSB	Initial phase of setting 3 of channel 1	
0x0337	0x0000	DDC_CH1_PHASE_INIT_3_MSB		
0x0338	0x0000	DDC_CH1_PHASE_INIT_4_LSB	Initial phase of setting 4 of channel 1	
0x0339	0x0000	DDC_CH1_PHASE_INIT_4_MSB		
0x033A	0x0000	DDC_CH1_PHASE_INIT_5_LSB	Initial phase of setting 5 of channel 1	
0x033B	0x0000	DDC_CH1_PHASE_INIT_5_MSB		
0x033C	0x0000	DDC_CH1_PHASE_INIT_6_LSB	Initial phase of setting 6 of channel 1	
0x033D	0x0000	DDC_CH1_PHASE_INIT_6_MSB		
0x033E	0x0000	DDC_CH1_PHASE_INIT_7_LSB	Initial phase of setting 7 of channel 1	
0x033F	0x0000	DDC_CH1_PHASE_INIT_7_MSB		
0x0340	0x0000	DDC_CH1_PHASE_INCR_0_LSB	Phase increment of setting 0 of channel 1	12.2.50
0x0341	0x8000	DDC_CH1_PHASE_INCR_0_MSB		
0x0342	0x0000	DDC_CH1_PHASE_INCR_1_LSB	Phase increment of setting 1 of channel 1	
0x0343	0x8000	DDC_CH1_PHASE_INCR_1_MSB		
0x0344	0x0000	DDC_CH1_PHASE_INCR_2_LSB	Phase increment of setting 2 of channel 1	

0x0345	0x8000	DDC_CH1_PHASE_INCR_2_MSB		
0x0346	0x0000	DDC_CH1_PHASE_INCR_3_LSB	Phase increment of setting 3 of channel 1	
0x0347	0x8000	DDC_CH1_PHASE_INCR_3_MSB		
0x0348	0x0000	DDC_CH1_PHASE_INCR_4_LSB	Phase increment of setting 4 of channel 1	
0x0349	0x8000	DDC_CH1_PHASE_INCR_4_MSB		
0x034A	0x0000	DDC_CH1_PHASE_INCR_5_LSB	Phase increment of setting 5 of channel 1	
0x034B	0x8000	DDC_CH1_PHASE_INCR_5_MSB		
0x034C	0x0000	DDC_CH1_PHASE_INCR_6_LSB	Phase increment of setting 6 of channel 1	
0x034D	0x8000	DDC_CH1_PHASE_INCR_6_MSB		
0x034E	0x0000	DDC_CH1_PHASE_INCR_7_LSB	Phase increment of setting 7 of channel 1	
0x034F	0x8000	DDC_CH1_PHASE_INCR_7_MSB		
0x0350	0x0000	DDC_CH2_PHASE_INIT_0_LSB	Initial phase of setting 0 of channel 2	
0x0351	0x0000	DDC_CH2_PHASE_INIT_0_MSB		
0x0352	0x0000	DDC_CH2_PHASE_INIT_1_LSB	Initial phase of setting 1 of channel 2	
0x0353	0x0000	DDC_CH2_PHASE_INIT_1_MSB		
0x0354	0x0000	DDC_CH2_PHASE_INIT_2_LSB	Initial phase of setting 2 of channel 2	
0x0355	0x0000	DDC_CH2_PHASE_INIT_2_MSB		
0x0356	0x0000	DDC_CH2_PHASE_INIT_3_LSB	Initial phase of setting 3 of channel 2	
0x0357	0x0000	DDC_CH2_PHASE_INIT_3_MSB		
0x0358	0x0000	DDC_CH2_PHASE_INIT_4_LSB	Initial phase of setting 4 of channel 2	
0x0359	0x0000	DDC_CH2_PHASE_INIT_4_MSB		
0x035A	0x0000	DDC_CH2_PHASE_INIT_5_LSB	Initial phase of setting 5 of channel 2	
0x035B	0x0000	DDC_CH2_PHASE_INIT_5_MSB		
0x035C	0x0000	DDC_CH2_PHASE_INIT_6_LSB	Initial phase of setting 6 of channel 2	
0x035D	0x0000	DDC_CH2_PHASE_INIT_6_MSB		
0x035E	0x0000	DDC_CH2_PHASE_INIT_7_LSB	Initial phase of setting 7 of channel 2	
0x035F	0x0000	DDC_CH2_PHASE_INIT_7_MSB		
0x0360	0x0000	DDC_CH2_PHASE_INCR_0_LSB	Phase increment of setting 0 of channel 2	
0x0361	0x8000	DDC_CH2_PHASE_INCR_0_MSB		
0x0362	0x0000	DDC_CH2_PHASE_INCR_1_LSB	Phase increment of setting 1 of channel 2	
0x0363	0x8000	DDC_CH2_PHASE_INCR_1_MSB		
0x0364	0x0000	DDC_CH2_PHASE_INCR_2_LSB	Phase increment of setting 2 of channel 2	
0x0365	0x8000	DDC_CH2_PHASE_INCR_2_MSB		
0x0366	0x0000	DDC_CH2_PHASE_INCR_3_LSB	Phase increment of setting 3 of channel 2	
0x0367	0x8000	DDC_CH2_PHASE_INCR_3_MSB		
0x0368	0x0000	DDC_CH2_PHASE_INCR_4_LSB	Phase increment of setting 4 of channel 2	
0x0369	0x8000	DDC_CH2_PHASE_INCR_4_MSB		
0x036A	0x0000	DDC_CH2_PHASE_INCR_5_LSB	Phase increment of setting 5 of channel 2	
0x036B	0x8000	DDC_CH2_PHASE_INCR_5_MSB		
0x036C	0x0000	DDC_CH2_PHASE_INCR_6_LSB	Phase increment of setting 6 of channel 2	
0x036D	0x8000	DDC_CH2_PHASE_INCR_6_MSB		
0x036E	0x0000	DDC_CH2_PHASE_INCR_7_LSB	Phase increment of setting 7 of channel 2	
0x036F	0x8000	DDC_CH2_PHASE_INCR_7_MSB		
0x0370	0x0000	DDC_CH3_PHASE_INIT_0_LSB	Initial phase of setting 0 of channel 3	
0x0371	0x0000	DDC_CH3_PHASE_INIT_0_MSB		
0x0372	0x0000	DDC_CH3_PHASE_INIT_1_LSB	Initial phase of setting 1 of channel 3	
0x0373	0x0000	DDC_CH3_PHASE_INIT_1_MSB		
0x0374	0x0000	DDC_CH3_PHASE_INIT_2_LSB	Initial phase of setting 2 of channel 3	
0x0375	0x0000	DDC_CH3_PHASE_INIT_2_MSB		
0x0376	0x0000	DDC_CH3_PHASE_INIT_3_LSB	Initial phase of setting 3 of channel 3	
0x0377	0x0000	DDC_CH3_PHASE_INIT_3_MSB		
0x0378	0x0000	DDC_CH3_PHASE_INIT_4_LSB	Initial phase of setting 4 of channel 3	
0x0379	0x0000	DDC_CH3_PHASE_INIT_4_MSB		
0x037A	0x0000	DDC_CH3_PHASE_INIT_5_LSB	Initial phase of setting 5 of channel 3	
0x037B	0x0000	DDC_CH3_PHASE_INIT_5_MSB		
0x037C	0x0000	DDC_CH3_PHASE_INIT_6_LSB	Initial phase of setting 6 of channel 3	
0x037D	0x0000	DDC_CH3_PHASE_INIT_6_MSB		
0x037E	0x0000	DDC_CH3_PHASE_INIT_7_LSB	Initial phase of setting 7 of channel 3	

0x037F	0x0000	DDC_CH3_PHASE_INIT_7_MSB		
0x0380	0x0000	DDC_CH3_PHASE_INCR_0_LSB	Phase increment of setting 0 of channel 3	12.2.50
0x0381	0x8000	DDC_CH3_PHASE_INCR_0_MSB		
0x0382	0x0000	DDC_CH3_PHASE_INCR_1_LSB	Phase increment of setting 1 of channel 3	
0x0383	0x8000	DDC_CH3_PHASE_INCR_1_MSB		
0x0384	0x0000	DDC_CH3_PHASE_INCR_2_LSB	Phase increment of setting 2 of channel 3	
0x0385	0x8000	DDC_CH3_PHASE_INCR_2_MSB		
0x0386	0x0000	DDC_CH3_PHASE_INCR_3_LSB	Phase increment of setting 3 of channel 3	
0x0387	0x8000	DDC_CH3_PHASE_INCR_3_MSB		
0x0388	0x0000	DDC_CH3_PHASE_INCR_4_LSB	Phase increment of setting 4 of channel 3	
0x0389	0x8000	DDC_CH3_PHASE_INCR_4_MSB		
0x038A	0x0000	DDC_CH3_PHASE_INCR_5_LSB	Phase increment of setting 5 of channel 3	
0x038B	0x8000	DDC_CH3_PHASE_INCR_5_MSB		
0x038C	0x0000	DDC_CH3_PHASE_INCR_6_LSB	Phase increment of setting 6 of channel 3	
0x038D	0x8000	DDC_CH3_PHASE_INCR_6_MSB		
0x038E	0x0000	DDC_CH3_PHASE_INCR_7_LSB	Phase increment of setting 7 of channel 3	
0x038F	0x8000	DDC_CH3_PHASE_INCR_7_MSB		
0x1000	0x0000	FLASH_MOTIF1_15_0	HSSL repeated Flash sequence	12.2.51
0x1001	0xFFFF	FLASH_MOTIF1_31_16		
0x1002	0xFF00	FLASH_MOTIF1_47_32		
0x1003	0xACF0	FLASH_MOTIF1_63_48		
0x100D	0x0000	SL_INV_DATA	HSSL data inversion	12.2.52
0x1072	0x0000	TIMER_SYNC_FINE_DIS	SYNC local gating against SET events	12.2.53
0x1084	0x0000	TIMER_SSO_DELAY	Programmable delay for SSO and SSO2	12.2.54
0x1085	0x0000	TIMER_SYNC_DELAY	Programmable delay for SYNC input and output	12.2.55
0x10B0	0x0000	FH_OBSERVABILITY1	Frequency hopping observable signals	12.2.56
0x10B1	0x0000	FH_OBSERVABILITY2		

12.2 Register Detailed Description

12.2.1 CHIP_ID (address = 0x0001) [reset = 0x0B14]

Bit	Field	Type	Reset	Description
15:0	CHIP_ID	R	0x0B14	Chip ID number

12.2.2 SERIAL_NUMBER (address = 0x0002) [reset = 0x0000]

Bit	Field	Type	Reset	Description
15:0	SERIAL_NUMBER	R	0x0000	Serial number

12.2.3 FUSE_LOADING (address = 0x0003)

Bit	Field	Type	Reset	Description
0	FUSE_LOADING	W		Download fuses in SPI register

12.2.4 FUSE_STATUS (address = 0x0004)

Bit	Field	Type	Reset	Description
1	STATUS	R		1: fuses OK after fuse loading 0: after fuse loading, CRC failed, one or several fuses are corrupted
0	READY	R		1: fuses ready 0: not ready

12.2.5 TIMER_SYNC_HSSL_DIS (address = 0x0005) [reset = 0x0000]

Bit	Field	Type	Reset	Description
1	UNUSED			
0	HSSL_PROTECT	R/W	0	Gate the SYNC signal at the input of the HSSL

12.2.6 TIMER_SSO_CFG (address = 0x0006) [reset = 0x0001]

Bit	Field	Type	Reset	Description
1	SSO_2_ENA	R/W	0	Enable SSO2 clock
0	SSO_1_ENA	R/W	1	Enable SSO clock

12.2.7 GPIO_OUT_CFG (address = 0x0007) [reset = 0x0000]

Bit	Field	Type	Reset	Description
1	RESERVED	R/W	0	Reserved
0	FH_OUT_ENA	R/W	0	Enable frequency hopping clock GPIO output

12.2.8 TH_CFG (address = 0x0008) [reset = 0x0020]

Bit	Field	Type	Reset	Description
6	RESERVED	R/W	0	Reserved
5	RESERVED	R/W	1	Reserved
4	STBTH	R/W	0	Standby mode data path
3	STBCK	R/W	0	Standby mode clock path
2	BOOST	R/W	0	Boosts the Front-End current (+10%)
1	CAPACAL1	R/W	0	Single to Diff Capacitor 1 Enable
0	CAPACAL2	R/W	0	Single to Diff Capacitor 2 Enable

12.2.9 TIMER_SYNCOUT_CFG (address = 0x0009) [reset = 0x0000]

Bit	Field	Type	Reset	Description
0	SYNCOUT_ENA	R/W	0	Enable SYNC LVDS output

12.2.10 DDC_CH_POWER_ENA (address = 0x000C) [reset = 0x0000]

To be forced to 1 in SCAN mode.

Bit	Field	Type	Reset	Description
3	CH_FINE3_ENA	R/W	0	Channel fine 3 enable
2	CH_FINE2_ENA	R/W	0	Channel fine 2 enable
1	CH_FINE1_ENA	R/W	0	Channel fine 1 enable
0	CH_FINE0_ENA	R/W	0	Channel fine 0 enable

12.2.11 ESI_CFG (address = 0x000E) [reset = 0x001F]

Bit	Field	Type	Reset	Description

6	FLASH_ENA	R/W	0	ESIstream enable, must be written at 1 to be functional. This avoids starting the FPGA synchronization before receiving a SYNC.
5	CB_SEL	R/W	0	Bit DC select 1: timestamp selected 0: parity selected (0 by default)
4	TOGGLE_ENA	R/W	1	Toggle bit enable
3	UNUSED			Unused
2	PRBS_ENA	R/W	1	PRBS enable
1	DC_BAL_ENA	R/W	1	DC-balance enable
0	LSB_FIRST	R/W	1	1: data LSB first for serial link (1 by default) 0: data MSB first for serial link

12.2.12 SL_TEST_MODE_CFG (address = 0x000F) [reset = 0x0020]

Bit	Field	Type	Reset	Description
8	RESERVED	R/W	0	Reserved
7	RESERVED	R/W	0	Reserved
6	RESERVED	R/W	0	Reserved
5	TESTER_CB2_TRUE	R/W	1	CB2 = T for decimation by 64 (default 1)
4	RESERVED	R/W	0	Reserved
3	FORCE_ENA	R/W	0	Force on serial-links a sequence of 64 bits from SL_FORCE_VALUE (12.2.13). Force has priority on Ramp mode.
2:0	RAMP_MODE_SEL	R/W	000	See paragraph 11.2.4 101: 1 ramp 15 bits for 1 SL (1 ramp for 1 SL, the same ramp on all SL) 011: 1 ramp 10 bits for 1 SL (1 ramp for 1 SL, the same ramp on all SL) 001: 1 ramp spread on x serial links (x depends on the functional mode) => 11 SL for decimation by 0 => 8 SL for decimation by 4 => 4 SL for decimation by 8 => 2 SL for decimation by 16 => 1 SL for decimation by 32 and more 000: test mode ramp disabled

12.2.13 SL_FORCE_VALUE_[15+X]_[X] (address = 0x0010 to 0x0013) [reset = 0x0001], X=0,16,32,48

Addr	Bit	Register	Type	Reset	Description
0x0013	15:0	SL_FORCE_VALUE_63_48	R/W	0x0001	
0x0012	15:0	SL_FORCE_VALUE_47_32	R/W	0x0001	
0x0011	15:0	SL_FORCE_VALUE_31_16	R/W	0x0001	
0x0010	15:0	SL_FORCE_VALUE_15_0	R/W	0x0001	

12.2.14 SL_CFG (address = 0x0015) [reset = 0x0001]

Bit	Field	Type	Reset	Description
1:0	SL_CFG	R/W	01	CML buffer driving capability 00: SD short distance (8,5 cm max) 01/10: RS reduced swing (17 cm max) 11: FS full swing with (17 cm max)

12.2.15 SL_ROUT (address = 0x0016) [reset = 0x0001]

Bit	Field	Type	Reset	Description
1:0	SL_ROUT	R/W	01	Output load trimming 11: 62 Ω 01: 50 Ω (default) 00: 41 Ω

12.2.16 SL_POWER_ON (address = 0x0017) [reset = 0x07FF]

This register manages the enable or disable of the 11-serial links. Each bit enables when at '1' or disables when at '0', the corresponding serial links. When disabled, the serializer and the output CML buffer are shut down.

Bit	Field	Type	Reset	Description
10	SL10_ENA	R/W	1	Enable/disable HSSL number 10
9	SL09_ENA	R/W	1	Enable/disable HSSL number 9
8	SL08_ENA	R/W	1	Enable/disable HSSL number 8
7	SL07_ENA	R/W	1	Enable/disable HSSL number 7
6	SL06_ENA	R/W	1	Enable/disable HSSL number 6
5	SL05_ENA	R/W	1	Enable/disable HSSL number 5
4	SL04_ENA	R/W	1	Enable/disable HSSL number 4
3	SL03_ENA	R/W	1	Enable/disable HSSL number 3
2	SL02_ENA	R/W	1	Enable/disable HSSL number 2
1	SL01_ENA	R/W	1	Enable/disable HSSL number 1
0	SL00_ENA	R/W	1	Enable/disable HSSL number 0

12.2.17 FALL_EDGE_SYNC_FLAG (address = 0x0040)

Bit	Field	Type	Reset	Description
0	FALL_EDGE_SYNC_FLAG	R		0: default 1: SYNC in forbidden zone versus clock falling edge

12.2.18 FALL_EDGE_SYNC_CLEAR_FLAG (address = 0x0041)

Bit	Field	Type	Reset	Description
0	FALL_EDGE_SYNC_CLEAR_FLAG	W		Clear syncA flag (simple access to this address clean the flag, just read or write 0 to register)

12.2.19 FALL_EDGE_SYNC_DELAY (address = 0x0042) [reset = 0x0000]

Bit	Field	Type	Reset	Description

1:0	FALL_EDGE_SYNC_DELAY	R/W	00	Add delay on SYNC signal to avoid forbidden zone (for rising edge) 11: three delays (~30 ps) 10: two delays (~20 ps) 01: one delay (~10 ps) 00: no delay

12.2.20 TIMER_A_SSO_DIV2 (address = 0x0043) [reset = 0x0000]

Bit	Field	Type	Reset	Description
0	TIMER_A_SSO_DIV2	R/W	0	SSO additional division by 2. Only with TIMER_A_SSO_INIT = 0x0000 or 0xFFFF (12.2.21)

12.2.21 TIMER_A_SSO_INIT (address = 0x0044) [reset = 0x00FF]

Bit	Field	Type	Reset	Description
15:0	TIMER_A_SSO_INIT	R/W	0x00FF	SSO sequence for shift register 0000/FFFF: Fsso=Fs/64, with TIMER_A_SSO_DIV2 = 1 (12.2.20) 00FF/01FE/03FC/07F8/0FF0/1FE0/3FC0/7F80/FF00/FE01/FC03/F807/F00F/E01F/C03F/807F: Fsso=Fs/32 0F0F/1E1E/3C3C/7878/F0F0/E1E1/C3C3/8787: Fsso=Fs/16 3333/6666/CCCC/9999: Fsso=Fs/8 5555/AAAA: Fsso=Fs/4

12.2.22 RISE EDGE_SYNC_FLAG (address = 0x004B)

Bit	Field	Type	Reset	Description
0	RISE EDGE_SYNC_FLAG	R		0: default. 1: SYNC in forbidden zone versus clock rising edge

12.2.23 RISE_EDGE_SYNC_CLEAR_FLAG (address = 0x004C)

Bit	Field	Type	Reset	Description
0	RISE_EDGE_SYNC_CLEAR_FLAG	W		Clear syncB flag (simple access to this address clean the flag, just read or write 0 to register)

12.2.24 RISE_EDGE_SYNC_DELAY (address = 0x004D) [reset = 0x0000]

Bit	Field	Type	Reset	Description
1:0	RISE_EDGE_SYNC_DELAY	R/W	00	Add delay on SYNC signal to avoid forbidden zone (for falling edge) 11: three delays (~30 ps) 10: two delays (~20 ps) 01: one delay (~10 ps) 00: no delay

12.2.25 TIMER_B_SSO_DIV2 (address = 0x004E) [reset = 0x0000]

Bit	Field	Type	Reset	Description
0	TIMER_B_SSO_DIV2	R/W	0	SSO2 additional division by 2. Only with TIMER_B_SSO_INIT = 0000 or FFFF (12.2.26)

12.2.26 TIMER_B_SSO_INIT (address = 0x004F) [reset = 0x00FF]

Bit	Field	Type	Reset	Description
15:0	TIMER_B_SSO_INIT	R/W	0x00FF	SSO2 sequence for shift register 0000/FFFF: Fsso=Fs/64 with TIMER_B_SSO_DIV2 = 1 (12.2.25) 00FF/01FE/03FC/07F8/0FF0/1FE0/3FC0/7F80/FF00/FE01/FC03/F807/F00F/E01F/C03F/807F: Fsso=Fs/32 0F0F/1E1E/3C3C/7878/F0F0/E1E1/C3C3/8787: Fsso=Fs/16 3333/6666/CCCC/9999: Fsso=Fs/8 5555/AAAA: Fsso=Fs/4

12.2.27 SYNC_SHIFT_FINE (address = 0x0058) [reset = 0x0000]

Bit	Field	Type	Reset	Description
3:0	TIMER_SYNC_SHIFT_FINE	R/W	0x0	For multi syncro fine steps (implemented in timer at Fs) (1) 1111: shift of 15 Fs cycles ... 0010: shift of 2 Fs cycles 0001: shift of 1 Fs cycle 0000: no shift

12.2.28 SYNC_SHIFT_COARSE (address = 0x0060) [reset = 0x0040]

Bit	Field	Type	Reset	Description
7:0	SYNC_SHIFT_COARSE	R/W	0x40	For multi syncro: coarse steps (implemented in digital at Fs/32) 1111 1111: sync shifted by 255x32 of Fs cycles ... 0100 0000: sync shifted by 64x32 of Fs cycles (default) ... 0000 0010: sync shifted by 2x32 of Fs cycles 0000 0001: sync shifted by 32 of Fs cycles 0000 0000: no shift

12.2.29 TIMER_SYNC_BY_SPI_ENA (address = 0x0082) [reset = 0x0000]

Bit	Field	Type	Reset	Description
0	TIMER_SYNC_BY_SPI_ENA	R/W	0	Selection external SYNC and soft SYNC 1: soft sync enabled 0: soft sync disabled For radiation hardening, must be returned to 0

12.2.30 TIMER_SYNC_BY_SPI (address = 0x0083)

Bit	Field	Type	Reset	Description

0	TIMER_SYNC_BY_SPI	W		Soft SYNC by SPI

12.2.31 TEMP_ENA (address = 0x0100) [reset = 0x0000]

Bit	Field	Type	Reset	Description
0	TEMP_ENA	R/W	0	1: Start temperature acquisition 0: Temperature sensor disable

12.2.32 TEMP_AVERAGE_NBR (address = 0x0102) [reset = 0x0008]

Bit	Field	Type	Reset	Description
4:0	TEMP_AVERAGE_NBR	R/W	0x08	Number of temperature measures used for average calculation: 00010: 2 measures 00100: 4 measures 01000: 8 measures 10000: 16 measures Others : 1 measure (averaged = instant temperature)

12.2.33 TEMP_CLOCK_CFG (address = 0x0103) [reset = 0x0000]

Bit	Field	Type	Reset	Description
2	SLOW_CLK_ENA	R/W	0	Slow clock enable
1:0	CLK_SEL	R/W	00	Cock selection 11: GPIO clock to sensor (100 MHz maximum) 10: Fs/32 clock for sensor, if Fs<6.4GHz (200MHz with Fs=6.4GHz, 100MHz if Fs = 3.2GHz) 01: Fs/64 clock for sensor, if Fs>6.4 and Fs<12.8GHz (200MHz with Fs=12.8GHz, 100MHz with Fs=6.4GHz) 00: Fs/128 clock for sensor, if Fs>12.8GHz (100MHz with Fs=12.8GHz)

12.2.34 TEMP_AVG (address = 0x0108) [reset = 0x0000]

Bit	Field	Type	Reset	Description
15	OUT_OF_RANGE	R	0	Out-of-range flag
14:10	RESERVED			
9:0	AVG_VAL	R	0x0000	Temperature averaged value: 2's complement format 8.2 (8 integer bits, 2 decimal bits)

12.2.35 TEMP_INST (address = 0x0109) [reset = 0x0000]

Bit	Field	Type	Reset	Description
15	OUT_OF_RANGE	R	0	Out-of-range flag
14:10	RESERVED			
9:0	INST_VAL	R	0x0000	Temperature instantaneous value: 2's complement format 8.2 (8 integer bits, 2 decimal bits)

12.2.36 CAL_OFFSET_ENA (address = 0x01B0) [reset = 0x0033]

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved
6	BCKGND_UPDATE_ENA	R/W	0	Enable background calibration update
5	LOCAL_UPDATE_ENA	R/W	1	Enable factory local offset calibration update
4	GLOBAL_UPDATE_ENA	R/W	1	Enable factory global offset calibration update
3	RESERVED			Reserved
2	BCKGND_ENA	R/W	0	Select background offset calibration source
1	LOCAL_ENA	R/W	1	Select factory local offset calibration source
0	GLOBAL_ENA	R/W	1	Select factory global offset calibration source

12.2.37 CAL_GAIN_ENA (address = 0x01B1) [reset = 0x0033]

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved
6	BCKGND_UPDATE_ENA	R/W	0	Enable background calibration update
5	LOCAL_UPDATE_ENA	R/W	1	Enable factory local gain calibration update
4	GLOBAL_UPDATE_ENA	R/W	1	Enable factory global gain calibration update
3	RESERVED			Reserved
2	BCKGND_ENA	R/W	0	Select background gain calibration source
1	LOCAL_ENA	R/W	1	Select factory local gain calibration source
0	GLOBAL_ENA	R/W	1	Select factory global gain calibration source

12.2.38 CAL_BG_MAVG_STEP_SIZE (address = 0x01B2) [reset = 0x00FF]

Bit	Field	Type	Reset	Description
7:4	BKCGND_OFST_STEP	R/W	0xF	Select step-size of offset cal (mu). Steps are powers of 2, range from 2^{-11} to 2^{-21} 0000: 2^{-11} 0001: 2^{-12} … 1010: 2^{-21}
3:0	BKCGND_GAIN_STEP	R/W	0xF	Select step-size of gain cal (mu). Steps are powers of 2, range from 2^{-7} to 2^{-17} 0000: 2^{-7} 0001: 2^{-8} … 1010: 2^{-17}

12.2.39 CAL_BG_CORR_CLIP (address = 0x01B3) [reset = 0x0FFF]

Default full correction range is maximum two's complement value which is +/-6.25% of full range. Clip value is tunable with steps of 0.78125% in the range 0.78125% to 6.25%

Bit	Field	Type	Reset	Description
11:9	BKCGND_OFST_CLIP_POS	R/W	111	Clip offset calibration towards positive
8:6	BKCGND_OFST_CLIP_NEG	R/W	111	Clip offset calibration towards negative
5:3	BKCGND_GAIN_CLIP_POS	R/W	111	Clip gain calibration towards positive
2:0	BKCGND_GAIN_CLIP_NEG	R/W	111	Clip gain calibration towards negative

12.2.40 ADC_TEMP_ENA (address = 0x02AB) [reset = 0x0001]

Settings for temperature ADC.

Bit	Field	Type	Reset	Description
0	SARA_TEMP_ENA	R/W	1	Enable temperature SAR

12.2.41 DDC_CFG (address = 0x0300) [reset = 0x0000]

Bit	Field	Type	Reset	Description
10:6	CH_ENA	R/W	0x00	Fine or Coarse decimation enables: 10000 : 4 channels fine used (CH0 to CH3) 01000 : 3 channels fine used (CH0, CH1 and CH2) 00100 : 2 channels fine used (CH0 and CH1) 00010 : 1 channel fine used (CH0) 00001 : 1 channel coarse used 00000 : DDC disabled
5:0	DECIM_RATIO	R/W	0x00	Fine or Coarse decimation ratio: 11 1111 : deciim fine by 2048 01 1111 : decim fine by 1024 00 1111 : decim fine by 512 00 0111 : decim fine by 256 or decim. coarse by 32 00 0011 : decim fine by 128 or decim. coarse by 16 00 0001 : decim fine by 64 or decim. coarse by 8 00 0000 : decim fine by 32 or decim. coarse by 4

12.2.42 DDC_COARSE_INT_DELAY (address = 0x0301) [reset = 0x0000]

Bit	Field	Type	Reset	Description
3:0	DDC_COARSE_INT_DELAY	R/W	0x0	coarse channel integer delay number of samples delay (range 0 to 15) of the input data

12.2.43 DDC_FINE_INT_DELAY (address = 0x0302) [reset = 0x0000]

Bit	Field	Type	Reset	Description
15:12	CH3_FINE	R/W	0x0	fine channel 3 integer delay number of samples delay (range 0 to 15) of the input data
11:8	CH2_FINE	R/W	0x0	fine channel 2 integer delay number of samples delay (range 0 to 15) of the input data
7:4	CH1_FINE	R/W	0x0	fine channel 1 integer delay number of samples delay (range 0 to 15) of the input data
3:0	CH0_FINE	R/W	0x0	fine channel 0 integer delay number of samples delay (range 0 to 15) of the input data

12.2.44 DDC_COARSE_FRAC_DELAY (address = 0x0303) [reset = 0x0000]

Bit	Field	Type	Reset	Description
6:0	DDC_COARSE_FRAC_DELAY	R/W	0x00	Coarse channel fractional delay. Range from -0.5 to 0.5 sample delay of the input data rate. Value has a signed representation, e.g., “1000000” = -0.5

12.2.45 DDC_FINE[X]_FRAC_DELAY (address = 0x0304 to 0x0307) [reset = 0x0000], X=0 to 3

Addr	Bit	Register	Type	Reset	Description
0x0307	6:0	DDC_FINE3_FRAC_DELAY	R/W	0x00	Fine channel 3 fractional delay. Range from -0.5 to 0.5 sample delay of the input data rate. Value has a signed representation, e.g., “1000000” = -0.5
0x0306	6:0	DDC_FINE2_FRAC_DELAY	R/W	0x00	Fine channel 2 fractional delay.
0x0305	6:0	DDC_FINE1_FRAC_DELAY	R/W	0x00	Fine channel 1 fractional delay.
0x0304	6:0	DDC_FINE0_FRAC_DELAY	R/W	0x00	Fine channel 0 fractional delay.

12.2.46 DDC_COARSE_GAIN (address = 0x0308) [reset = 0x136E]

Bit	Field	Type	Reset	Description
12:0	DDC_COARSE_GAIN	R/W	0x00	Coarse channel gain. Range from 0 to 1,65. 0x136E correspond to gain = 1

12.2.47 DDC_FINE[X]_GAIN (address = 0x0309 to 0x030C) [reset = 0x136E], X=0 to 3

Addr	Bit	Register	Type	Reset	Description
0x030C	12:0	DDC_FINE3_GAIN	R/W	0x136E	Fine channel 3 gain. Range from 0 to 1,65. 0x136E correspond to gain = 1
0x030B	12:0	DDC_FINE2_GAIN	R/W	0x136E	Fine channel 2 gain.
0x030A	12:0	DDC_FINE1_GAIN	R/W	0x136E	Fine channel 1 gain.
0x0309	12:0	DDC_FINE0_GAIN	R/W	0x136E	Fine channel 0 gain.

12.2.48 DDC_FH_MODE (address = 0x030F) [reset = 0x0000]

Bit	Field	Type	Reset	Description
3	FH_ENA	R/W	0	Frequency Hopping Enable
2	GPIO_FREQ	R/W	0	GPIO frequency 1: Fs/256 0: Fs/128
1	RESERVED	R/W	0	
0	FH_PHASE_MODE	R/W	0	Frequency hopping mode: 1: phase coherent mode (switch between 4 accumulators per channel) 0: phase reset (phase restart at 0) or continuous mode (phase restart at the same value)

12.2.49 DDC_CH[X]_PHASE_INIT_[Y] (address = 0x0310 to 0x37F) [reset = 0x0000], X= 0 to 3

Addr	Bit	Register	Type	Reset	Description
0x037F	15:0	DDC_CH3_PHASE_INIT_7_MSB	R/W	0x0000	Phase initial value (32 bits distributed on LSB and MSB) for CHANNEL FINE 3
0x037E	15:0	DDC_CH3_PHASE_INIT_7_LSB	R/W	0x0000	
0x037D	15:0	DDC_CH3_PHASE_INIT_6_MSB	R/W	0x0000	
0x037C	15:0	DDC_CH3_PHASE_INIT_6_LSB	R/W	0x0000	
0x037B	15:0	DDC_CH3_PHASE_INIT_5_MSB	R/W	0x0000	
0x037A	15:0	DDC_CH3_PHASE_INIT_5_LSB	R/W	0x0000	
0x0379	15:0	DDC_CH3_PHASE_INIT_4_MSB	R/W	0x0000	
0x0378	15:0	DDC_CH3_PHASE_INIT_4_LSB	R/W	0x0000	
0x0377	15:0	DDC_CH3_PHASE_INIT_3_MSB	R/W	0x0000	
0x0376	15:0	DDC_CH3_PHASE_INIT_3_LSB	R/W	0x0000	
0x0375	15:0	DDC_CH3_PHASE_INIT_2_MSB	R/W	0x0000	
0x0374	15:0	DDC_CH3_PHASE_INIT_2_LSB	R/W	0x0000	
0x0373	15:0	DDC_CH3_PHASE_INIT_1_MSB	R/W	0x0000	
0x0372	15:0	DDC_CH3_PHASE_INIT_1_LSB	R/W	0x0000	
0x0371	15:0	DDC_CH3_PHASE_INIT_0_MSB	R/W	0x0000	
0x0370	15:0	DDC_CH3_PHASE_INIT_0_LSB	R/W	0x0000	
0x035F	15:0	DDC_CH2_PHASE_INIT_7_MSB	R/W	0x0000	Phase initial value (32 bits distributed on LSB and MSB) for CHANNEL FINE 2
0x035E	15:0	DDC_CH2_PHASE_INIT_7_LSB	R/W	0x0000	

0x035D	15:0	DDC_CH2_PHASE_INIT_6_MSB	R/W	0x0000	
0x035C	15:0	DDC_CH2_PHASE_INIT_6_LSB	R/W	0x0000	
0x035B	15:0	DDC_CH2_PHASE_INIT_5_MSB	R/W	0x0000	
0x035A	15:0	DDC_CH2_PHASE_INIT_5_LSB	R/W	0x0000	
0x0359	15:0	DDC_CH2_PHASE_INIT_4_MSB	R/W	0x0000	
0x0358	15:0	DDC_CH2_PHASE_INIT_4_LSB	R/W	0x0000	
0x0357	15:0	DDC_CH2_PHASE_INIT_3_MSB	R/W	0x0000	
0x0356	15:0	DDC_CH2_PHASE_INIT_3_LSB	R/W	0x0000	
0x0355	15:0	DDC_CH2_PHASE_INIT_2_MSB	R/W	0x0000	
0x0354	15:0	DDC_CH2_PHASE_INIT_2_LSB	R/W	0x0000	
0x0353	15:0	DDC_CH2_PHASE_INIT_1_MSB	R/W	0x0000	
0x0352	15:0	DDC_CH2_PHASE_INIT_1_LSB	R/W	0x0000	
0x0351	15:0	DDC_CH2_PHASE_INIT_0_MSB	R/W	0x0000	
0x0350	15:0	DDC_CH2_PHASE_INIT_0_LSB	R/W	0x0000	
0x033F	15:0	DDC_CH1_PHASE_INIT_7_MSB	R/W	0x0000	
0x033E	15:0	DDC_CH1_PHASE_INIT_7_LSB	R/W	0x0000	
0x033D	15:0	DDC_CH1_PHASE_INIT_6_MSB	R/W	0x0000	
0x033C	15:0	DDC_CH1_PHASE_INIT_6_LSB	R/W	0x0000	
0x033B	15:0	DDC_CH1_PHASE_INIT_5_MSB	R/W	0x0000	
0x033A	15:0	DDC_CH1_PHASE_INIT_5_LSB	R/W	0x0000	
0x0339	15:0	DDC_CH1_PHASE_INIT_4_MSB	R/W	0x0000	
0x0338	15:0	DDC_CH1_PHASE_INIT_4_LSB	R/W	0x0000	Phase initial value (32 bits distributed on LSB and MSB) for CHANNEL FINE 1
0x0337	15:0	DDC_CH1_PHASE_INIT_3_MSB	R/W	0x0000	
0x0336	15:0	DDC_CH1_PHASE_INIT_3_LSB	R/W	0x0000	
0x0335	15:0	DDC_CH1_PHASE_INIT_2_MSB	R/W	0x0000	
0x0334	15:0	DDC_CH1_PHASE_INIT_2_LSB	R/W	0x0000	
0x0333	15:0	DDC_CH1_PHASE_INIT_1_MSB	R/W	0x0000	
0x0332	15:0	DDC_CH1_PHASE_INIT_1_LSB	R/W	0x0000	
0x0331	15:0	DDC_CH1_PHASE_INIT_0_MSB	R/W	0x0000	
0x0330	15:0	DDC_CH1_PHASE_INIT_0_LSB	R/W	0x0000	
0x031F	15:0	DDC_CH0_PHASE_INIT_7_MSB	R/W	0x0000	
0x031E	15:0	DDC_CH0_PHASE_INIT_7_LSB	R/W	0x0000	
0x031D	15:0	DDC_CH0_PHASE_INIT_6_MSB	R/W	0x0000	
0x031C	15:0	DDC_CH0_PHASE_INIT_6_LSB	R/W	0x0000	
0x031B	15:0	DDC_CH0_PHASE_INIT_5_MSB	R/W	0x0000	
0x031A	15:0	DDC_CH0_PHASE_INIT_5_LSB	R/W	0x0000	
0x0319	15:0	DDC_CH0_PHASE_INIT_4_MSB	R/W	0x0000	
0x0318	15:0	DDC_CH0_PHASE_INIT_4_LSB	R/W	0x0000	Phase initial value (32 bits distributed on LSB and MSB) for CHANNEL FINE 1 or CHANNEL COARSE
0x0317	15:0	DDC_CH0_PHASE_INIT_3_MSB	R/W	0x0000	
0x0316	15:0	DDC_CH0_PHASE_INIT_3_LSB	R/W	0x0000	
0x0315	15:0	DDC_CH0_PHASE_INIT_2_MSB	R/W	0x0000	
0x0314	15:0	DDC_CH0_PHASE_INIT_2_LSB	R/W	0x0000	
0x0313	15:0	DDC_CH0_PHASE_INIT_1_MSB	R/W	0x0000	
0x0312	15:0	DDC_CH0_PHASE_INIT_1_LSB	R/W	0x0000	
0x0311	15:0	DDC_CH0_PHASE_INIT_0_MSB	R/W	0x0000	

0x0310	15:0	DDC_CH0_PHASE_INIT_0_LSB	R/W	0x0000	

12.2.50 DDC_CH[X]_PHASE_INCR_[Y] (address = 0x0320 to 0x038F) [reset = 0x0000/0x8000]

Addr	Bit	Register	Type	Reset	Description
0x038F	15:0	DDC_CH3_PHASE_INCR_7_MSB	R/W	0x8000	Phase increment value (32 bits distributed on LSB and MSB) for CHANNEL FINE 3 8000 0000 = LO=Fs/2 4000 0000 = LO=Fs/4 2000 0000 = LO=Fs/8 0000 0001 = LO=Fs/2^32
0x038E	15:0	DDC_CH3_PHASE_INCR_7_LSB	R/W	0x0000	
0x038D	15:0	DDC_CH3_PHASE_INCR_6_MSB	R/W	0x8000	
0x038C	15:0	DDC_CH3_PHASE_INCR_6_LSB	R/W	0x0000	
0x038B	15:0	DDC_CH3_PHASE_INCR_5_MSB	R/W	0x8000	
0x038A	15:0	DDC_CH3_PHASE_INCR_5_LSB	R/W	0x0000	
0x0389	15:0	DDC_CH3_PHASE_INCR_4_MSB	R/W	0x8000	
0x0388	15:0	DDC_CH3_PHASE_INCR_4_LSB	R/W	0x0000	
0x0387	15:0	DDC_CH3_PHASE_INCR_3_MSB	R/W	0x8000	
0x0386	15:0	DDC_CH3_PHASE_INCR_3_LSB	R/W	0x0000	
0x0385	15:0	DDC_CH3_PHASE_INCR_2_MSB	R/W	0x8000	
0x0384	15:0	DDC_CH3_PHASE_INCR_2_LSB	R/W	0x0000	
0x0383	15:0	DDC_CH3_PHASE_INCR_1_MSB	R/W	0x8000	
0x0382	15:0	DDC_CH3_PHASE_INCR_1_LSB	R/W	0x0000	
0x0381	15:0	DDC_CH3_PHASE_INCR_0_MSB	R/W	0x8000	
0x0380	15:0	DDC_CH3_PHASE_INCR_0_LSB	R/W	0x0000	
0x036F	15:0	DDC_CH2_PHASE_INCR_7_MSB	R/W	0x8000	Phase increment value (32 bits distributed on LSB and MSB) for CHANNEL FINE 2 8000 0000 = LO=Fs/2 4000 0000 = LO=Fs/4 2000 0000 = LO=Fs/8 0000 0001 = LO=Fs/2^32
0x036E	15:0	DDC_CH2_PHASE_INCR_7_LSB	R/W	0x0000	
0x036D	15:0	DDC_CH2_PHASE_INCR_6_MSB	R/W	0x8000	
0x036C	15:0	DDC_CH2_PHASE_INCR_6_LSB	R/W	0x0000	
0x036B	15:0	DDC_CH2_PHASE_INCR_5_MSB	R/W	0x8000	
0x036A	15:0	DDC_CH2_PHASE_INCR_5_LSB	R/W	0x0000	
0x0369	15:0	DDC_CH2_PHASE_INCR_4_MSB	R/W	0x8000	
0x0368	15:0	DDC_CH2_PHASE_INCR_4_LSB	R/W	0x0000	
0x0367	15:0	DDC_CH2_PHASE_INCR_3_MSB	R/W	0x8000	
0x0366	15:0	DDC_CH2_PHASE_INCR_3_LSB	R/W	0x0000	
0x0365	15:0	DDC_CH2_PHASE_INCR_2_MSB	R/W	0x8000	
0x0364	15:0	DDC_CH2_PHASE_INCR_2_LSB	R/W	0x0000	
0x0363	15:0	DDC_CH2_PHASE_INCR_1_MSB	R/W	0x8000	
0x0362	15:0	DDC_CH2_PHASE_INCR_1_LSB	R/W	0x0000	
0x0361	15:0	DDC_CH2_PHASE_INCR_0_MSB	R/W	0x8000	
0x0360	15:0	DDC_CH2_PHASE_INCR_0_LSB	R/W	0x0000	
0x034F	15:0	DDC_CH1_PHASE_INCR_7_MSB	R/W	0x8000	Phase increment value (32 bits distributed on LSB and MSB) for CHANNEL FINE 1 8000 0000 = LO=Fs/2 4000 0000 = LO=Fs/4 2000 0000 = LO=Fs/8 0000 0001 = LO=Fs/2^32
0x034E	15:0	DDC_CH1_PHASE_INCR_7_LSB	R/W	0x0000	
0x034D	15:0	DDC_CH1_PHASE_INCR_6_MSB	R/W	0x8000	
0x034C	15:0	DDC_CH1_PHASE_INCR_6_LSB	R/W	0x0000	
0x034B	15:0	DDC_CH1_PHASE_INCR_5_MSB	R/W	0x8000	
0x034A	15:0	DDC_CH1_PHASE_INCR_5_LSB	R/W	0x0000	
0x0349	15:0	DDC_CH1_PHASE_INCR_4_MSB	R/W	0x8000	
0x0348	15:0	DDC_CH1_PHASE_INCR_4_LSB	R/W	0x0000	

0x0347	15:0	DDC_CH1_PHASE_INCR_3_MSB	R/W	0x8000	
0x0346	15:0	DDC_CH1_PHASE_INCR_3_LSB	R/W	0x0000	
0x0345	15:0	DDC_CH1_PHASE_INCR_2_MSB	R/W	0x8000	
0x0344	15:0	DDC_CH1_PHASE_INCR_2_LSB	R/W	0x0000	
0x0343	15:0	DDC_CH1_PHASE_INCR_1_MSB	R/W	0x8000	
0x0342	15:0	DDC_CH1_PHASE_INCR_1_LSB	R/W	0x0000	
0x0341	15:0	DDC_CH1_PHASE_INCR_0_MSB	R/W	0x8000	
0x0340	15:0	DDC_CH1_PHASE_INCR_0_LSB	R/W	0x0000	
0x032F	15:0	DDC_CH0_PHASE_INCR_7_MSB	R/W	0x8000	Phase increment value (32 bits distributed on LSB and MSB) for CHANNEL FINE 0 or CHANNEL COARSE 8000 0000 = LO=Fs/2 4000 0000 = LO=Fs/4 2000 0000 = LO=Fs/8 0000 0001 = LO=Fs/2^32
0x032E	15:0	DDC_CH0_PHASE_INCR_7_LSB	R/W	0x0000	
0x032D	15:0	DDC_CH0_PHASE_INCR_6_MSB	R/W	0x8000	
0x032C	15:0	DDC_CH0_PHASE_INCR_6_LSB	R/W	0x0000	
0x032B	15:0	DDC_CH0_PHASE_INCR_5_MSB	R/W	0x8000	
0x032A	15:0	DDC_CH0_PHASE_INCR_5_LSB	R/W	0x0000	
0x0329	15:0	DDC_CH0_PHASE_INCR_4_MSB	R/W	0x8000	
0x0328	15:0	DDC_CH0_PHASE_INCR_4_LSB	R/W	0x0000	
0x0327	15:0	DDC_CH0_PHASE_INCR_3_MSB	R/W	0x8000	
0x0326	15:0	DDC_CH0_PHASE_INCR_3_LSB	R/W	0x0000	
0x0325	15:0	DDC_CH0_PHASE_INCR_2_MSB	R/W	0x8000	
0x0324	15:0	DDC_CH0_PHASE_INCR_2_LSB	R/W	0x0000	
0x0323	15:0	DDC_CH0_PHASE_INCR_1_MSB	R/W	0x8000	
0x0322	15:0	DDC_CH0_PHASE_INCR_1_LSB	R/W	0x0000	
0x0321	15:0	DDC_CH0_PHASE_INCR_0_MSB	R/W	0x8000	
0x0320	15:0	DDC_CH0_PHASE_INCR_0_LSB	R/W	0x0000	

12.2.51 FLASH_MOTIF1_[15+X]_[X] (address = 0x1000 to 0x1003) [reset = 0x0000,FFFF,FF00,ACF0], X=0,16,32,48

Output 64-bit repeated sequence for HSSL in flash mode.

Addr	Bit	Register	Type	Reset	Description
0x1003	15:0	FLASH_MOTIF1_63_48	R/W	0xACF0	sequence bits 48 to 63
0x1002	15:0	FLASH_MOTIF1_47_32	R/W	0xFF00	sequence bits 32 to 47
0x1001	15:0	FLASH_MOTIF1_31_16	R/W	0xFFFF	sequence bits 16 to 31
0x1000	15:0	FLASH_MOTIF1_15_0	R/W	0x0000	sequence bits 0 to 15

12.2.52 SL_INV_DATA (address = 0x100D) [reset = 0x0000]

Invert data on serial link.

Bit	Field	Type	Reset	Description
10	SL10_INV_DATA	R/W	0	
9	SL09_INV_DATA	R/W	0	
8	SL08_INV_DATA	R/W	0	
7	SL07_INV_DATA	R/W	0	
6	SL06_INV_DATA	R/W	0	
5	SL05_INV_DATA	R/W	0	

4	SL04_INV_DATA	R/W	0	
3	SL03_INV_DATA	R/W	0	
2	SL02_INV_DATA	R/W	0	
1	SL01_INV_DATA	R/W	0	
0	SL00_INV_DATA	R/W	0	

12.2.53 TIMER_SYNC_FINE_DIS (address = 0x1072) [reset = 0x0000]

Gate the SYNC signal on specific sub-functions (to protect the circuit from SEE events or simply to synchronize only a specific function)

Bit	Field	Type	Reset	Description
15	CONVB	R/W	0	Gate SYNC for conversion path B clock
14	DATAB	R/W	0	Gate SYNC for B data-path clock
13	CONVA	R/W	0	Gate SYNC for conversion path A clock
12	DATAA	R/W	0	Gate SYNC for A data-path clock
11	INTERNAL_TMR3	R/W	0	Gate SYNC for parity bit calculation (tripled)
10	INTERNAL_TMR2	R/W	0	
9	INTERNAL_TMR1	R/W	0	
8	SERDES	R/W	0	Gate SYNC for HSSL clock
7	SSOB	R/W	0	Gate SYNC for SSO2 clock
6	SSOA	R/W	0	Gate SYNC for SSO clock
5	SYNCB	R/W	0	Gate SYNC for B-path clock SYNC
4	SYNCA	R/W	0	Gate SYNC for A-path clock SYNC
3	SYNCSHIFTB	R/W	0	Gate SYNC for B-path clock SYNCSHIFT
2	SYNCSHIFTA	R/W	0	Gate SYNC for A-path clock SYNCSHIFT
1	SYNCDIG	R/W	0	Gate SYNC for digital clock SYNC
0	CKDIG	R/W	0	Gate SYNC for digital clock

12.2.54 TIMER_SSO_DELAY (address = 0x1084) [reset = 0x0000]

Bit	Field	Type	Reset	Description
9:5	SSO2	R/W	0x00	SDA delay for SSO2. Increment: 14ps in typical PVT corners
4:0	SSO1	R/W	0x00	SDA delay for SSO. Increment: 14ps in typical PVT corners

12.2.55 TIMER_SYNC_DELAY (address = 0x1085) [reset = 0x0000]

Bit	Field	Type	Reset	Description
9:5	SYNCO	R/W	0x00	SDA delay for output SYNC. Increment: 14ps typical
4:0	SYNCI	R/W	0x00	SDA delay for input SYNC. Increment: 14ps typical

12.2.56 FH_OBSERVABILITY[X] (address = 0x10B0, 0x10B1), X= 1, 2

Addr	Bit	Field	Type	Reset	Description
FH_OBSERVABILITY2					
0x10B1	15:14	CH_F4_PH_SEL	R		

	13:12	CH_F3_PH_SEL	R		
	11:9	SWITCH_C4_PH_INCR	R		
	8:6	SWITCH_C3_PH_INCR	R		
	5:3	SWITCH_C2_PH_INCR	R		
	2:0	SWITCH_C1_PH_INCR	R		
FH_OBSERVABILITY1					
0x10B0	15:14	CH_F2_PH_SEL	R		
	13:12	CH_F1_PH_SEL	R		
	11:9	SWITCH_C4_PH_ACCU	R		
	8:6	SWITCH_C3_PH_ACCU	R		
	5:3	SWITCH_C2_PH_ACCU	R		
	2:0	SWITCH_C1_PH_ACCU	R		

13. APPLICATION INFORMATION

13.1 Power Supply Sequencing

The is no specific power up sequencing on the different EV10AS940 supplies, but **we highly recommend** to ramp-up all the supplies simultaneously. Moreover, no power supply should be left unpowered when the component is plugged.

14. ORDERING INFORMATION

Table 17 : Product Ordering Information.

Part Number	Package	Temperature Range	Screening Level	RoHS	Comment
EVP10AS940ZJ	FC-BGA350	Ambient	Prototype	Pb-Free	Prototype

Table 18 : Daisy Chain Ordering Information.

Part Number	Package	Temperature Range	Screening Level	RoHS	Comment
XDCHAIN350-ZJ	FC-BGA350	Ambient	N/A	Pb-Free	Daisy Chain Package

Table 19 : Evaluation Kit Ordering Information.

Part Number	Temperature Range	Screening Level	Comment
EV10AS940X-FMC-EVM	Ambient	Prototype	Development Kit : ADC evaluation board with FMC+ connector
EV10AS940X-FPG-EVM	Ambient	Prototype	Demo Kit : ADC and FPGA evaluation board

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