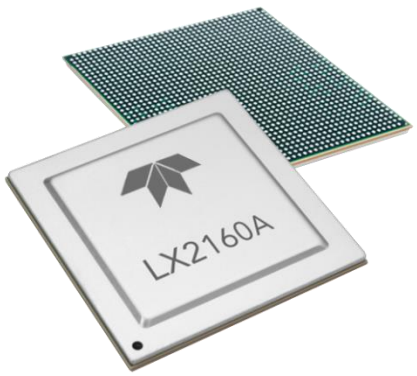
LX2160A

Datasheet - Preliminary Specification

DS 60S 222625



Features

- Arm Cortex®-A72 cores:
  - Up to 2.2 GHz
  - Single-threaded cores with 48KB L1 instruction cache and 32 KB L1 data cache
  - Layerscape® LX2160A has 16 cores, 8 MB L2 cache; LX2120A has 12 cores, 6 MB L2 cache; LX2080A has 8 cores, 8 MB L2 cache
- Cache Coherent Interconnect Fabric
  - Up to 1500 MHz
  - 8 MB Level 3 cache with ECC and On-Chip Memory (OCM) mode
- Two 72-bit (64-bit + ECC) 3.2 GT/s DDR4 SDRAM memory controllers with ECC
- Datapath acceleration architecture 2.0 (DPAA2)
  - Packet parsing, classification, and distribution (WRIOP)
  - Queue and hardware buffer management
  - Cryptography acceleration (SEC) at up to 50 Gbps
  - Decompression/compression acceleration (DCE) at up to 100 Gbps
  - Queue Direct Memory Access (QDMA) engine
  - Management complex (MC)
  - 2 MB Packet express buffer
  - L2 Switching (114 Gbps)
- 24 SerDes lanes at up to 25 Gbps
- High-speed peripheral interfaces
  - Two PCI express Gen 3.0 8-lane controllers supporting SR-IOV
  - Four PCI express Gen 3.0 4-lane controllers
  - Four serial ATA (SATA 3.0) controllers
- Ethernet interfaces supporting IEEE 1588
  - Up to 18 Ethernet MACs
  - Support for 10G-SXGMII (USXGMII)
  - Support for SGMII (and 1000Base-KX)
  - Support for XFI, SFI, and 10GBase-KR
  - Support for CAUI4 (100G), 50GAUI-2 (50G), 25G- AUI (25G)
  - Support for XLAUI4 (and 40GBase-KR4) for 40G
  - Support for two RGMII parallel interfaces
  - Energy-efficient support (802.3az)
- Additional peripheral interfaces
  - Two USB 3.0 controllers with integrated PHY
  - Two enhanced secure digital host controllers
  - Two Controller Area Network (CAN) modules, optionally supporting Flexible Data rate
  - Flexible Serial Peripheral Interface (FlexSPI) and three Serial Peripheral Interface (SPI) controllers
  - Eight I2C controllers
  - Four UARTs
  - General Purpose IO (GPIO)
- Support for hardware virtualization and partitioning enforcement (Arm MMU-500)
- QorIQ platform trust architecture 3.0 with 256 KB on-chip RAM for trusted accesses
- Global interrupt controller (Arm GIC-500)
- Two Flextimers, one secure watchdog timer and one non-secure watchdog timer
- Debug supporting run control, data acquisition, high-speed trace, and performance/event monitoring
- Support for Voltage ID (VID) for yield improvement

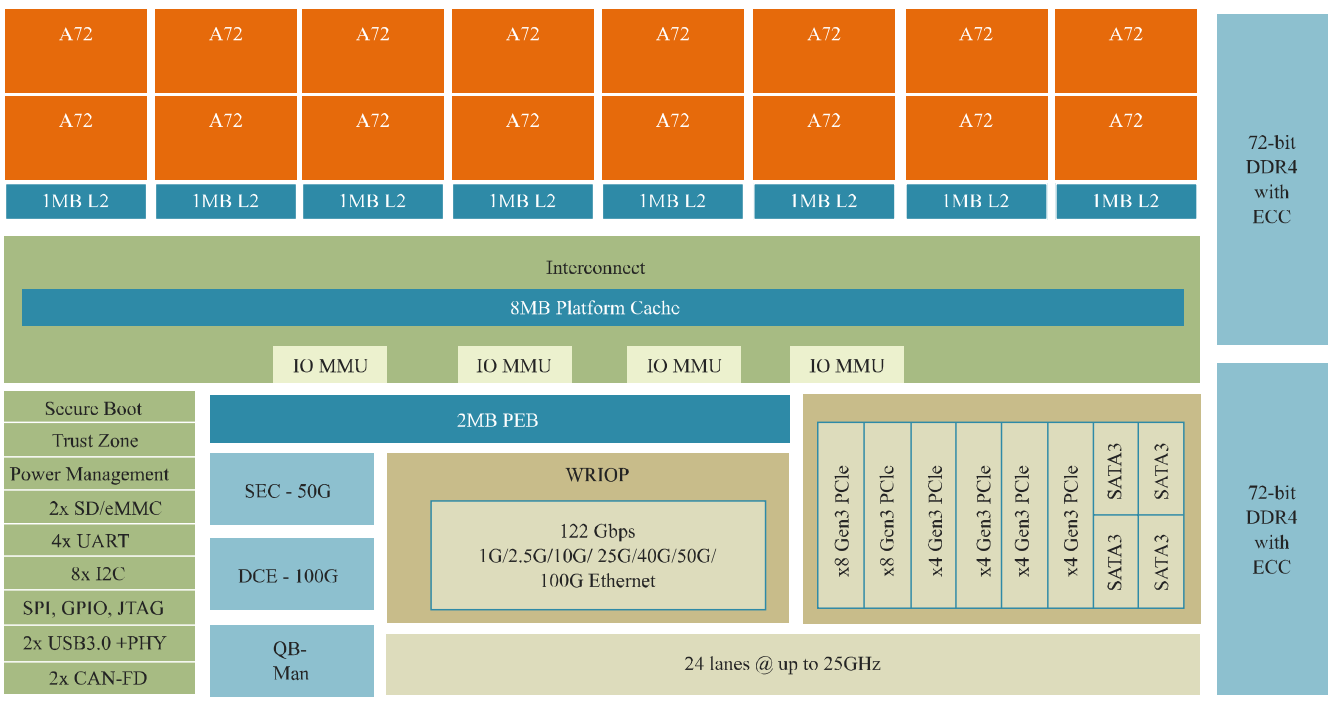
1 INTRODUCTION

The Layerscape® LX2160A processor is built on software-aware, core-agnostic DPAA2(*) architecture, which delivers scalable acceleration elements sized for application needs, unprecedented efficiency, and smarter, more capable networks. When coupled with ease-of-use facilities such as real-time monitoring and debug, virtualization, and software management utilities, the available toolkits allow for both hardware and software engineers to bring a complete solution to market faster than ever.[1]

The device integrated multicore processor combines sixteen Arm Cortex®-A72 processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, storage, telecom/datacom, wireless infrastructure, automotive, and military/aerospace applications.

The device processor is supported by a consistent API that provides both basic and complex manipulation of the hardware peripherals in the device, releasing the developer from the classic programming challenges of interfacing with new peripherals at the hardware level.

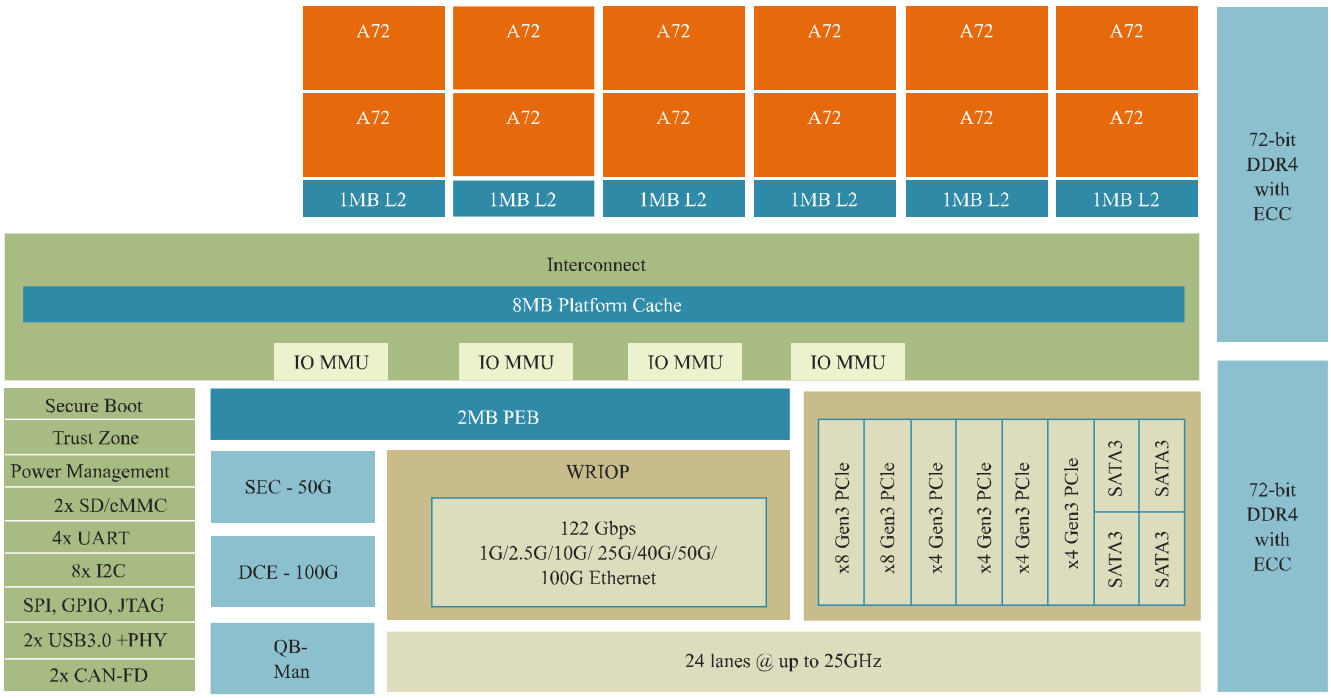
Figure 1. LX2160A Block diagram



The LX2120A integrated multicore processor combines twelve Arm® v8 A72 cores. This figure shows the major functional units within the chip

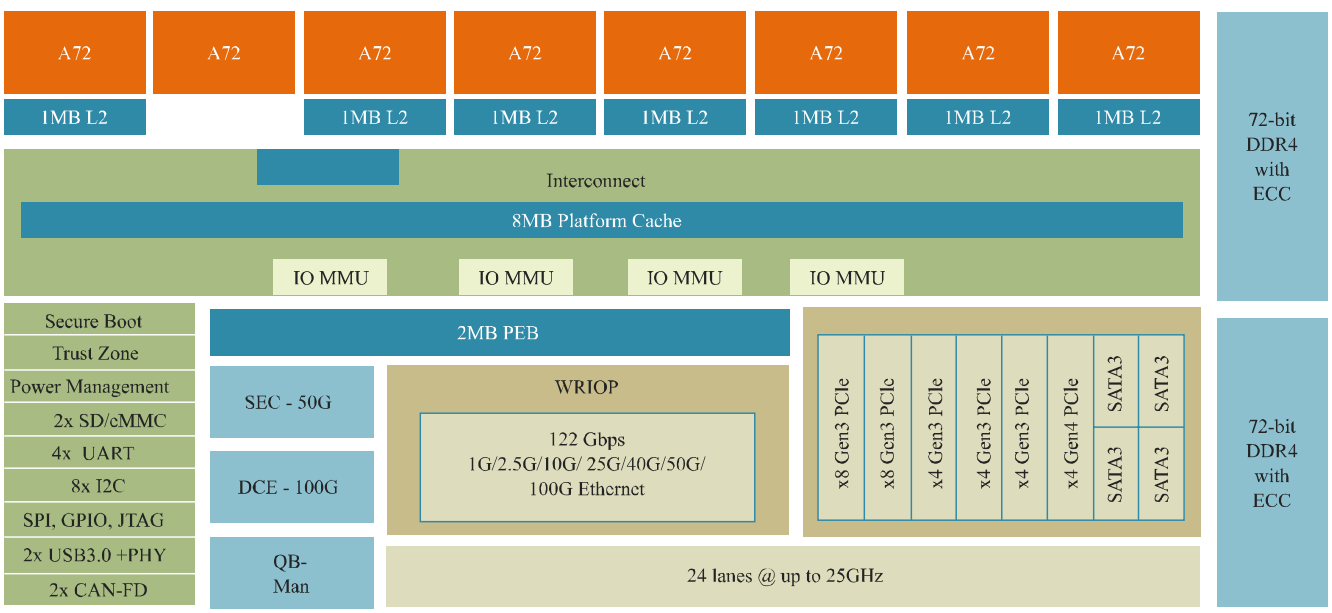
(*) DPAA2 architecture is an evolution and extension of DPAA, a comprehensive architecture which integrates all aspects of packet processing in the SoC, addressing issues and requirements resulting from the multicore nature of QorIQ™ SoCs.

Figure 2. LX2120A Block diagram



The LX2080A integrated multicore processor combines eight Arm® v8 A72 cores. This figure shows the major functional units within the chip.

Figure 3. LX2080A Block diagram



1.1 Device selection

This table shows how to set the TEST_SEL_B and the cfg_svr[0:1] pins to select between LX2160A, LX2120A, and LX2080A.

Table 1. Device Personality Selection

Personality	TEST_SEL_B	cfg_svr0 (primary signal XSPI1_A_CS0_B)	cfg_svr1 (primary signal XSPI1_A_CS1_B)
LX2160A	1	1	1
LX2120A	0	1	1
LX2080A	1	0	1

2 PIN ASSIGNMENTS

2.1 1517 ball layout diagrams

This figure shows the complete view of the LX2160A BGA ball map diagram. Figure 5, Figure 6, Figure 7, and Figure 8 show quadrant views.

Figure 4. Complete BGA Map for the LX2160A

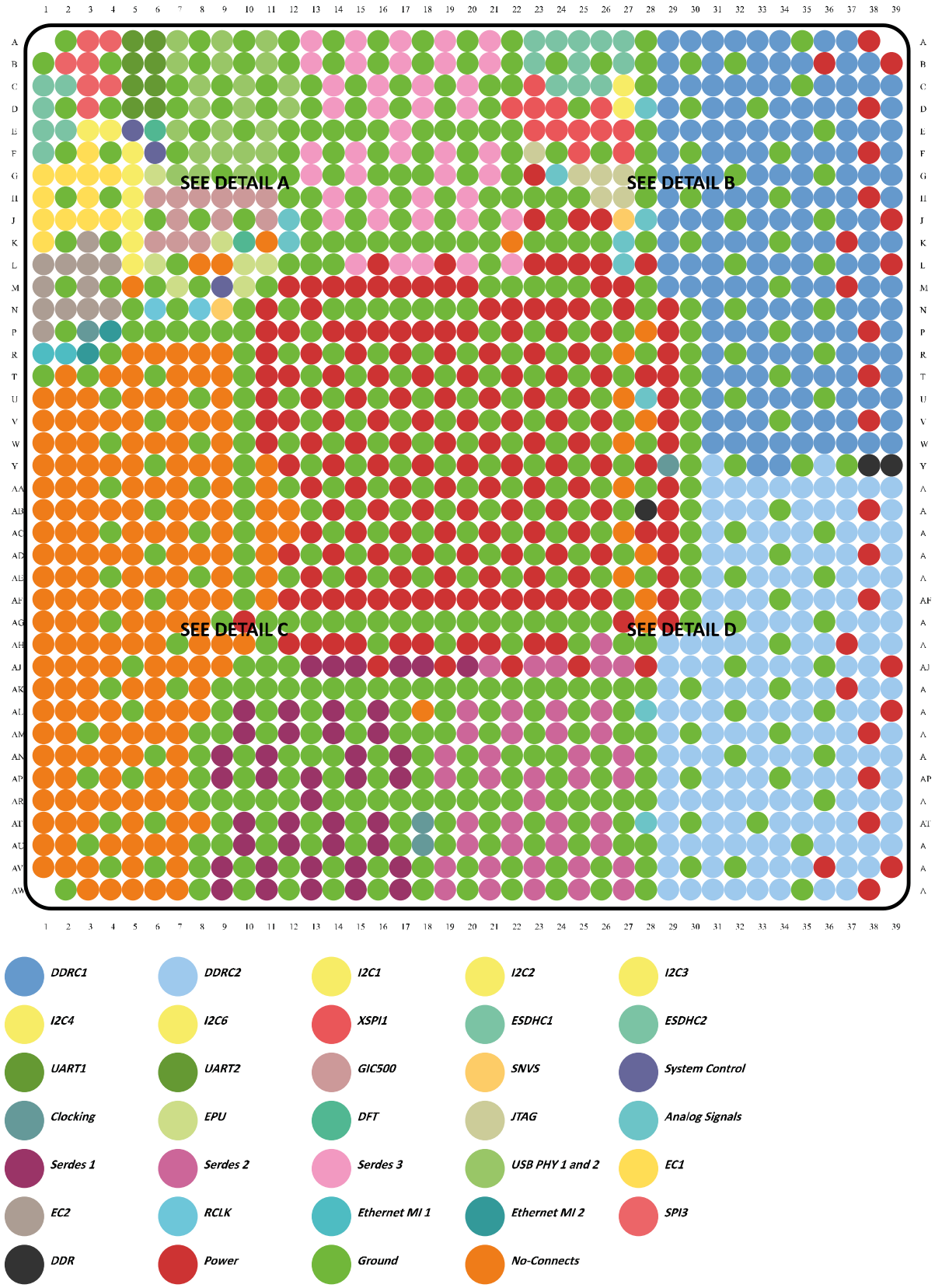


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Figure 5. Detail A

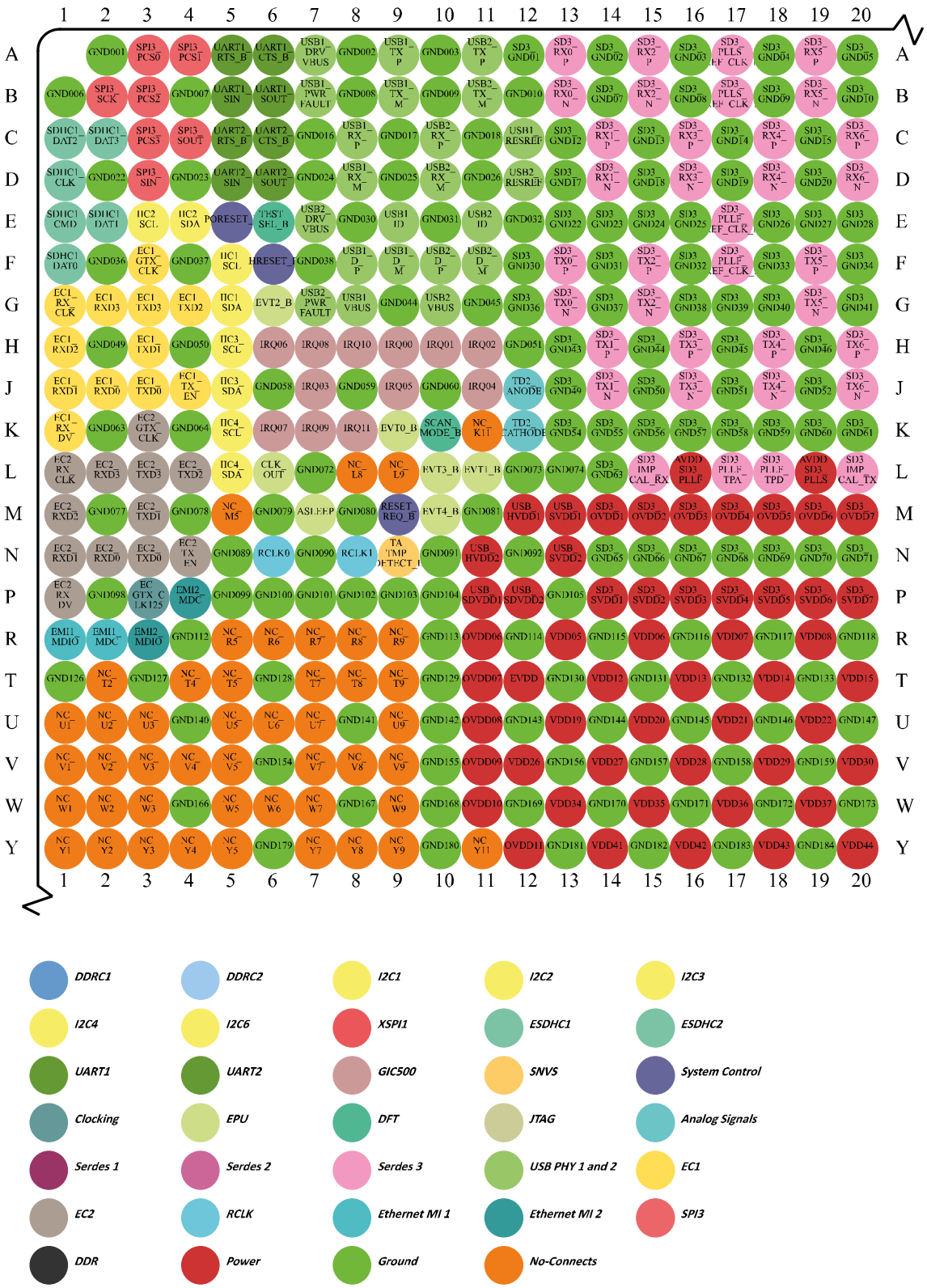


Figure 6. Detail B

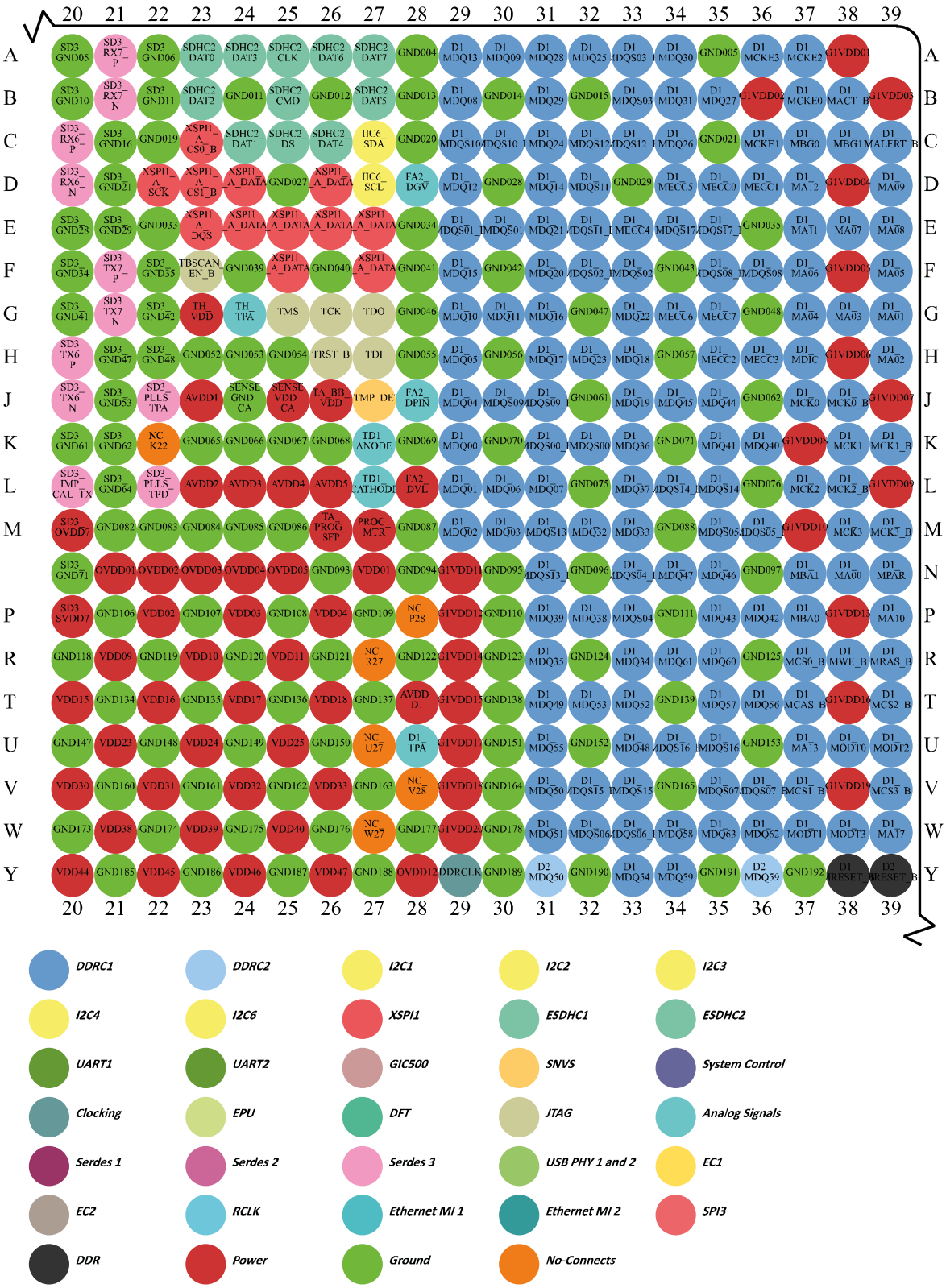


Figure 7. Detail C

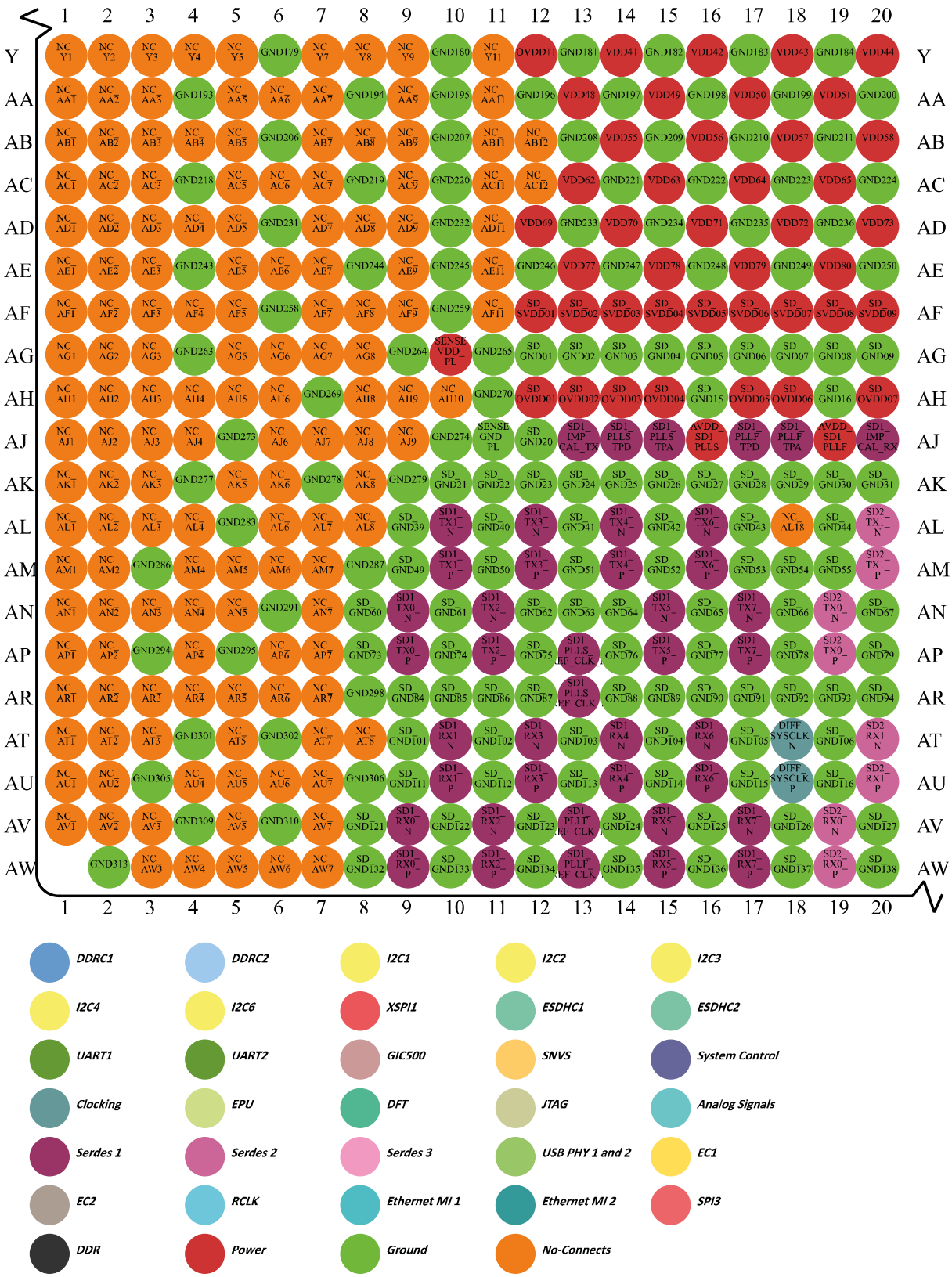
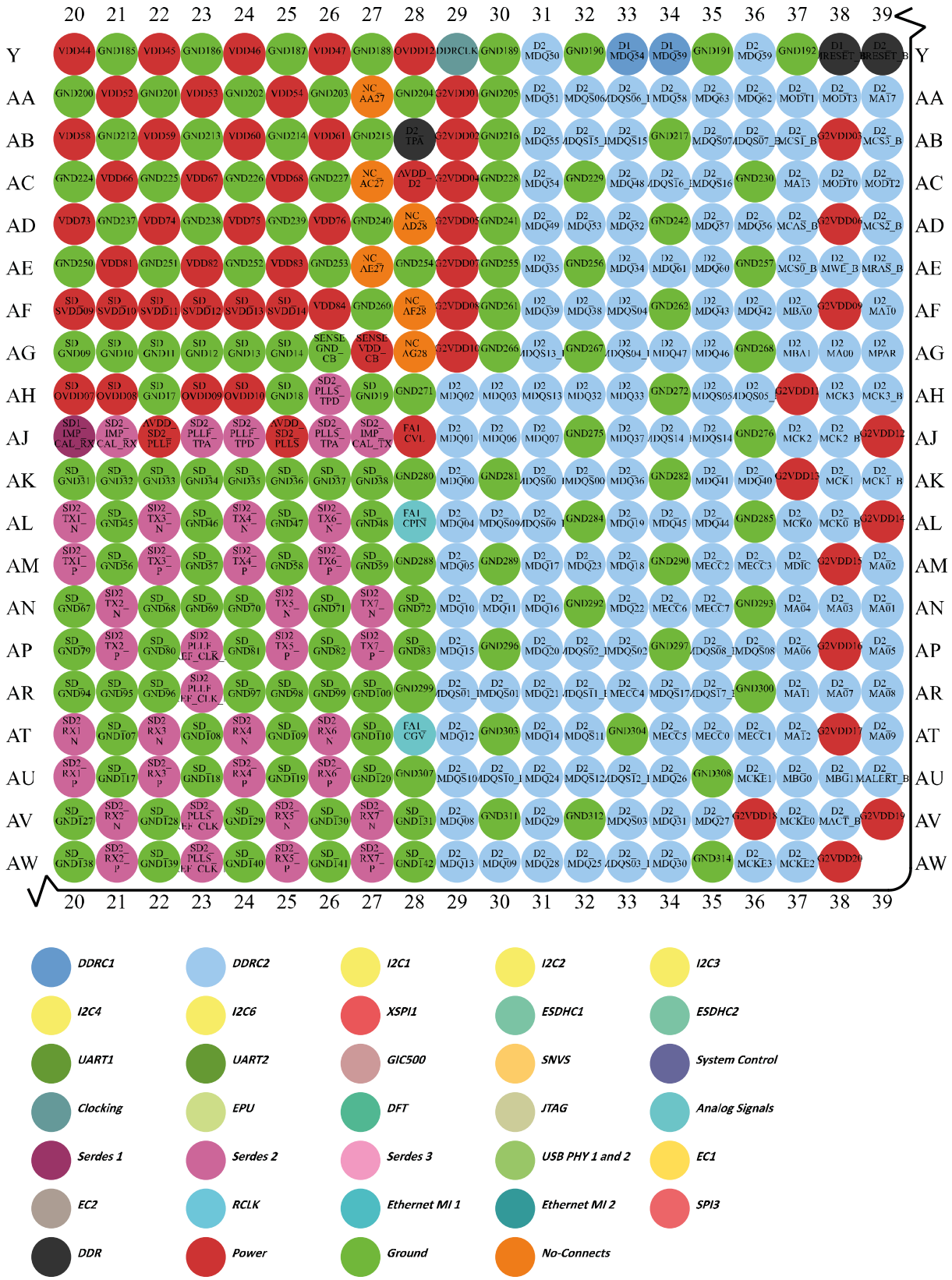


Figure 8. Detail D



2.2 Pinout list

This table provides the pinout listing for the LX2160A by bus. Primary functions are **bolded** in the table.

Table 2. Pinout list by bus

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	N38	O	$G1V_{DD}$	---
D1_MA01	Address	G39	O	$G1V_{DD}$	---
D1_MA02	Address	H39	O	$G1V_{DD}$	---
D1_MA03	Address	G38	O	$G1V_{DD}$	---
D1_MA04	Address	G37	O	$G1V_{DD}$	---
D1_MA05	Address	F39	O	$G1V_{DD}$	---
D1_MA06	Address	F37	O	$G1V_{DD}$	---
D1_MA07	Address	E38	O	$G1V_{DD}$	---
D1_MA08	Address	E39	O	$G1V_{DD}$	---
D1_MA09	Address	D39	O	$G1V_{DD}$	---
D1_MA10	Address	P39	O	$G1V_{DD}$	---
D1_MA11	Address	E37	O	$G1V_{DD}$	---
D1_MA12	Address	D37	O	$G1V_{DD}$	---
D1_MA13	Address	U37	O	$G1V_{DD}$	---
D1_MA17	Address	W39	O	$G1V_{DD}$	---
D1_MACT_B	Activate	B38	O	$G1V_{DD}$	---
D1_MALERT_B	Alert	C39	I	$G1V_{DD}$	1, 16
D1_MBA0	Bank Select	P37	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	N37	O	$G1V_{DD}$	---
D1_MBG0	Bank Group	C37	O	$G1V_{DD}$	---
D1_MBG1	Bank Group	C38	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	T37	O	$G1V_{DD}$	---
D1_MCK0	Clock	J37	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	J38	O	$G1V_{DD}$	---
D1_MCK1	Clock	K38	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	K39	O	$G1V_{DD}$	---
D1_MCK2	Clock	L37	O	$G1V_{DD}$	---
D1_MCK2_B	Clock Complement	L38	O	$G1V_{DD}$	---
D1_MCK3	Clock	M38	O	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MCK3_B	Clock Complement	M39	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	B37	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	C36	O	$G1V_{DD}$	2
D1_MCKE2	Clock Enable	A37	O	$G1V_{DD}$	2
D1_MCKE3	Clock Enable	A36	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	R37	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	V37	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select / MCID[0]	T39	O	$G1V_{DD}$	---
D1_MCS3_B	Chip Select / MCID[1]	V39	O	$G1V_{DD}$	---
D1_MDIC	Driver Impedence Calibration	H37	IO	$G1V_{DD}$	3
D1_MDQ00	Data	K29	IO	$G1V_{DD}$	---
D1_MDQ01	Data	L29	IO	$G1V_{DD}$	---
D1_MDQ02	Data	M29	IO	$G1V_{DD}$	---
D1_MDQ03	Data	M30	IO	$G1V_{DD}$	---
D1_MDQ04	Data	J29	IO	$G1V_{DD}$	---
D1_MDQ05	Data	H29	IO	$G1V_{DD}$	---
D1_MDQ06	Data	L30	IO	$G1V_{DD}$	---
D1_MDQ07	Data	L31	IO	$G1V_{DD}$	---
D1_MDQ08	Data	B29	IO	$G1V_{DD}$	---
D1_MDQ09	Data	A30	IO	$G1V_{DD}$	---
D1_MDQ10	Data	G29	IO	$G1V_{DD}$	---
D1_MDQ11	Data	G30	IO	$G1V_{DD}$	---
D1_MDQ12	Data	D29	IO	$G1V_{DD}$	---
D1_MDQ13	Data	A29	IO	$G1V_{DD}$	---
D1_MDQ14	Data	D31	IO	$G1V_{DD}$	---
D1_MDQ15	Data	F29	IO	$G1V_{DD}$	---
D1_MDQ16	Data	G31	IO	$G1V_{DD}$	---
D1_MDQ17	Data	H31	IO	$G1V_{DD}$	---
D1_MDQ18	Data	H33	IO	$G1V_{DD}$	---
D1_MDQ19	Data	J33	IO	$G1V_{DD}$	---
D1_MDQ20	Data	F31	IO	$G1V_{DD}$	---
D1_MDQ21	Data	E31	IO	$G1V_{DD}$	---
D1_MDQ22	Data	G33	IO	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQ23	Data	H32	IO	$G1V_{DD}$	---
D1_MDQ24	Data	C31	IO	$G1V_{DD}$	---
D1_MDQ25	Data	A32	IO	$G1V_{DD}$	---
D1_MDQ26	Data	C34	IO	$G1V_{DD}$	---
D1_MDQ27	Data	B35	IO	$G1V_{DD}$	---
D1_MDQ28	Data	A31	IO	$G1V_{DD}$	---
D1_MDQ29	Data	B31	IO	$G1V_{DD}$	---
D1_MDQ30	Data	A34	IO	$G1V_{DD}$	---
D1_MDQ31	Data	B34	IO	$G1V_{DD}$	---
D1_MDQ32	Data	M32	IO	$G1V_{DD}$	---
D1_MDQ33	Data	M33	IO	$G1V_{DD}$	---
D1_MDQ34	Data	R33	IO	$G1V_{DD}$	---
D1_MDQ35	Data	R31	IO	$G1V_{DD}$	---
D1_MDQ36	Data	K33	IO	$G1V_{DD}$	---
D1_MDQ37	Data	L33	IO	$G1V_{DD}$	---
D1_MDQ38	Data	P32	IO	$G1V_{DD}$	---
D1_MDQ39	Data	P31	IO	$G1V_{DD}$	---
D1_MDQ40	Data	K36	IO	$G1V_{DD}$	---
D1_MDQ41	Data	K35	IO	$G1V_{DD}$	---
D1_MDQ42	Data	P36	IO	$G1V_{DD}$	---
D1_MDQ43	Data	P35	IO	$G1V_{DD}$	---
D1_MDQ44	Data	J35	IO	$G1V_{DD}$	---
D1_MDQ45	Data	J34	IO	$G1V_{DD}$	---
D1_MDQ46	Data	N35	IO	$G1V_{DD}$	---
D1_MDQ47	Data	N34	IO	$G1V_{DD}$	---
D1_MDQ48	Data	U33	IO	$G1V_{DD}$	---
D1_MDQ49	Data	T31	IO	$G1V_{DD}$	---
D1_MDQ50	Data	V31	IO	$G1V_{DD}$	---
D1_MDQ51	Data	W31	IO	$G1V_{DD}$	---
D1_MDQ52	Data	T33	IO	$G1V_{DD}$	---
D1_MDQ53	Data	T32	IO	$G1V_{DD}$	---
D1_MDQ54	Data	Y33	IO	$G1V_{DD}$	---
D1_MDQ55	Data	U31	IO	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQ56	Data	T36	IO	$G1V_{DD}$	---
D1_MDQ57	Data	T35	IO	$G1V_{DD}$	---
D1_MDQ58	Data	W34	IO	$G1V_{DD}$	---
D1_MDQ59	Data	Y34	IO	$G1V_{DD}$	---
D1_MDQ60	Data	R35	IO	$G1V_{DD}$	---
D1_MDQ61	Data	R34	IO	$G1V_{DD}$	---
D1_MDQ62	Data	W36	IO	$G1V_{DD}$	---
D1_MDQ63	Data	W35	IO	$G1V_{DD}$	---
D1_MDQS00	Data Strobe	K32	IO	$G1V_{DD}$	---
D1_MDQS00_B	Data Strobe	K31	IO	$G1V_{DD}$	---
D1_MDQS01	Data Strobe	E30	IO	$G1V_{DD}$	---
D1_MDQS01_B	Data Strobe	E29	IO	$G1V_{DD}$	---
D1_MDQS02	Data Strobe	F33	IO	$G1V_{DD}$	---
D1_MDQS02_B	Data Strobe	F32	IO	$G1V_{DD}$	---
D1_MDQS03	Data Strobe	B33	IO	$G1V_{DD}$	---
D1_MDQS03_B	Data Strobe	A33	IO	$G1V_{DD}$	---
D1_MDQS04	Data Strobe	P33	IO	$G1V_{DD}$	---
D1_MDQS04_B	Data Strobe	N33	IO	$G1V_{DD}$	---
D1_MDQS05	Data Strobe	M35	IO	$G1V_{DD}$	---
D1_MDQS05_B	Data Strobe	M36	IO	$G1V_{DD}$	---
D1_MDQS06	Data Strobe	W32	IO	$G1V_{DD}$	---
D1_MDQS06_B	Data Strobe	W33	IO	$G1V_{DD}$	---
D1_MDQS07	Data Strobe	V35	IO	$G1V_{DD}$	---
D1_MDQS07_B	Data Strobe	V36	IO	$G1V_{DD}$	---
D1_MDQS08	Data Strobe	F36	IO	$G1V_{DD}$	---
D1_MDQS08_B	Data Strobe	F35	IO	$G1V_{DD}$	---
D1_MDM00_B/D1_MDBI00_B/ D1_MDQS09	Data Mask/Data Bus Inversion/Data Strobe (x4)	J30	IO	$G1V_{DD}$	---
D1_MDQS09_B	Data Strobe (x4 support)	J31	IO	$G1V_{DD}$	---
D1_MDM01_B/D1_MDBI01_B/ D1_MDQS10	Data Mask/Data Bus Inversion/Data Strobe (x4)	C29	IO	$G1V_{DD}$	---
D1_MDQS10_B	Data Strobe (x4 support)	C30	IO	$G1V_{DD}$	---
D1_MDM02_B/D1_MDBI02_B/ D1_MDQS11	Data Mask/Data Bus Inversion/Data Strobe (x4)	D32	IO	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQS11_B	Data Strobe (x4 support)	E32	IO	$G1V_{DD}$	---
D1_MDM03_B/D1_MDBI03_B/ D1_MDQS12	Data Mask/Data Bus Inversion/Data Strobe (x4)	C32	IO	$G1V_{DD}$	---
D1_MDQS12_B	Data Strobe (x4 support)	C33	IO	$G1V_{DD}$	---
D1_MDM04_B/D1_MDBI04_B/ D1_MDQS13	Data Mask/Data Bus Inversion/Data Strobe (x4)	M31	IO	$G1V_{DD}$	---
D1_MDQS13_B	Data Strobe (x4 support)	N31	IO	$G1V_{DD}$	---
D1_MDM05_B/D1_MDBI05_B/ D1_MDQS14	Data Mask/Data Bus Inversion/Data Strobe (x4)	L35	IO	$G1V_{DD}$	---
D1_MDQS14_B	Data Strobe (x4 support)	L34	IO	$G1V_{DD}$	---
D1_MDM06_B/D1_MDBI06_B/ D1_MDQS15	Data Mask/Data Bus Inversion/Data Strobe (x4)	V33	IO	$G1V_{DD}$	---
D1_MDQS15_B	Data Strobe (x4 support)	V32	IO	$G1V_{DD}$	---
D1_MDM07_B/D1_MDBI07_B/ D1_MDQS16	Data Mask/Data Bus Inversion/Data Strobe (x4)	U35	IO	$G1V_{DD}$	---
D1_MDQS16_B	Data Strobe (x4 support)	U34	IO	$G1V_{DD}$	---
D1_MDM08_B/D1_MDBI08_B/ D1_MDQS17	Data Mask/Data Bus Inversion/Data Strobe (x4)	E34	IO	$G1V_{DD}$	---
D1_MDQS17_B	Data Strobe (x4 support)	E35	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	D35	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	D36	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	H35	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	H36	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	E33	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	D34	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	G34	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	G35	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	U38	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination / MCID[2]	W37	O	$G1V_{DD}$	2
D1_MODT2	On Die Termination	U39	O	$G1V_{DD}$	2
D1_MODT3	On Die Termination	W38	O	$G1V_{DD}$	2
D1_MPAR	Address Parity Out	N39	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	R39	O	$G1V_{DD}$	---
D1_MRESET_B	Reset to DRAM	Y38	O	$G1V_{DD}$	16
D1_MWE_B	Write Enable / MA[14]	R38	O	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DDR SDRAM Memory Interface 2					
D2_MA00	Address	AG38	O	$G2V_{DD}$	---
D2_MA01	Address	AN39	O	$G2V_{DD}$	---
D2_MA02	Address	AM39	O	$G2V_{DD}$	---
D2_MA03	Address	AN38	O	$G2V_{DD}$	---
D2_MA04	Address	AN37	O	$G2V_{DD}$	---
D2_MA05	Address	AP39	O	$G2V_{DD}$	---
D2_MA06	Address	AP37	O	$G2V_{DD}$	---
D2_MA07	Address	AR38	O	$G2V_{DD}$	---
D2_MA08	Address	AR39	O	$G2V_{DD}$	---
D2_MA09	Address	AT39	O	$G2V_{DD}$	---
D2_MA10	Address	AF39	O	$G2V_{DD}$	---
D2_MA11	Address	AR37	O	$G2V_{DD}$	---
D2_MA12	Address	AT37	O	$G2V_{DD}$	---
D2_MA13	Address	AC37	O	$G2V_{DD}$	---
D2_MA17	Address	AA39	O	$G2V_{DD}$	---
D2_MACT_B	Activate	AV38	O	$G2V_{DD}$	---
D2_MALERT_B	Alert	AU39	I	$G2V_{DD}$	1, 16
D2_MBA0	Bank Select	AF37	O	$G2V_{DD}$	---
D2_MBA1	Bank Select	AG37	O	$G2V_{DD}$	---
D2_MBG0	Bank Group	AU37	O	$G2V_{DD}$	---
D2_MBG1	Bank Group	AU38	O	$G2V_{DD}$	---
D2_MCAS_B	Column Address Strobe / MA[15]	AD37	O	$G2V_{DD}$	---
D2_MCK0	Clock	AL37	O	$G2V_{DD}$	---
D2_MCK0_B	Clock Complement	AL38	O	$G2V_{DD}$	---
D2_MCK1	Clock	AK38	O	$G2V_{DD}$	---
D2_MCK1_B	Clock Complement	AK39	O	$G2V_{DD}$	---
D2_MCK2	Clock	AJ37	O	$G2V_{DD}$	---
D2_MCK2_B	Clock Complement	AJ38	O	$G2V_{DD}$	---
D2_MCK3	Clock	AH38	O	$G2V_{DD}$	---
D2_MCK3_B	Clock Complement	AH39	O	$G2V_{DD}$	---
D2_MCKE0	Clock Enable	AV37	O	$G2V_{DD}$	2
D2_MCKE1	Clock Enable	AU36	O	$G2V_{DD}$	2

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D2_MCKE2	Clock Enable	AW37	O	$G2V_{DD}$	2
D2_MCKE3	Clock Enable	AW36	O	$G2V_{DD}$	2
D2_MCS0_B	Chip Select	AE37	O	$G2V_{DD}$	---
D2_MCS1_B	Chip Select	AB37	O	$G2V_{DD}$	---
D2_MCS2_B	Chip Select / MCID[0]	AD39	O	$G2V_{DD}$	---
D2_MCS3_B	Chip Select / MCID[1]	AB39	O	$G2V_{DD}$	---
D2_MDIC	Driver Impedence Calibration	AM37	IO	$G2V_{DD}$	3
D2_MDQ00	Data	AK29	IO	$G2V_{DD}$	---
D2_MDQ01	Data	AJ29	IO	$G2V_{DD}$	---
D2_MDQ02	Data	AH29	IO	$G2V_{DD}$	---
D2_MDQ03	Data	AH30	IO	$G2V_{DD}$	---
D2_MDQ04	Data	AL29	IO	$G2V_{DD}$	---
D2_MDQ05	Data	AM29	IO	$G2V_{DD}$	---
D2_MDQ06	Data	AJ30	IO	$G2V_{DD}$	---
D2_MDQ07	Data	AJ31	IO	$G2V_{DD}$	---
D2_MDQ08	Data	AV29	IO	$G2V_{DD}$	---
D2_MDQ09	Data	AW30	IO	$G2V_{DD}$	---
D2_MDQ10	Data	AN29	IO	$G2V_{DD}$	---
D2_MDQ11	Data	AN30	IO	$G2V_{DD}$	---
D2_MDQ12	Data	AT29	IO	$G2V_{DD}$	---
D2_MDQ13	Data	AW29	IO	$G2V_{DD}$	---
D2_MDQ14	Data	AT31	IO	$G2V_{DD}$	---
D2_MDQ15	Data	AP29	IO	$G2V_{DD}$	---
D2_MDQ16	Data	AN31	IO	$G2V_{DD}$	---
D2_MDQ17	Data	AM31	IO	$G2V_{DD}$	---
D2_MDQ18	Data	AM33	IO	$G2V_{DD}$	---
D2_MDQ19	Data	AL33	IO	$G2V_{DD}$	---
D2_MDQ20	Data	AP31	IO	$G2V_{DD}$	---
D2_MDQ21	Data	AR31	IO	$G2V_{DD}$	---
D2_MDQ22	Data	AN33	IO	$G2V_{DD}$	---
D2_MDQ23	Data	AM32	IO	$G2V_{DD}$	---
D2_MDQ24	Data	AU31	IO	$G2V_{DD}$	---
D2_MDQ25	Data	AW32	IO	$G2V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D2_MDQ26	Data	AU34	IO	$G2V_{DD}$	---
D2_MDQ27	Data	AV35	IO	$G2V_{DD}$	---
D2_MDQ28	Data	AW31	IO	$G2V_{DD}$	---
D2_MDQ29	Data	AV31	IO	$G2V_{DD}$	---
D2_MDQ30	Data	AW34	IO	$G2V_{DD}$	---
D2_MDQ31	Data	AV34	IO	$G2V_{DD}$	---
D2_MDQ32	Data	AH32	IO	$G2V_{DD}$	---
D2_MDQ33	Data	AH33	IO	$G2V_{DD}$	---
D2_MDQ34	Data	AE33	IO	$G2V_{DD}$	---
D2_MDQ35	Data	AE31	IO	$G2V_{DD}$	---
D2_MDQ36	Data	AK33	IO	$G2V_{DD}$	---
D2_MDQ37	Data	AJ33	IO	$G2V_{DD}$	---
D2_MDQ38	Data	AF32	IO	$G2V_{DD}$	---
D2_MDQ39	Data	AF31	IO	$G2V_{DD}$	---
D2_MDQ40	Data	AK36	IO	$G2V_{DD}$	---
D2_MDQ41	Data	AK35	IO	$G2V_{DD}$	---
D2_MDQ42	Data	AF36	IO	$G2V_{DD}$	---
D2_MDQ43	Data	AF35	IO	$G2V_{DD}$	---
D2_MDQ44	Data	AL35	IO	$G2V_{DD}$	---
D2_MDQ45	Data	AL34	IO	$G2V_{DD}$	---
D2_MDQ46	Data	AG35	IO	$G2V_{DD}$	---
D2_MDQ47	Data	AG34	IO	$G2V_{DD}$	---
D2_MDQ48	Data	AC33	IO	$G2V_{DD}$	---
D2_MDQ49	Data	AD31	IO	$G2V_{DD}$	---
D2_MDQ50	Data	Y31	IO	$G2V_{DD}$	---
D2_MDQ51	Data	AA31	IO	$G2V_{DD}$	---
D2_MDQ52	Data	AD33	IO	$G2V_{DD}$	---
D2_MDQ53	Data	AD32	IO	$G2V_{DD}$	---
D2_MDQ54	Data	AC31	IO	$G2V_{DD}$	---
D2_MDQ55	Data	AB31	IO	$G2V_{DD}$	---
D2_MDQ56	Data	AD36	IO	$G2V_{DD}$	---
D2_MDQ57	Data	AD35	IO	$G2V_{DD}$	---
D2_MDQ58	Data	AA34	IO	$G2V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D2_MDQ59	Data	Y36	IO	$G2V_{DD}$	---
D2_MDQ60	Data	AE35	IO	$G2V_{DD}$	---
D2_MDQ61	Data	AE34	IO	$G2V_{DD}$	---
D2_MDQ62	Data	AA36	IO	$G2V_{DD}$	---
D2_MDQ63	Data	AA35	IO	$G2V_{DD}$	---
D2_MDQS00	Data Strobe	AK32	IO	$G2V_{DD}$	---
D2_MDQS00_B	Data Strobe	AK31	IO	$G2V_{DD}$	---
D2_MDQS01	Data Strobe	AR30	IO	$G2V_{DD}$	---
D2_MDQS01_B	Data Strobe	AR29	IO	$G2V_{DD}$	---
D2_MDQS02	Data Strobe	AP33	IO	$G2V_{DD}$	---
D2_MDQS02_B	Data Strobe	AP32	IO	$G2V_{DD}$	---
D2_MDQS03	Data Strobe	AV33	IO	$G2V_{DD}$	---
D2_MDQS03_B	Data Strobe	AW33	IO	$G2V_{DD}$	---
D2_MDQS04	Data Strobe	AF33	IO	$G2V_{DD}$	---
D2_MDQS04_B	Data Strobe	AG33	IO	$G2V_{DD}$	---
D2_MDQS05	Data Strobe	AH35	IO	$G2V_{DD}$	---
D2_MDQS05_B	Data Strobe	AH36	IO	$G2V_{DD}$	---
D2_MDQS06	Data Strobe	AA32	IO	$G2V_{DD}$	---
D2_MDQS06_B	Data Strobe	AA33	IO	$G2V_{DD}$	---
D2_MDQS07	Data Strobe	AB35	IO	$G2V_{DD}$	---
D2_MDQS07_B	Data Strobe	AB36	IO	$G2V_{DD}$	---
D2_MDQS08	Data Strobe	AP36	IO	$G2V_{DD}$	---
D2_MDQS08_B	Data Strobe	AP35	IO	$G2V_{DD}$	---
D2_MDM00_B/D2_MDBI00_B/ D2_MDQS09	Data Mask/Data Bus Inversion/Data Strobe (x4)	AL30	IO	$G2V_{DD}$	---
D2_MDQS09_B	Data Strobe (x4 support)	AL31	IO	$G2V_{DD}$	---
D2_MDM01_B/D2_MDBI01_B/ D2_MDQS10	Data Mask/Data Bus Inversion/Data Strobe (x4)	AU29	IO	$G2V_{DD}$	---
D2_MDQS10_B	Data Strobe (x4 support)	AU30	IO	$G2V_{DD}$	---
D2_MDM02_B/D2_MDBI02_B/ D2_MDQS11	Data Mask/Data Bus Inversion/Data Strobe (x4)	AT32	IO	$G2V_{DD}$	---
D2_MDQS11_B	Data Strobe (x4 support)	AR32	IO	$G2V_{DD}$	---
D2_MDM03_B/D2_MDBI03_B/ D2_MDQS12	Data Mask/Data Bus Inversion/Data Strobe (x4)	AU32	IO	$G2V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D2_MDQS12_B	Data Strobe (x4 support)	AU33	IO	$G2V_{DD}$	---
D2_MDM04_B/D2_MDBI04_B/ D2_MDQS13	Data Mask/Data Bus Inversion/Data Strobe (x4)	AH31	IO	$G2V_{DD}$	---
D2_MDQS13_B	Data Strobe (x4 support)	AG31	IO	$G2V_{DD}$	---
D2_MDM05_B/D2_MDBI05_B/ D2_MDQS14	Data Mask/Data Bus Inversion/Data Strobe (x4)	AJ35	IO	$G2V_{DD}$	---
D2_MDQS14_B	Data Strobe (x4 support)	AJ34	IO	$G2V_{DD}$	---
D2_MDM06_B/D2_MDBI06_B/ D2_MDQS15	Data Mask/Data Bus Inversion/Data Strobe (x4)	AB33	IO	$G2V_{DD}$	---
D2_MDQS15_B	Data Strobe (x4 support)	AB32	IO	$G2V_{DD}$	---
D2_MDM07_B/D2_MDBI07_B/ D2_MDQS16	Data Mask/Data Bus Inversion/Data Strobe (x4)	AC35	IO	$G2V_{DD}$	---
D2_MDQS16_B	Data Strobe (x4 support)	AC34	IO	$G2V_{DD}$	---
D2_MDM08_B/D2_MDBI08_B/ D2_MDQS17	Data Mask/Data Bus Inversion/Data Strobe (x4)	AR34	IO	$G2V_{DD}$	---
D2_MDQS17_B	Data Strobe (x4 support)	AR35	IO	$G2V_{DD}$	---
D2_MECC0	Error Correcting Code	AT35	IO	$G2V_{DD}$	---
D2_MECC1	Error Correcting Code	AT36	IO	$G2V_{DD}$	---
D2_MECC2	Error Correcting Code	AM35	IO	$G2V_{DD}$	---
D2_MECC3	Error Correcting Code	AM36	IO	$G2V_{DD}$	---
D2_MECC4	Error Correcting Code	AR33	IO	$G2V_{DD}$	---
D2_MECC5	Error Correcting Code	AT34	IO	$G2V_{DD}$	---
D2_MECC6	Error Correcting Code	AN34	IO	$G2V_{DD}$	---
D2_MECC7	Error Correcting Code	AN35	IO	$G2V_{DD}$	---
D2_MODT0	On Die Termination	AC38	O	$G2V_{DD}$	2
D2_MODT1	On Die Termination / MCID[2]	AA37	O	$G2V_{DD}$	2
D2_MODT2	On Die Termination	AC39	O	$G2V_{DD}$	2
D2_MODT3	On Die Termination	AA38	O	$G2V_{DD}$	2
D2_MPAR	Address Parity Out	AG39	O	$G2V_{DD}$	---
D2_MRAS_B	Row Address Strobe / MA[16]	AE39	O	$G2V_{DD}$	---
D2_MRESET_B	Reset to DRAM	Y39	O	$G2V_{DD}$	16
D2_MWE_B	Write Enable / MA[14]	AE38	O	$G2V_{DD}$	---
I2C1					
IIC1_SCL /GPIO1_DAT03	Serial Clock	F5	IO	OV_{DD}	5, 6
IIC1_SDA /GPIO1_DAT02	Serial Data	G5	IO	OV_{DD}	5, 6

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
I2C2					
IIC2_SCL /GPIO1_DAT31 / FTM1_CH0 /SDHC1_CD_B	Serial Clock	E3	IO	OV_{DD}	5, 6
IIC2_SDA /GPIO1_DAT30 / FTM2_CH0/SDHC1_WP	Serial Data	E4	IO	OV_{DD}	5, 6
I2C3					
IIC3_SCL /GPIO1_DAT29 / CAN1_TX /EVT5_B	Serial Clock	H5	IO	OV_{DD}	5, 6
IIC3_SDA /GPIO1_DAT28 / CAN1_RX/EVT6_B	Serial Data	J5	IO	OV_{DD}	5, 6
I2C4					
IIC4_SCL /GPIO1_DAT27 / CAN2_TX /EVT7_B	Serial Clock	K5	IO	OV_{DD}	5, 6
IIC4_SDA /GPIO1_DAT26 / CAN2_RX/EVT8_B	Serial Data	L5	IO	OV_{DD}	5, 6
I2C5					
IIC5_SCL/ SPI3_SOUT / GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT	Serial Clock	C4	IO	OV_{DD}	5, 6
IIC5_SDA/ SPI3_SIN / GPIO1_DAT24 / SDHC1_CLK_SYNC_IN	Serial Data	D3	IO	OV_{DD}	5, 6
I2C6					
IIC6_SCL /GPIO1_DAT23 / SDHC2_CLK_SYNC_OUT	Serial Clock	D27	IO	OV_{DD}	5, 6
IIC6_SDA /GPIO1_DAT22 / SDHC2_CLK_SYNC_IN	Serial Data	C27	IO	OV_{DD}	5, 6
I2C7					
IIC7_SCL/ SDHC2_DAT5 / GPIO2_DAT16 / XSPI1_B_DATA5	Serial Clock	B27	IO	OV_{DD}	5, 6
IIC7_SDA/ SDHC2_DAT4 / GPIO2_DAT15 / XSPI1_B_DATA4	Serial Data	C26	IO	OV_{DD}	5, 6
I2C8					
IIC8_SCL/ SDHC2_DAT7 / GPIO2_DAT18 / XSPI1_B_DATA7	Serial Clock	A27	IO	OV_{DD}	5, 6
IIC8_SDA/ SDHC2_DAT6 / GPIO2_DAT17 / XSPI1_B_DATA6	Serial Data	A26	IO	OV_{DD}	5, 6
XSPI1					
XSPI1_A_CS0_B / GPIO2_DAT21	Chip Select	C23	O	OV_{DD}	1
XSPI1_A_CS1_B / GPIO2_DAT20	Chip Select	D23	O	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_A_DATA0 / GPIO2_DAT24	Data	F25	IO	OV_{DD}	---
XSPI1_A_DATA1 / GPIO2_DAT25	Data	E24	IO	OV_{DD}	---
XSPI1_A_DATA2 / GPIO2_DAT26	Data	E26	IO	OV_{DD}	---
XSPI1_A_DATA3 / GPIO2_DAT27	Data	E27	IO	OV_{DD}	---
XSPI1_A_DATA4 / GPIO2_DAT28	Data	F27	IO	OV_{DD}	---
XSPI1_A_DATA5 / GPIO2_DAT29	Data	D26	IO	OV_{DD}	---
XSPI1_A_DATA6 / GPIO2_DAT30	Data	E25	IO	OV_{DD}	---
XSPI1_A_DATA7 / GPIO2_DAT31	Data	D24	IO	OV_{DD}	---
XSPI1_A_DQS / GPIO2_DAT23	Data Strobe	E23	IO	OV_{DD}	---
XSPI1_A_SCK / GPIO2_DAT22 /cfg_eng_use0	Clock	D22	O	OV_{DD}	1
XSPI1_B_CS1_B/ SDHC2_CMD / GPIO2_DAT19/SPI2_SOUT	Chip Select	B25	O	OV_{DD}	1
XSPI1_B_DATA0/ SDHC2_DAT0 / GPIO2_DAT11 /SPI2_SIN /cfg_gpinput4	Data	A23	IO	OV_{DD}	
XSPI1_B_DATA1/ SDHC2_DAT1 / GPIO2_DAT12 /SPI2_PCS2 / cfg_gpinput5	Data	C24	IO	OV_{DD}	
XSPI1_B_DATA2/ SDHC2_DAT2 / GPIO2_DAT13 /SPI2_PCS1 / cfg_gpinput6	Data	B23	IO	OV_{DD}	
XSPI1_B_DATA3/ SDHC2_DAT3 / GPIO2_DAT14 /SPI2_PCS0 / cfg_gpinput7	Data	A24	IO	OV_{DD}	
XSPI1_B_DATA4/ SDHC2_DAT4 / GPIO2_DAT15/IIC7_SDA	Data	C26	IO	OV_{DD}	---
XSPI1_B_DATA5/ SDHC2_DAT5 / GPIO2_DAT16/IIC7_SCL	Data	B27	IO	OV_{DD}	---
XSPI1_B_DATA6/ SDHC2_DAT6 / GPIO2_DAT17/IIC8_SDA	Data	A26	IO	OV_{DD}	---
XSPI1_B_DATA7/ SDHC2_DAT7 / GPIO2_DAT18/IIC8_SCL	Data	A27	IO	OV_{DD}	---
XSPI1_B_DQS/ SDHC2_DS / GPIO2_DAT10/SPI2_PCS3	Data Strobe	C25	IO	OV_{DD}	---
XSPI1_B_SCK/ SDHC2_CLK / GPIO2_DAT09/SPI2_SCK	Clock	A25	O	OV_{DD}	1
eSDHC 1					
SDHC1_CD_B/ IIC2_SCL / GPIO1_DAT31/FTM1_CH0	Card Detect	E3	I	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC1_CLK /GPIO1_DAT16 / SPI1_SCK	Host to Card Clock	D1	O	EV_{DD}	1
SDHC1_CLK_SYNC_IN/ SPI3_SIN /GPIO1_DAT24 / IIC5_SDA	Input Synchronous Clock	D3	I	OV_{DD}	1
SDHC1_CLK_SYNC_OUT/ SPI3_SOUT /GPIO1_DAT25 / IIC5_SCL	Output Synchronuous Clock	C4	O	OV_{DD}	1
SDHC1_CMD / GPIO1_DAT21 /SPI1_SOUT	Command/Response	E1	IO	EV_{DD}	5
SDHC1_CMD_DIR/ SPI3_PCS1 /GPIO1_DAT14 / SDHC1_DAT5	Command Direction	A4	O	OV_{DD}	1
SDHC1_DAT0 / GPIO1_DAT17 /SPI1_SIN / cfg_gpinput0	Data	F1	IO	EV_{DD}	5
SDHC1_DAT0_DIR/ SPI3_PCS2 /GPIO1_DAT13 / SDHC1_DAT6	DAT0 Direction	B3	O	OV_{DD}	1
SDHC1_DAT1 / GPIO1_DAT18 /SPI1_PCS2 / cfg_gpinput1	Data	E2	IO	EV_{DD}	5
SDHC1_DAT123_DIR/ SPI3_PCS3 /GPIO1_DAT12 / SDHC1_DAT7	DATA[1:3] Direction	C3	O	OV_{DD}	1
SDHC1_DAT2 / GPIO1_DAT19 /SPI1_PCS1 / cfg_gpinput2	Data	C1	IO	EV_{DD}	5
SDHC1_DAT3 / GPIO1_DAT20 /SPI1_PCS0 / cfg_gpinput3	Data	C2	IO	EV_{DD}	5
SDHC1_DAT4/ SPI3_PCS0 / GPIO1_DAT15 /SPI1_PCS3 / SDHC1_VSEL	Data	A3	IO	OV_{DD}	---
SDHC1_DAT5/ SPI3_PCS1 / GPIO1_DAT14 / SDHC1_CMD_DIR	Data	A4	IO	OV_{DD}	---
SDHC1_DAT6/ SPI3_PCS2 / GPIO1_DAT13 / SDHC1_DAT0_DIR	Data	B3	IO	OV_{DD}	---
SDHC1_DAT7/ SPI3_PCS3 / GPIO1_DAT12 / SDHC1_DAT123_DIR	Data	C3	IO	OV_{DD}	---
SDHC1_DS/ SPI3_SCK / GPIO4_DAT29	Data Strobe (eMMC HS400 mode)	B2	I	OV_{DD}	1
SDHC1_VSEL/ SPI3_PCS0 / GPIO1_DAT15 /SPI1_PCS3 / SDHC1_DAT4	SDHC Voltage Select	A3	O	OV_{DD}	1
SDHC1_WP/ IIC2_SDA / GPIO1_DAT30/FTM2_CH0	Write Protect	E4	I	OV_{DD}	1
eSDHC 2					
SDHC2_CLK /GPIO2_DAT09 / SPI2_SCK /XSPI1_B_SCK	Host to Card Clock	A25	O	OV_{DD}	1
SDHC2_CLK_SYNC_IN/ IIC6_SDA /GPIO1_DAT22	Input Synchronous Clock	C27	I	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC2_CLK_SYNC_OUT/ IIC6_SCL /GPIO1_DAT23	Output Synchronuous Clock	D27	O	OV_{DD}	1
SDHC2_CMD / GPIO2_DAT19 /SPI2_SOUT / XSPI1_B_CS1_B	Command/Response	B25	IO	OV_{DD}	5
SDHC2_DAT0 / GPIO2_DAT11 /SPI2_SIN /	Data	A23	IO	OV_{DD}	5
XSPI1_B_DATA0/ cfg_gpinput4					
SDHC2_DAT1 / GPIO2_DAT12 /SPI2_PCS2 / XSPI1_B_DATA1/ cfg_gpinput5	Data	C24	IO	OV_{DD}	5
SDHC2_DAT2 / GPIO2_DAT13 /SPI2_PCS1 / XSPI1_B_DATA2/ cfg_gpinput6	Data	B23	IO	OV_{DD}	5
SDHC2_DAT3 / GPIO2_DAT14 /SPI2_PCS0 / XSPI1_B_DATA3/ cfg_gpinput7	Data	A24	IO	OV_{DD}	5
SDHC2_DAT4 / GPIO2_DAT15 /IIC7_SDA / XSPI1_B_DATA4	Data	C26	IO	OV_{DD}	5
SDHC2_DAT5 / GPIO2_DAT16 /IIC7_SCL / XSPI1_B_DATA5	Data	B27	IO	OV_{DD}	5
SDHC2_DAT6 / GPIO2_DAT17 /IIC8_SDA / XSPI1_B_DATA6	Data	A26	IO	OV_{DD}	5
SDHC2_DAT7 / GPIO2_DAT18 /IIC8_SCL / XSPI1_B_DATA7	Data	A27	IO	OV_{DD}	5
SDHC2_DS / GPIO2_DAT10 / SPI2_PCS3 / XSPI1_B_DQS	Data Strobe (eMMC HS400 mode)	C25	I	OV_{DD}	1, 11
UART					
UART1_CTS_B / GPIO1_DAT08 /UART3_SIN	Clear To Send	A6	I	OV_{DD}	1
UART1_RTS_B / GPIO1_DAT09 / UART3_SOUT	Ready to Send	A5	O	OV_{DD}	1
UART1_SIN/GPIO1_DAT10	Receive Data	B5	I	OV_{DD}	1
UART1_SOUT / GPIO1_DAT11 /cfg_rcw_src1	Transmit Data	B6	O	OV_{DD}	1
UART2_CTS_B / GPIO1_DAT04 /UART4_SIN	Clear To Send	C6	I	OV_{DD}	1
UART2_RTS_B / GPIO1_DAT05 / UART4_SOUT /cfg_eng_use2	Ready to Send	C5	O	OV_{DD}	1
UART2_SIN/GPIO1_DAT06	Receive Data	D5	I	OV_{DD}	1
UART2_SOUT / GPIO1_DAT07 /cfg_rcw_src0	Transmit Data	D6	O	OV_{DD}	1
UART3_SIN/ UART1_CTS_B / GPIO1_DAT08	Serial Input	A6	I	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
UART3_SOUT/ UART1_RTS_B / GPIO1_DAT09	Serial Output	A5	O	OV_{DD}	1
UART4_SIN/UART2_CTS_B/ GPIO1_DAT04	Serial Input	C6	I	OV_{DD}	1
UART4_SOUT/ UART2_RTS_B / GPIO1_DAT05 / cfg_eng_use2	Serial Output	C5	O	OV_{DD}	1
Interrupt Controller					
IRQ00 /GPIO3_DAT00 / FTM1_CH4	External Interrupt	H9	I	OV_{DD}	1
IRQ01 /GPIO3_DAT01 / FTM2_CH4	External Interrupt	H10	I	OV_{DD}	1
IRQ02 /GPIO3_DAT02 / FTM1_CH5	External Interrupt	H11	I	OV_{DD}	1
IRQ03 /GPIO3_DAT03 / FTM2_CH5	External Interrupt	J7	I	OV_{DD}	1
IRQ04 /GPIO3_DAT04 / FTM1_CH6	External Interrupt	J11	I	OV_{DD}	1
IRQ05 /GPIO3_DAT05 / FTM2_CH6	External Interrupt	J9	I	OV_{DD}	1
IRQ06 /GPIO3_DAT06 / FTM1_CH7	External Interrupt	H6	I	OV_{DD}	1
IRQ07 /GPIO3_DAT07 / FTM2_CH7	External Interrupt	K6	I	OV_{DD}	1
IRQ08 /GPIO3_DAT08	External Interrupt	H7	I	OV_{DD}	1
IRQ09 /GPIO3_DAT09	External Interrupt	K7	I	OV_{DD}	1
IRQ10 /GPIO3_DAT10	External Interrupt	H8	I	OV_{DD}	1
IRQ11 /GPIO3_DAT11	External Interrupt	K8	I	OV_{DD}	1
Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	J27	I	$TA\_BB\_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	N9	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	F6	IO	OV_{DD}	5, 6
PORESET_B	Power On Reset	E5	I	OV_{DD}	---
RESET_REQ_B / GPIO2_DAT08	Reset Request (POR or Hard)	M9	O	OV_{DD}	1, 17
Clocking					
DDRCLK	DDR Controller Clock	Y29	I	OV_{DD}	---
DIFF_SYSCLK_N	Differential System Clock (negative)	AT18	I	$SD3\_SV_{DD}$	---
DIFF_SYSCLK_P	Differential System Clock (positive)	AU18	I	$SD3\_SV_{DD}$	---
EC_GTX_CLK125 / GPIO4_DAT24	Reference Clock	P3	I	OV_{DD}	1
Debug					
ASLEEP /GPIO2_DAT06 / EVT9_B /cfg_rcw_src2	Asleep	M7	O	OV_{DD}	1, 4

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
CLK_OUT/GPIO2_DAT07/ FTM1_CH1 /cfg_rcw_src3	Clock Out	L6	O	OV_{DD}	2
CLK_OUT2/ EC1_TXD0 / GPIO4_DAT03	Clock Output	J3	O	OV_{DD}	1
EVT0_B /GPIO3_DAT12 / FTM2_CH1	Event 0	K9	IO	OV_{DD}	7
EVT1_B /GPIO3_DAT13 / FTM1_CH2	Event 1	L11	IO	OV_{DD}	7
EVT2_B /GPIO3_DAT14 / FTM2_CH2	Event 2	G6	IO	OV_{DD}	7
EVT3_B /GPIO3_DAT15 / FTM1_CH3	Event 3	L10	IO	OV_{DD}	7
EVT4_B /GPIO3_DAT16 / FTM2_CH3	Event 4	M10	IO	OV_{DD}	7
EVT5_B/ IIC3_SCL / GPIO1_DAT29 /CAN1_TX	Event 5	H5	IO	OV_{DD}	---
EVT6_B/ IIC3_SDA / GPIO1_DAT28 /CAN1_RX	Event 6	J5	IO	OV_{DD}	---
EVT7_B/ IIC4_SCL / GPIO1_DAT27 /CAN2_TX	Event 7	K5	IO	OV_{DD}	---
EVT8_B/ IIC4_SDA / GPIO1_DAT26 /CAN2_RX	Event 8	L5	IO	OV_{DD}	---
EVT9_B/ ASLEEP / GPIO2_DAT06 /cfg_rcw_src2	Event 9	M7	O	OV_{DD}	1, 4
DFT					
SCAN_MODE_B	Internal Use Only	K10	I	OV_{DD}	8
TEST_SEL_B	Internal Use Only	E6	I	OV_{DD}	5
JTAG					
TBSCAN_EN_B	Test Boundary Scan Enable	F23	I	OV_{DD}	5
TCK	Test Clock	G26	I	OV_{DD}	---
TDI	Test Data In	H27	I	OV_{DD}	7
TDO	Test Data Out	G27	O	OV_{DD}	2
TMS	Test Mode Select	G25	I	OV_{DD}	7
TRST_B	Test Reset	H26	I	OV_{DD}	7
Analog Signals					
D1_TPA	DDR Controller 1 Test Point Analog	U28	IO	-	10
D2_TPA	DDR Controller 2 Test Point Analog	AB28	IO	$G2V_{DD}$	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
FA1_CGV	Internal Use Only	AT28	IO	-	12
FA1_CPIN	Internal Use Only	AL28	IO	-	12
FA2_DGV	Internal Use Only	D28	IO	-	12
FA2_DPIN	Internal Use Only	J28	IO	-	12
TD1_ANODE	Thermal diode anode	K27	IO	-	14
TD1_CATHODE	Thermal diode cathode	L27	IO	-	14
TD2_ANODE	Thermal diode anode	J12	IO	-	14
TD2_CATHODE	Thermal diode cathode	K12	IO	-	14
TH_TPA	Thermal Test Point Analog	G24	-	-	10
Serdes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AJ20	I	SD_SV_{DD}	9
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AJ13	I	SD_OV_{DD}	13
SD1_PLLF_REF_CLK_N	SerDes PLL Fast Reference Clock Complement	AV13	I	SD_SV_{DD}	---
SD1_PLLF_REF_CLK_P	SerDes PLL Fast Reference Clock	AW13	I	SD_SV_{DD}	---
SD1_PLLF_TPA	SerDes PLL Fast Analog Test Point	AJ18	O	AVDD_SD1_PLLF	10
SD1_PLLF_TPD	SerDes PLL Fast Digital Test Point	AJ17	O	SD_SV_{DD}	10
SD1_PLLS_REF_CLK_N	SerDes PLL Slow Reference Clock Complement	AP13	I	SD_SV_{DD}	---
SD1_PLLS_REF_CLK_P	SerDes PLL Slow Reference Clock	AR13	I	SD_SV_{DD}	---
SD1_PLLS_TPA	SerDes PLL Slow Analog Test Point	AJ15	O	AVDD_SD1_PLLS	10
SD1_PLLS_TPD	SerDes PLL Slow Digital Test Point	AJ14	O	SD_SV_{DD}	10
SD1_RX0_N	SerDes Receive Data (negative)	AV9	I	SD_SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AW9	I	SD_SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	AT10	I	SD_SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AU10	I	SD_SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AV11	I	SD_SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AW11	I	SD_SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AT12	I	SD_SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AU12	I	SD_SV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD1_RX4_N	SerDes Receive Data (negative)	AT14	I	SD_SV_{DD}	---
SD1_RX4_P	SerDes Receive Data (positive)	AU14	I	SD_SV_{DD}	---
SD1_RX5_N	SerDes Receive Data (negative)	AV15	I	SD_SV_{DD}	---
SD1_RX5_P	SerDes Receive Data (positive)	AW15	I	SD_SV_{DD}	---
SD1_RX6_N	SerDes Receive Data (negative)	AT16	I	SD_SV_{DD}	---
SD1_RX6_P	SerDes Receive Data (positive)	AU16	I	SD_SV_{DD}	---
SD1_RX7_N	SerDes Receive Data (negative)	AV17	I	SD_SV_{DD}	---
SD1_RX7_P	SerDes Receive Data (positive)	AW17	I	SD_SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AN9	O	SD_OV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AP9	O	SD_OV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AL10	O	SD_OV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AM10	O	SD_OV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AN11	O	SD_OV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AP11	O	SD_OV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AL12	O	SD_OV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AM12	O	SD_OV_{DD}	---
SD1_TX4_N	SerDes Transmit Data (negative)	AL14	O	SD_OV_{DD}	---
SD1_TX4_P	SerDes Transmit Data (positive)	AM14	O	SD_OV_{DD}	---
SD1_TX5_N	SerDes Transmit Data (negative)	AN15	O	SD_OV_{DD}	---
SD1_TX5_P	SerDes Transmit Data (positive)	AP15	O	SD_OV_{DD}	---
SD1_TX6_N	SerDes Transmit Data (negative)	AL16	O	SD_OV_{DD}	---
SD1_TX6_P	SerDes Transmit Data (positive)	AM16	O	SD_OV_{DD}	---
SD1_TX7_N	SerDes Transmit Data (negative)	AN17	O	SD_OV_{DD}	---
SD1_TX7_P	SerDes Transmit Data (positive)	AP17	O	SD_OV_{DD}	---
Serdes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	AJ21	I	SD_SV_{DD}	9

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AJ27	I	SD_OV_{DD}	13
SD2_PLLF_REF_CLK_N	SerDes PLL Fast Reference Clock Complement	AR23	I	SD_SV_{DD}	---
SD2_PLLF_REF_CLK_P	SerDes PLL Fast Reference Clock	AP23	I	SD_SV_{DD}	---
SD2_PLLF_TPA	SerDes PLL Fast Analog Test Point	AJ23	O	AVDD_SD2_PLLF	10
SD2_PLLF_TPD	SerDes PLL Fast Digital Test Point	AJ24	O	SD_SV_{DD}	10
SD2_PLLS_REF_CLK_N	SerDes PLL Slow Reference Clock Complement	AW23	I	SD_SV_{DD}	---
SD2_PLLS_REF_CLK_P	SerDes PLL Slow Reference Clock	AV23	I	SD_SV_{DD}	---
SD2_PLLS_TPA	SerDes PLL Slow Analog Test Point	AJ26	O	AVDD_SD2_PLLS	10
SD2_PLLS_TPD	SerDes PLL Slow Digital Test Point	AH26	O	SD_SV_{DD}	10
SD2_RX0_N	SerDes Receive Data (negative)	AV19	I	SD_SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AW19	I	SD_SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AT20	I	SD_SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AU20	I	SD_SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AV21	I	SD_SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AW21	I	SD_SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AT22	I	SD_SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AU22	I	SD_SV_{DD}	---
SD2_RX4_N	SerDes Receive Data (negative)	AT24	I	SD_SV_{DD}	---
SD2_RX4_P	SerDes Receive Data (positive)	AU24	I	SD_SV_{DD}	---
SD2_RX5_N	SerDes Receive Data (negative)	AV25	I	SD_SV_{DD}	---
SD2_RX5_P	SerDes Receive Data (positive)	AW25	I	SD_SV_{DD}	---
SD2_RX6_N	SerDes Receive Data (negative)	AT26	I	SD_SV_{DD}	---
SD2_RX6_P	SerDes Receive Data (positive)	AU26	I	SD_SV_{DD}	---
SD2_RX7_N	SerDes Receive Data (negative)	AV27	I	SD_SV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD2_RX7_P	SerDes Receive Data (positive)	AW27	I	SD_SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AN19	O	SD_OV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AP19	O	SD_OV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AL20	O	SD_OV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AM20	O	SD_OV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AN21	O	SD_OV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AP21	O	SD_OV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AL22	O	SD_OV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AM22	O	SD_OV_{DD}	---
SD2_TX4_N	SerDes Transmit Data (negative)	AL24	O	SD_OV_{DD}	---
SD2_TX4_P	SerDes Transmit Data (positive)	AM24	O	SD_OV_{DD}	---
SD2_TX5_N	SerDes Transmit Data (negative)	AN25	O	SD_OV_{DD}	---
SD2_TX5_P	SerDes Transmit Data (positive)	AP25	O	SD_OV_{DD}	---
SD2_TX6_N	SerDes Transmit Data (negative)	AL26	O	SD_OV_{DD}	---
SD2_TX6_P	SerDes Transmit Data (positive)	AM26	O	SD_OV_{DD}	---
SD2_TX7_N	SerDes Transmit Data (negative)	AN27	O	SD_OV_{DD}	---
SD2_TX7_P	SerDes Transmit Data (positive)	AP27	O	SD_OV_{DD}	---
Serdes 3					
SD3_IMP_CAL_RX	SerDes Receive Impedence Calibration	L15	I	$SD3\_SV_{DD}$	9
SD3_IMP_CAL_TX	SerDes Transmit Impedance Calibration	L20	I	$SD3\_OV_{DD}$	13
SD3_PLLF_REF_CLK_N	SerDes PLL Fast Reference Clock Complement	E17	I	$SD3\_SV_{DD}$	---
SD3_PLLF_REF_CLK_P	SerDes PLL Fast Reference Clock	F17	I	$SD3\_SV_{DD}$	---
SD3_PLLF_TPA	SerDes PLL Fast Analog Test Point	L17	O	AVDD_SD3_PLLF	10
SD3_PLLF_TPD	SerDes PLL Fast Digital Test Point	L18	O	$SD3\_SV_{DD}$	10
SD3_PLLS_REF_CLK_N	SerDes PLL Slow Reference Clock Complement	A17	I	$SD3\_SV_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD3_PLLS_REF_CLK_P	SerDes PLL Slow Reference Clock	B17	I	$SD3\_SV_{DD}$	---
SD3_PLLS_TPA	SerDes PLL Slow Analog Test Point	J22	O	AVDD_SD3_PLLS	10
SD3_PLLS_TPD	SerDes PLL Slow Digital Test Point	L22	O	$SD3\_SV_{DD}$	10
SD3_RX0_N	SerDes Receive Data (negative)	B13	I	$SD3\_SV_{DD}$	---
SD3_RX0_P	SerDes Receive Data (positive)	A13	I	$SD3\_SV_{DD}$	---
SD3_RX1_N	SerDes Receive Data (negative)	D14	I	$SD3\_SV_{DD}$	---
SD3_RX1_P	SerDes Receive Data (positive)	C14	I	$SD3\_SV_{DD}$	---
SD3_RX2_N	SerDes Receive Data (negative)	B15	I	$SD3\_SV_{DD}$	---
SD3_RX2_P	SerDes Receive Data (positive)	A15	I	$SD3\_SV_{DD}$	---
SD3_RX3_N	SerDes Receive Data (negative)	D16	I	$SD3\_SV_{DD}$	---
SD3_RX3_P	SerDes Receive Data (positive)	C16	I	$SD3\_SV_{DD}$	---
SD3_RX4_N	SerDes Receive Data (negative)	D18	I	$SD3\_SV_{DD}$	---
SD3_RX4_P	SerDes Receive Data (positive)	C18	I	$SD3\_SV_{DD}$	---
SD3_RX5_N	SerDes Receive Data (negative)	B19	I	$SD3\_SV_{DD}$	---
SD3_RX5_P	SerDes Receive Data (positive)	A19	I	$SD3\_SV_{DD}$	---
SD3_RX6_N	SerDes Receive Data (negative)	D20	I	$SD3\_SV_{DD}$	---
SD3_RX6_P	SerDes Receive Data (positive)	C20	I	$SD3\_SV_{DD}$	---
SD3_RX7_N	SerDes Receive Data (negative)	B21	I	$SD3\_SV_{DD}$	---
SD3_RX7_P	SerDes Receive Data (positive)	A21	I	$SD3\_SV_{DD}$	---
SD3_TX0_N	SerDes Transmit Data (negative)	G13	O	$SD3\_OV_{DD}$	---
SD3_TX0_P	SerDes Transmit Data (positive)	F13	O	$SD3\_OV_{DD}$	---
SD3_TX1_N	SerDes Transmit Data (negative)	J14	O	$SD3\_OV_{DD}$	---
SD3_TX1_P	SerDes Transmit Data (positive)	H14	O	$SD3\_OV_{DD}$	---
SD3_TX2_N	SerDes Transmit Data (negative)	G15	O	$SD3\_OV_{DD}$	---
SD3_TX2_P	SerDes Transmit Data (positive)	F15	O	$SD3\_OV_{DD}$	---
SD3_TX3_N	SerDes Transmit Data (negative)	J16	O	$SD3\_OV_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD3_TX3_P	SerDes Transmit Data (positive)	H16	O	$SD3\_OV_{DD}$	---
SD3_TX4_N	SerDes Transmit Data (negative)	J18	O	$SD3\_OV_{DD}$	---
SD3_TX4_P	SerDes Transmit Data (positive)	H18	O	$SD3\_OV_{DD}$	---
SD3_TX5_N	SerDes Transmit Data (negative)	G19	O	$SD3\_OV_{DD}$	---
SD3_TX5_P	SerDes Transmit Data (positive)	F19	O	$SD3\_OV_{DD}$	---
SD3_TX6_N	SerDes Transmit Data (negative)	J20	O	$SD3\_OV_{DD}$	---
SD3_TX6_P	SerDes Transmit Data (positive)	H20	O	$SD3\_OV_{DD}$	---
SD3_TX7_N	SerDes Transmit Data (negative)	G21	O	$SD3\_OV_{DD}$	---
SD3_TX7_P	SerDes Transmit Data (positive)	F21	O	$SD3\_OV_{DD}$	---
USB PHY 1 and 2					
USB1_DRVVBUS / GPIO4_DAT25/cfg_soc_use	USB PHY Digital signal - Drive VBUS	A7	O	OV_{DD}	1
USB1_D_M	USB PHY Data Minus	F9	IO	USB_HV_{DD}	---
USB1_D_P	USB PHY Data Plus	F8	IO	USB_HV_{DD}	---
USB1_ID	USB PHY ID Detect	E9	I	-	---
USB1_PWRFAULT / GPIO4_DAT26	USB PHY Digital signal - Power Fault	B7	I	OV_{DD}	1
USB1_RESREF	USB PHY Impedance Calibration	C12	IO	-	15
USB1_RX_M	USB PHY 3.0 Receive Data (negative)	D8	I	USB_SV_{DD}	---
USB1_RX_P	USB PHY 3.0 Receive Data (positive)	C8	I	USB_SV_{DD}	---
USB1_TX_M	USB PHY 3.0 Transmit Data (negative)	B9	O	USB_SV_{DD}	---
USB1_TX_P	USB PHY 3.0 Transmit Data (positive)	A9	O	USB_SV_{DD}	---
USB1_VBUS	USB PHY VBUS	G8	I	-	18
USB2_DRVVBUS / GPIO4_DAT27	USB PHY Digital signal - Drive VBUS	E7	O	OV_{DD}	1
USB2_D_M	USB PHY Data Minus	F11	IO	USB_HV_{DD}	---
USB2_D_P	USB PHY Data Plus	F10	IO	USB_HV_{DD}	---
USB2_ID	USB PHY ID Detect	E11	I	-	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
USB2_PWRFAULT / GPIO4_DAT28	USB PHY Digital signal - Power Fault	G7	I	OV_{DD}	1
USB2_RESREF	USB PHY Impedance Calibration	D12	IO	-	15
USB2_RX_M	USB PHY 3.0 Receive Data (negative)	D10	I	USB_SV_{DD}	---
USB2_RX_P	USB PHY 3.0 Receive Data (positive)	C10	I	USB_SV_{DD}	---
USB2_TX_M	USB PHY 3.0 Transmit Data (negative)	B11	O	USB_SV_{DD}	---
USB2_TX_P	USB PHY 3.0 Transmit Data (positive)	A11	O	USB_SV_{DD}	---
USB2_VBUS	USB PHY VBUS	G10	I	-	18
Ethernet Controller 1					
EC1_GTX_CLK / GPIO4_DAT05	Transmit Clock Out	F3	O	OV_{DD}	1
EC1_RXD0/GPIO4_DAT09	Receive Data	J2	I	OV_{DD}	1
EC1_RXD1/GPIO4_DAT08	Receive Data	J1	I	OV_{DD}	1
EC1_RXD2/GPIO4_DAT07	Receive Data	H1	I	OV_{DD}	1
EC1_RXD3/GPIO4_DAT06	Receive Data	G2	I	OV_{DD}	1
EC1_RX_CLK /GPIO4_DAT10	Receive Clock	G1	I	OV_{DD}	1
EC1_RX_DV /GPIO4_DAT11	Receive Data Valid	K1	I	OV_{DD}	1
EC1_TXD0/GPIO4_DAT03/ CLK_OUT2	Transmit Data	J3	O	OV_{DD}	1
EC1_TXD1/GPIO4_DAT02	Transmit Data	H3	O	OV_{DD}	1
EC1_TXD2/GPIO4_DAT01	Transmit Data	G4	O	OV_{DD}	1
EC1_TXD3/GPIO4_DAT00	Transmit Data	G3	O	OV_{DD}	1
EC1_TX_EN/GPIO4_DAT04	Transmit Enable	J4	O	OV_{DD}	1, 11
Ethernet Controller 2					
EC2_GTX_CLK / GPIO4_DAT17	Transmit Clock Out	K3	O	OV_{DD}	1
EC2_RXD0/GPIO4_DAT21/ TSEC_1588_TRIG_IN2	Receive Data	N2	I	OV_{DD}	1
EC2_RXD1/GPIO4_DAT20/ TSEC_1588_PULSE_OUT1	Receive Data	N1	I	OV_{DD}	1
EC2_RXD2/GPIO4_DAT19	Receive Data	M1	I	OV_{DD}	1
EC2_RXD3/GPIO4_DAT18	Receive Data	L2	I	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EC2_RX_CLK / GPIO4_DAT22 / TSEC_1588_CLK_IN	Receive Clock	L1	I	OV_{DD}	1
EC2_RX_DV /GPIO4_DAT23 / TSEC_1588_TRIG_IN1	Receive Data Valid	P1	I	OV_{DD}	1
EC2_TXD0 /GPIO4_DAT15 / TSEC_1588_PULSE_OUT2	Transmit Data	N3	O	OV_{DD}	1
EC2_TXD1 /GPIO4_DAT14 / TSEC_1588_CLK_OUT	Transmit Data	M3	O	OV_{DD}	1
EC2_TXD2 /GPIO4_DAT13 / TSEC_1588_ALARM_OUT1	Transmit Data	L4	O	OV_{DD}	1
EC2_TXD3 /GPIO4_DAT12 / TSEC_1588_ALARM_OUT2	Transmit Data	L3	O	OV_{DD}	1
EC2_TX_EN/GPIO4_DAT16	Transmit Enable	N4	O	OV_{DD}	1, 11
Sync Ethernet ClockOut					
RCLK0	Reconstructed Clock	N6	O	OV_{DD}	---
RCLK1	Reconstructed Clock	N8	O	OV_{DD}	---
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	R2	O	OV_{DD}	---
EMI1_MDIO	Management Data In/Out	R1	IO	OV_{DD}	---
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock	P4	O	OV_{DD}	---
EMI2_MDIO	Management Data In/Out	R3	IO	OV_{DD}	5, 6
General Purpose Input/Output					
GPIO1_DAT02/ IIC1_SDA	General Purpose Input/Output	G5	IO	OV_{DD}	---
GPIO1_DAT03/ IIC1_SCL	General Purpose Input/Output	F5	IO	OV_{DD}	---
GPIO1_DAT04/ UART2_CTS_B /UART4_SIN	General Purpose Input/Output	C6	IO	OV_{DD}	---
GPIO1_DAT05/ UART2_RTS_B / UART4_SOUT /cfg_eng_use2	General Purpose Input/Output	C5	O	OV_{DD}	1
GPIO1_DAT06/UART2_SIN	General Purpose Input/Output	D5	IO	OV_{DD}	---
GPIO1_DAT07/ UART2_SOUT /cfg_rcw_src0	General Purpose Input/Output	D6	O	OV_{DD}	1
GPIO1_DAT08/ UART1_CTS_B /UART3_SIN	General Purpose Input/Output	A6	IO	OV_{DD}	---
GPIO1_DAT09/ UART1_RTS_B / UART3_SOUT	General Purpose Input/Output	A5	O	OV_{DD}	1
GPIO1_DAT10/UART1_SIN	General Purpose Input/Output	B5	IO	OV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT11/ UART1_SOUT /cfg_rcw_src1	General Purpose Input/Output	B6	O	OV_{DD}	1
GPIO1_DAT12/ SPI3_PCS3 / SDHC1_DAT123_DIR / SDHC1_DAT7	General Purpose Input/Output	C3	IO	OV_{DD}	---
GPIO1_DAT13/ SPI3_PCS2 / SDHC1_DAT0_DIR/ SDHC1_DAT6	General Purpose Input/Output	B3	IO	OV_{DD}	---
GPIO1_DAT14/ SPI3_PCS1 / SDHC1_CMD_DIR/ SDHC1_DAT5	General Purpose Input/Output	A4	IO	OV_{DD}	---
GPIO1_DAT15/ SPI3_PCS0 / SPI1_PCS3 /SDHC1_VSEL / SDHC1_DAT4	General Purpose Input/Output	A3	IO	OV_{DD}	---
GPIO1_DAT16/ SDHC1_CLK / SPI1_SCK	General Purpose Input/Output	D1	IO	EV_{DD}	---
GPIO1_DAT17/ SDHC1_DAT0 /SPI1_SIN / cfg_gpinput0	General Purpose Input/Output	F1	IO	EV_{DD}	
GPIO1_DAT18/ SDHC1_DAT1 /SPI1_PCS2 / cfg_gpinput1	General Purpose Input/Output	E2	IO	EV_{DD}	
GPIO1_DAT19/ SDHC1_DAT2 /SPI1_PCS1 / cfg_gpinput2	General Purpose Input/Output	C1	IO	EV_{DD}	
GPIO1_DAT20/ SDHC1_DAT3 /SPI1_PCS0 / cfg_gpinput3	General Purpose Input/Output	C2	IO	EV_{DD}	
GPIO1_DAT21/ SDHC1_CMD /SPI1_SOUT	General Purpose Input/Output	E1	IO	EV_{DD}	---
GPIO1_DAT22/ IIC6_SDA / SDHC2_CLK_SYNC_IN	General Purpose Input/Output	C27	IO	OV_{DD}	---
GPIO1_DAT23/ IIC6_SCL / SDHC2_CLK_SYNC_OUT	General Purpose Input/Output	D27	IO	OV_{DD}	---
GPIO1_DAT24/ SPI3_SIN / SDHC1_CLK_SYNC_IN / IIC5_SDA	General Purpose Input/Output	D3	IO	OV_{DD}	---
GPIO1_DAT25/ SPI3_SOUT / SDHC1_CLK_SYNC_OUT / IIC5_SCL	General Purpose Input/Output	C4	IO	OV_{DD}	---
GPIO1_DAT26/ IIC4_SDA / CAN2_RX/EVT8_B	General Purpose Input/Output	L5	IO	OV_{DD}	---
GPIO1_DAT27/ IIC4_SCL / CAN2_TX /EVT7_B	General Purpose Input/Output	K5	IO	OV_{DD}	---
GPIO1_DAT28/ IIC3_SDA / CAN1_RX/EVT6_B	General Purpose Input/Output	J5	IO	OV_{DD}	---
GPIO1_DAT29/ IIC3_SCL / CAN1_TX /EVT5_B	General Purpose Input/Output	H5	IO	OV_{DD}	---
GPIO1_DAT30/ IIC2_SDA / FTM2_CH0/SDHC1_WP	General Purpose Input/Output	E4	IO	OV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT31/ IIC2_SCL / FTM1_CH0 /SDHC1_CD_B	General Purpose Input/Output	E3	IO	OV_{DD}	---
GPIO2_DAT06/ ASLEEP / EVT9_B /cfg_rcw_src2	General Purpose Input/Output	M7	O	OV_{DD}	1
GPIO2_DAT07/ CLK_OUT / FTM1_CH1 /cfg_rcw_src3	General Purpose Input/Output	L6	O	OV_{DD}	1
GPIO2_DAT08/ RESET_REQ_B	General Purpose Input/Output	M9	O	OV_{DD}	1
GPIO2_DAT09/ SDHC2_CLK / SPI2_SCK /XSPI1_B_SCK	General Purpose Input/Output	A25	IO	OV_{DD}	---
GPIO2_DAT10/ SDHC2_DS / SPI2_PCS3 /XSPI1_B_DQS	General Purpose Input/Output	C25	IO	OV_{DD}	---
GPIO2_DAT11/ SDHC2_DAT0 /SPI2_SIN/ XSPI1_B_DATA0/ cfg_gpinput4	General Purpose Input/Output	A23	IO	OV_{DD}	
GPIO2_DAT12/ SDHC2_DAT1 /SPI2_PCS2/ XSPI1_B_DATA1/ cfg_gpinput5	General Purpose Input/Output	C24	IO	OV_{DD}	
GPIO2_DAT13/ SDHC2_DAT2 /SPI2_PCS1/ XSPI1_B_DATA2/ cfg_gpinput6	General Purpose Input/Output	B23	IO	OV_{DD}	
GPIO2_DAT14/ SDHC2_DAT3 /SPI2_PCS0/ XSPI1_B_DATA3/ cfg_gpinput7	General Purpose Input/Output	A24	IO	OV_{DD}	
GPIO2_DAT15/ SDHC2_DAT4 /IIC7_SDA/ XSPI1_B_DATA4	General Purpose Input/Output	C26	IO	OV_{DD}	---
GPIO2_DAT16/ SDHC2_DAT5 /IIC7_SCL/ XSPI1_B_DATA5	General Purpose Input/Output	B27	IO	OV_{DD}	---
GPIO2_DAT17/ SDHC2_DAT6 /IIC8_SDA/ XSPI1_B_DATA6	General Purpose Input/Output	A26	IO	OV_{DD}	---
GPIO2_DAT18/ SDHC2_DAT7 /IIC8_SCL/ XSPI1_B_DATA7	General Purpose Input/Output	A27	IO	OV_{DD}	---
GPIO2_DAT19/ SDHC2_CMD /SPI2_SOUT / XSPI1_B_CS1_B	General Purpose Input/Output	B25	IO	OV_{DD}	---
GPIO2_DAT20/ XSPI1_A_CS1_B	General Purpose Input/Output	D23	O	OV_{DD}	1
GPIO2_DAT21/ XSPI1_A_CS0_B	General Purpose Input/Output	C23	O	OV_{DD}	1
GPIO2_DAT22/ XSPI1_A_SCK /cfg_eng_use0	General Purpose Input/Output	D22	O	OV_{DD}	1
GPIO2_DAT23/ XSPI1_A_DQS	General Purpose Input/Output	E23	IO	OV_{DD}	---
GPIO2_DAT24/ XSPI1_A_DATA0	General Purpose Input/Output	F25	IO	OV_{DD}	---
GPIO2_DAT25/ XSPI1_A_DATA1	General Purpose Input/Output	E24	IO	OV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO2_DAT26/ XSPI1_A_DATA2	General Purpose Input/Output	E26	IO	OV_{DD}	---
GPIO2_DAT27/ XSPI1_A_DATA3	General Purpose Input/Output	E27	IO	OV_{DD}	---
GPIO2_DAT28/ XSPI1_A_DATA4	General Purpose Input/Output	F27	IO	OV_{DD}	---
GPIO2_DAT29/ XSPI1_A_DATA5	General Purpose Input/Output	D26	IO	OV_{DD}	---
GPIO2_DAT30/ XSPI1_A_DATA6	General Purpose Input/Output	E25	IO	OV_{DD}	---
GPIO2_DAT31/ XSPI1_A_DATA7	General Purpose Input/Output	D24	IO	OV_{DD}	---
GPIO3_DAT00/ IRQ00 / FTM1_CH4	General Purpose Input/Output	H9	IO	OV_{DD}	---
GPIO3_DAT01/ IRQ01 / FTM2_CH4	General Purpose Input/Output	H10	IO	OV_{DD}	---
GPIO3_DAT02/ IRQ02 / FTM1_CH5	General Purpose Input/Output	H11	IO	OV_{DD}	---
GPIO3_DAT03/ IRQ03 / FTM2_CH5	General Purpose Input/Output	J7	IO	OV_{DD}	---
GPIO3_DAT04/ IRQ04 / FTM1_CH6	General Purpose Input/Output	J11	IO	OV_{DD}	---
GPIO3_DAT05/ IRQ05 / FTM2_CH6	General Purpose Input/Output	J9	IO	OV_{DD}	---
GPIO3_DAT06/ IRQ06 / FTM1_CH7	General Purpose Input/Output	H6	IO	OV_{DD}	---
GPIO3_DAT07/ IRQ07 / FTM2_CH7	General Purpose Input/Output	K6	IO	OV_{DD}	---
GPIO3_DAT08/ IRQ08	General Purpose Input/Output	H7	IO	OV_{DD}	---
GPIO3_DAT09/ IRQ09	General Purpose Input/Output	K7	IO	OV_{DD}	---
GPIO3_DAT10/ IRQ10	General Purpose Input/Output	H8	IO	OV_{DD}	---
GPIO3_DAT11/ IRQ11	General Purpose Input/Output	K8	IO	OV_{DD}	---
GPIO3_DAT12/ EVT0_B / FTM2_CH1	General Purpose Input/Output	K9	IO	OV_{DD}	---
GPIO3_DAT13/ EVT1_B / FTM1_CH2	General Purpose Input/Output	L11	IO	OV_{DD}	---
GPIO3_DAT14/ EVT2_B / FTM2_CH2	General Purpose Input/Output	G6	IO	OV_{DD}	---
GPIO3_DAT15/ EVT3_B / FTM1_CH3	General Purpose Input/Output	L10	IO	OV_{DD}	---
GPIO3_DAT16/ EVT4_B / FTM2_CH3	General Purpose Input/Output	M10	IO	OV_{DD}	---
GPIO4_DAT00/EC1_TXD3	General Purpose Input/Output	G3	IO	OV_{DD}	---
GPIO4_DAT01/EC1_TXD2	General Purpose Input/Output	G4	IO	OV_{DD}	---
GPIO4_DAT02/EC1_TXD1	General Purpose Input/Output	H3	IO	OV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO4_DAT03/ EC1_TXD0 / CLK_OUT2	General Purpose Input/Output	J3	IO	OV_{DD}	---
GPIO4_DAT04/EC1_TX_EN	General Purpose Input/Output	J4	IO	OV_{DD}	---
GPIO4_DAT05/ EC1_GTX_CLK	General Purpose Input/Output	F3	IO	OV_{DD}	---
GPIO4_DAT06/EC1_RXD3	General Purpose Input/Output	G2	IO	OV_{DD}	---
GPIO4_DAT07/EC1_RXD2	General Purpose Input/Output	H1	IO	OV_{DD}	---
GPIO4_DAT08/EC1_RXD1	General Purpose Input/Output	J1	IO	OV_{DD}	---
GPIO4_DAT09/EC1_RXD0	General Purpose Input/Output	J2	IO	OV_{DD}	---
GPIO4_DAT10/ EC1_RX_CLK	General Purpose Input/Output	G1	IO	OV_{DD}	---
GPIO4_DAT11/ EC1_RX_DV	General Purpose Input/Output	K1	IO	OV_{DD}	---
GPIO4_DAT12/ EC2_TXD3 / TSEC_1588_ALARM_OUT2	General Purpose Input/Output	L3	IO	OV_{DD}	---
GPIO4_DAT13/ EC2_TXD2 / TSEC_1588_ALARM_OUT1	General Purpose Input/Output	L4	IO	OV_{DD}	---
GPIO4_DAT14/ EC2_TXD1 / TSEC_1588_CLK_OUT	General Purpose Input/Output	M3	IO	OV_{DD}	---
GPIO4_DAT15/ EC2_TXD0 / TSEC_1588_PULSE_OUT2	General Purpose Input/Output	N3	IO	OV_{DD}	---
GPIO4_DAT16/EC2_TX_EN	General Purpose Input/Output	N4	IO	OV_{DD}	---
GPIO4_DAT17/ EC2_GTX_CLK	General Purpose Input/Output	K3	IO	OV_{DD}	---
GPIO4_DAT18/EC2_RXD3	General Purpose Input/Output	L2	IO	OV_{DD}	---
GPIO4_DAT19/EC2_RXD2	General Purpose Input/Output	M1	IO	OV_{DD}	---
GPIO4_DAT20/ EC2_RXD1 / TSEC_1588_PULSE_OUT1	General Purpose Input/Output	N1	IO	OV_{DD}	---
GPIO4_DAT21/ EC2_RXD0 / TSEC_1588_TRIG_IN2	General Purpose Input/Output	N2	IO	OV_{DD}	---
GPIO4_DAT22/ EC2_RX_CLK / TSEC_1588_CLK_IN	General Purpose Input/Output	L1	IO	OV_{DD}	---
GPIO4_DAT23/ EC2_RX_DV/ TSEC_1588_TRIG_IN1	General Purpose Input/Output	P1	IO	OV_{DD}	---
GPIO4_DAT24/ EC_GTX_CLK125	General Purpose Input/Output	P3	IO	OV_{DD}	---
GPIO4_DAT25/ USB1_DRVVBUS / cfg_soc_use	General Purpose Input/Output	A7	IO	OV_{DD}	1
GPIO4_DAT26/ USB1_PWRFAULT	General Purpose Input/Output	B7	IO	OV_{DD}	---
GPIO4_DAT27/ USB2_DRVVBUS	General Purpose Input/Output	E7	IO	OV_{DD}	---
GPIO4_DAT28/ USB2_PWRFAULT	General Purpose Input/Output	G7	IO	OV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO4_DAT29/ SPI3_SCK / SDHC1_DS	General Purpose Input/Output	B2	IO	OV_{DD}	---
FlexTimer Module					
FTM1_CH0/ IIC2_SCL / GPIO1_DAT31 / SDHC1_CD_B	Channel 0	E3	IO	OV_{DD}	---
FTM1_CH1/ CLK_OUT / GPIO2_DAT07 /cfg_rcw_src3	Channel 1	L6	O	OV_{DD}	1
FTM1_CH2/ EVT1_B / GPIO3_DAT13	Channel 2	L11	IO	OV_{DD}	---
FTM1_CH3/ EVT3_B / GPIO3_DAT15	Channel 3	L10	IO	OV_{DD}	---
FTM1_CH4/ IRQ00 / GPIO3_DAT00	Channel 4	H9	IO	OV_{DD}	---
FTM1_CH5/ IRQ02 / GPIO3_DAT02	Channel 5	H11	IO	OV_{DD}	---
FTM1_CH6/ IRQ04 / GPIO3_DAT04	Channel 6	J11	IO	OV_{DD}	---
FTM1_CH7/ IRQ06 / GPIO3_DAT06	Channel 7	H6	IO	OV_{DD}	---
FTM2_CH0/ IIC2_SDA / GPIO1_DAT30/SDHC1_WP	Channel 0	E4	IO	OV_{DD}	---
FTM2_CH1/ EVT0_B / GPIO3_DAT12	Channel 1	K9	IO	OV_{DD}	---
FTM2_CH2/ EVT2_B / GPIO3_DAT14	Channel 2	G6	IO	OV_{DD}	---
FTM2_CH3/ EVT4_B / GPIO3_DAT16	Channel 3	M10	IO	OV_{DD}	---
FTM2_CH4/ IRQ01 / GPIO3_DAT01	Channel 4	H10	IO	OV_{DD}	---
FTM2_CH5/ IRQ03 / GPIO3_DAT03	Channel 5	J7	IO	OV_{DD}	---
FTM2_CH6/ IRQ05 / GPIO3_DAT05	Channel 6	J9	IO	OV_{DD}	---
FTM2_CH7/ IRQ07 / GPIO3_DAT07	Channel 7	K6	IO	OV_{DD}	---
Controller Area Network					
CAN1_RX/ IIC3_SDA / GPIO1_DAT28/EVT6_B	Receive Data	J5	I	OV_{DD}	1
CAN1_TX/ IIC3_SCL / GPIO1_DAT29 /EVT5_B	Transmit Data	H5	O	OV_{DD}	1
CAN2_RX/ IIC4_SDA / GPIO1_DAT26/EVT8_B	Receive Data	L5	I	OV_{DD}	1
CAN2_TX/ IIC4_SCL / GPIO1_DAT27 /EVT7_B	Transmit Data	K5	O	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
Power-On-Reset Configuration					
cfg_eng_use0/ XSPI1_A_SCK / GPIO2_DAT22	Power-on-Reset Configuration	D22	I	OV_{DD}	1, 4
cfg_eng_use2/ UART2_RTS_B / GPIO1_DAT05 / UART4_SOUT	Power-on-Reset Configuration	C5	I	OV_{DD}	1, 4
cfg_gpinput0/ SDHC1_DAT0 / GPIO1_DAT17/SPI1_SIN	General Input	F1	I	EV_{DD}	1, 4
cfg_gpinput1/ SDHC1_DAT1 / GPIO1_DAT18/SPI1_PCS2	General Input	E2	I	EV_{DD}	1, 4
cfg_gpinput2/ SDHC1_DAT2 / GPIO1_DAT19/SPI1_PCS1	General Input	C1	I	EV_{DD}	1, 4
cfg_gpinput3/ SDHC1_DAT3 / GPIO1_DAT20/SPI1_PCS0	General Input	C2	I	EV_{DD}	1, 4
cfg_gpinput4/ SDHC2_DAT0 / GPIO2_DAT11/SPI2_SIN / XSPI1_B_DATA0	General Input	A23	I	OV_{DD}	1, 4
cfg_gpinput5/ SDHC2_DAT1 / GPIO2_DAT12/SPI2_PCS2 / XSPI1_B_DATA1	General Input	C24	I	OV_{DD}	1, 4
cfg_gpinput6/ SDHC2_DAT2 / GPIO2_DAT13/SPI2_PCS1 / XSPI1_B_DATA2	General Input	B23	I	OV_{DD}	1, 4
cfg_gpinput7/ SDHC2_DAT3 / GPIO2_DAT14/SPI2_PCS0 / XSPI1_B_DATA3	General Input	A24	I	OV_{DD}	1, 4
cfg_rcw_src0/ UART2_SOUT / GPIO1_DAT07	Reset Configuration Word	D6	I	OV_{DD}	1, 4
cfg_rcw_src1/ UART1_SOUT / GPIO1_DAT11	Reset Configuration Word	B6	I	OV_{DD}	1, 4
cfg_rcw_src2/ ASLEEP / GPIO2_DAT06/EVT9_B	Reset Configuration Word	M7	I	OV_{DD}	1, 4
cfg_rcw_src3/ CLK_OUT / GPIO2_DAT07/FTM1_CH1	Reset Configuration Word	L6	I	OV_{DD}	1, 4
cfg_soc_use/ USB1_DRVVBUS / GPIO4_DAT25	Power-on-Reset Configuration	A7	I	OV_{DD}	1, 4
cfg_svr0/ XSPI1_A_CS0_B / GPIO2_DAT21	Power-on-Reset Configuration	C23	I	OV_{DD}	1, 4
cfg_svr1/ XSPI1_A_CS1_B / GPIO2_DAT20	Power-on-Reset Configuration	D23	I	OV_{DD}	1, 4
SPI1					
SPI1_PCS0/ SDHC1_DAT3 / GPIO1_DAT20/cfg_gpinput3	SPI Chip Select	C2	O	EV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI1_PCS1/ SDHC1_DAT2 / GPIO1_DAT19 /cfg_gpinput2	SPI Chip Select	C1	O	EV_{DD}	1
SPI1_PCS2/ SDHC1_DAT1 / GPIO1_DAT18 /cfg_gpinput1	SPI Chip Select	E2	O	EV_{DD}	1
SPI1_PCS3/ SPI3_PCS0 / GPIO1_DAT15 / SDHC1_VSEL /SDHC1_DAT4	SPI Chip Select	A3	O	OV_{DD}	1
SPI1_SCK/ SDHC1_CLK / GPIO1_DAT16	Serial Clock	D1	O	EV_{DD}	1
SPI1_SIN/ SDHC1_DAT0 / GPIO1_DAT17 /cfg_gpinput0	Serial Data Input	F1	I	EV_{DD}	1
SPI1_SOUT/ SDHC1_CMD / GPIO1_DAT21	Serial Data Output	E1	O	EV_{DD}	1
SPI2					
SPI2_PCS0/ SDHC2_DAT3 / GPIO2_DAT14 / XSPI1_B_DATA3/ cfg_gpinput7	SPI Chip Select	A24	O	OV_{DD}	1
SPI2_PCS1/ SDHC2_DAT2 / GPIO2_DAT13 / XSPI1_B_DATA2/ cfg_gpinput6	SPI Chip Select	B23	O	OV_{DD}	1
SPI2_PCS2/ SDHC2_DAT1 / GPIO2_DAT12 / XSPI1_B_DATA1/ cfg_gpinput5	SPI Chip Select	C24	O	OV_{DD}	1
SPI2_PCS3/ SDHC2_DS / GPIO2_DAT10 / XSPI1_B_DQS	SPI Chip Select	C25	O	OV_{DD}	1
SPI2_SCK/ SDHC2_CLK / GPIO2_DAT09 / XSPI1_B_SCK	Serial Clock	A25	O	OV_{DD}	1
SPI2_SIN/ SDHC2_DAT0 / GPIO2_DAT11 / XSPI1_B_DATA0/ cfg_gpinput4	Serial Data Input	A23	I	OV_{DD}	1
SPI2_SOUT/ SDHC2_CMD / GPIO2_DAT19 / XSPI1_B_CS1_B	Serial Data Output	B25	O	OV_{DD}	1
SPI3					
SPI3_PCS0 /GPIO1_DAT15 / SPI1_PCS3 /SDHC1_VSEL / SDHC1_DAT4	SPI Chip Select	A3	O	OV_{DD}	1
SPI3_PCS1 /GPIO1_DAT14 / SDHC1_CMD_DIR/ SDHC1_DAT5	SPI Chip Select	A4	O	OV_{DD}	1
SPI3_PCS2 /GPIO1_DAT13 / SDHC1_DAT0_DIR/ SDHC1_DAT6	SPI Chip Select	B3	O	OV_{DD}	1
SPI3_PCS3 /GPIO1_DAT12 / SDHC1_DAT123_DIR / SDHC1_DAT7	SPI Chip Select	C3	O	OV_{DD}	1
SPI3_SCK /GPIO4_DAT29 / SDHC1_DS	Serial Clock	B2	O	OV_{DD}	1

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI3_SIN /GPIO1_DAT24 / SDHC1_CLK_SYNC_IN / IIC5_SDA	Serial Data Input	D3	I	OV_{DD}	1
SPI3_SOUT /GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT / IIC5_SCL	Serial Data Output	C4	O	OV_{DD}	1
IEEE 1588					
TSEC_1588_ALARM_OUT1/ EC2_TXD2/GPIO4_DAT13	Alarm Out	L4	O	OV_{DD}	1
TSEC_1588_ALARM_OUT2/ EC2_TXD3/GPIO4_DAT12	Alarm Out	L3	O	OV_{DD}	1
TSEC_1588_CLK_IN/ EC2_RX_CLK /GPIO4_DAT22	Clock Input	L1	I	OV_{DD}	1
TSEC_1588_CLK_OUT/ EC2_TXD1 /GPIO4_DAT14	Clock Out	M3	O	OV_{DD}	1
TSEC_1588_PULSE_OUT1/ EC2_RXD1/GPIO4_DAT20	Pulse Out	N1	O	OV_{DD}	1
TSEC_1588_PULSE_OUT2/ EC2_TXD0/GPIO4_DAT15	Pulse Out	N3	O	OV_{DD}	1
TSEC_1588_TRIG_IN1/ EC2_RX_DV /GPIO4_DAT23	Trigger In	P1	I	OV_{DD}	1
TSEC_1588_TRIG_IN2/ EC2_RXD0 /GPIO4_DAT21	Trigger In	N2	I	OV_{DD}	1
Power and Ground Signals					
GND001	GND	A2	---	---	---
GND002	GND	A8	---	---	---
GND003	GND	A10	---	---	---
GND004	GND	A28	---	---	---
GND005	GND	A35	---	---	---
GND006	GND	B1	---	---	---
GND007	GND	B4	---	---	---
GND008	GND	B8	---	---	---
GND009	GND	B10	---	---	---
GND010	GND	B12	---	---	---
GND011	GND	B24	---	---	---
GND012	GND	B26	---	---	---
GND013	GND	B28	---	---	---
GND014	GND	B30	---	---	---
GND015	GND	B32	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND016	GND	C7	---	---	---
GND017	GND	C9	---	---	---
GND018	GND	C11	---	---	---
GND019	GND	C22	---	---	---
GND020	GND	C28	---	---	---
GND021	GND	C35	---	---	---
GND022	GND	D2	---	---	---
GND023	GND	D4	---	---	---
GND024	GND	D7	---	---	---
GND025	GND	D9	---	---	---
GND026	GND	D11	---	---	---
GND027	GND	D25	---	---	---
GND028	GND	D30	---	---	---
GND029	GND	D33	---	---	---
GND030	GND	E8	---	---	---
GND031	GND	E10	---	---	---
GND032	GND	E12	---	---	---
GND033	GND	E22	---	---	---
GND034	GND	E28	---	---	---
GND035	GND	E36	---	---	---
GND036	GND	F2	---	---	---
GND037	GND	F4	---	---	---
GND038	GND	F7	---	---	---
GND039	GND	F24	---	---	---
GND040	GND	F26	---	---	---
GND041	GND	F28	---	---	---
GND042	GND	F30	---	---	---
GND043	GND	F34	---	---	---
GND044	GND	G9	---	---	---
GND045	GND	G11	---	---	---
GND046	GND	G28	---	---	---
GND047	GND	G32	---	---	---
GND048	GND	G36	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND049	GND	H2	---	---	---
GND050	GND	H4	---	---	---
GND051	GND	H12	---	---	---
GND052	GND	H23	---	---	---
GND053	GND	H24	---	---	---
GND054	GND	H25	---	---	---
GND055	GND	H28	---	---	---
GND056	GND	H30	---	---	---
GND057	GND	H34	---	---	---
GND058	GND	J6	---	---	---
GND059	GND	J8	---	---	---
GND060	GND	J10	---	---	---
GND061	GND	J32	---	---	---
GND062	GND	J36	---	---	---
GND063	GND	K2	---	---	---
GND064	GND	K4	---	---	---
GND065	GND	K23	---	---	---
GND066	GND	K24	---	---	---
GND067	GND	K25	---	---	---
GND068	GND	K26	---	---	---
GND069	GND	K28	---	---	---
GND070	GND	K30	---	---	---
GND071	GND	K34	---	---	---
GND072	GND	L7	---	---	---
GND073	GND	L12	---	---	---
GND074	GND	L13	---	---	---
GND075	GND	L32	---	---	---
GND076	GND	L36	---	---	---
GND077	GND	M2	---	---	---
GND078	GND	M4	---	---	---
GND079	GND	M6	---	---	---
GND080	GND	M8	---	---	---
GND081	GND	M11	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND082	GND	M21	---	---	---
GND083	GND	M22	---	---	---
GND084	GND	M23	---	---	---
GND085	GND	M24	---	---	---
GND086	GND	M25	---	---	---
GND087	GND	M28	---	---	---
GND088	GND	M34	---	---	---
GND089	GND	N5	---	---	---
GND090	GND	N7	---	---	---
GND091	GND	N10	---	---	---
GND092	GND	N12	---	---	---
GND093	GND	N26	---	---	---
GND094	GND	N28	---	---	---
GND095	GND	N30	---	---	---
GND096	GND	N32	---	---	---
GND097	GND	N36	---	---	---
GND098	GND	P2	---	---	---
GND099	GND	P5	---	---	---
GND100	GND	P6	---	---	---
GND101	GND	P7	---	---	---
GND102	GND	P8	---	---	---
GND103	GND	P9	---	---	---
GND104	GND	P10	---	---	---
GND105	GND	P13	---	---	---
GND106	GND	P21	---	---	---
GND107	GND	P23	---	---	---
GND108	GND	P25	---	---	---
GND109	GND	P27	---	---	---
GND110	GND	P30	---	---	---
GND111	GND	P34	---	---	---
GND112	GND	R4	---	---	---
GND113	GND	R10	---	---	---
GND114	GND	R12	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND115	GND	R14	---	---	---
GND116	GND	R16	---	---	---
GND117	GND	R18	---	---	---
GND118	GND	R20	---	---	---
GND119	GND	R22	---	---	---
GND120	GND	R24	---	---	---
GND121	GND	R26	---	---	---
GND122	GND	R28	---	---	---
GND123	GND	R30	---	---	---
GND124	GND	R32	---	---	---
GND125	GND	R36	---	---	---
GND126	GND	T1	---	---	---
GND127	GND	T3	---	---	---
GND128	GND	T6	---	---	---
GND129	GND	T10	---	---	---
GND130	GND	T13	---	---	---
GND131	GND	T15	---	---	---
GND132	GND	T17	---	---	---
GND133	GND	T19	---	---	---
GND134	GND	T21	---	---	---
GND135	GND	T23	---	---	---
GND136	GND	T25	---	---	---
GND137	GND	T27	---	---	---
GND138	GND	T30	---	---	---
GND139	GND	T34	---	---	---
GND140	GND	U4	---	---	---
GND141	GND	U8	---	---	---
GND142	GND	U10	---	---	---
GND143	GND	U12	---	---	---
GND144	GND	U14	---	---	---
GND145	GND	U16	---	---	---
GND146	GND	U18	---	---	---
GND147	GND	U20	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND148	GND	U22	---	---	---
GND149	GND	U24	---	---	---
GND150	GND	U26	---	---	---
GND151	GND	U30	---	---	---
GND152	GND	U32	---	---	---
GND153	GND	U36	---	---	---
GND154	GND	V6	---	---	---
GND155	GND	V10	---	---	---
GND156	GND	V13	---	---	---
GND157	GND	V15	---	---	---
GND158	GND	V17	---	---	---
GND159	GND	V19	---	---	---
GND160	GND	V21	---	---	---
GND161	GND	V23	---	---	---
GND162	GND	V25	---	---	---
GND163	GND	V27	---	---	---
GND164	GND	V30	---	---	---
GND165	GND	V34	---	---	---
GND166	GND	W4	---	---	---
GND167	GND	W8	---	---	---
GND168	GND	W10	---	---	---
GND169	GND	W12	---	---	---
GND170	GND	W14	---	---	---
GND171	GND	W16	---	---	---
GND172	GND	W18	---	---	---
GND173	GND	W20	---	---	---
GND174	GND	W22	---	---	---
GND175	GND	W24	---	---	---
GND176	GND	W26	---	---	---
GND177	GND	W28	---	---	---
GND178	GND	W30	---	---	---
GND179	GND	Y6	---	---	---
GND180	GND	Y10	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND181	GND	Y13	---	---	---
GND182	GND	Y15	---	---	---
GND183	GND	Y17	---	---	---
GND184	GND	Y19	---	---	---
GND185	GND	Y21	---	---	---
GND186	GND	Y23	---	---	---
GND187	GND	Y25	---	---	---
GND188	GND	Y27	---	---	---
GND189	GND	Y30	---	---	---
GND190	GND	Y32	---	---	---
GND191	GND	Y35	---	---	---
GND192	GND	Y37	---	---	---
GND193	GND	AA4	---	---	---
GND194	GND	AA8	---	---	---
GND195	GND	AA10	---	---	---
GND196	GND	AA12	---	---	---
GND197	GND	AA14	---	---	---
GND198	GND	AA16	---	---	---
GND199	GND	AA18	---	---	---
GND200	GND	AA20	---	---	---
GND201	GND	AA22	---	---	---
GND202	GND	AA24	---	---	---
GND203	GND	AA26	---	---	---
GND204	GND	AA28	---	---	---
GND205	GND	AA30	---	---	---
GND206	GND	AB6	---	---	---
GND207	GND	AB10	---	---	---
GND208	GND	AB13	---	---	---
GND209	GND	AB15	---	---	---
GND210	GND	AB17	---	---	---
GND211	GND	AB19	---	---	---
GND212	GND	AB21	---	---	---
GND213	GND	AB23	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND214	GND	AB25	---	---	---
GND215	GND	AB27	---	---	---
GND216	GND	AB30	---	---	---
GND217	GND	AB34	---	---	---
GND218	GND	AC4	---	---	---
GND219	GND	AC8	---	---	---
GND220	GND	AC10	---	---	---
GND221	GND	AC14	---	---	---
GND222	GND	AC16	---	---	---
GND223	GND	AC18	---	---	---
GND224	GND	AC20	---	---	---
GND225	GND	AC22	---	---	---
GND226	GND	AC24	---	---	---
GND227	GND	AC26	---	---	---
GND228	GND	AC30	---	---	---
GND229	GND	AC32	---	---	---
GND230	GND	AC36	---	---	---
GND231	GND	AD6	---	---	---
GND232	GND	AD10	---	---	---
GND233	GND	AD13	---	---	---
GND234	GND	AD15	---	---	---
GND235	GND	AD17	---	---	---
GND236	GND	AD19	---	---	---
GND237	GND	AD21	---	---	---
GND238	GND	AD23	---	---	---
GND239	GND	AD25	---	---	---
GND240	GND	AD27	---	---	---
GND241	GND	AD30	---	---	---
GND242	GND	AD34	---	---	---
GND243	GND	AE4	---	---	---
GND244	GND	AE8	---	---	---
GND245	GND	AE10	---	---	---
GND246	GND	AE12	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND247	GND	AE14	---	---	---
GND248	GND	AE16	---	---	---
GND249	GND	AE18	---	---	---
GND250	GND	AE20	---	---	---
GND251	GND	AE22	---	---	---
GND252	GND	AE24	---	---	---
GND253	GND	AE26	---	---	---
GND254	GND	AE28	---	---	---
GND255	GND	AE30	---	---	---
GND256	GND	AE32	---	---	---
GND257	GND	AE36	---	---	---
GND258	GND	AF6	---	---	---
GND259	GND	AF10	---	---	---
GND260	GND	AF27	---	---	---
GND261	GND	AF30	---	---	---
GND262	GND	AF34	---	---	---
GND263	GND	AG4	---	---	---
GND264	GND	AG9	---	---	---
GND265	GND	AG11	---	---	---
GND266	GND	AG30	---	---	---
GND267	GND	AG32	---	---	---
GND268	GND	AG36	---	---	---
GND269	GND	AH7	---	---	---
GND270	GND	AH11	---	---	---
GND271	GND	AH28	---	---	---
GND272	GND	AH34	---	---	---
GND273	GND	AJ5	---	---	---
GND274	GND	AJ10	---	---	---
GND275	GND	AJ32	---	---	---
GND276	GND	AJ36	---	---	---
GND277	GND	AK4	---	---	---
GND278	GND	AK7	---	---	---
GND279	GND	AK9	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND280	GND	AK28	---	---	---
GND281	GND	AK30	---	---	---
GND282	GND	AK34	---	---	---
GND283	GND	AL5	---	---	---
GND284	GND	AL32	---	---	---
GND285	GND	AL36	---	---	---
GND286	GND	AM3	---	---	---
GND287	GND	AM8	---	---	---
GND288	GND	AM28	---	---	---
GND289	GND	AM30	---	---	---
GND290	GND	AM34	---	---	---
GND291	GND	AN6	---	---	---
GND292	GND	AN32	---	---	---
GND293	GND	AN36	---	---	---
GND294	GND	AP3	---	---	---
GND295	GND	AP5	---	---	---
GND296	GND	AP30	---	---	---
GND297	GND	AP34	---	---	---
GND298	GND	AR8	---	---	---
GND299	GND	AR28	---	---	---
GND300	GND	AR36	---	---	---
GND301	GND	AT4	---	---	---
GND302	GND	AT6	---	---	---
GND303	GND	AT30	---	---	---
GND304	GND	AT33	---	---	---
GND305	GND	AU3	---	---	---
GND306	GND	AU8	---	---	---
GND307	GND	AU28	---	---	---
GND308	GND	AU35	---	---	---
GND309	GND	AV4	---	---	---
GND310	GND	AV6	---	---	---
GND311	GND	AV30	---	---	---
GND312	GND	AV32	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND313	GND	AW2	---	---	---
GND314	GND	AW35	---	---	---
SENSEGND_CA	GND Sense pin	J24	---	---	---
SENSEGND_CB	GND Sense pin	AG26	---	---	---
SENSEGND_PL	GND Sense pin	AJ11	---	---	---
SD_GND01	SerDes 1 and SerDes 2 Ground	AG12	---	---	---
SD_GND02	SerDes 1 and SerDes 2 Ground	AG13	---	---	---
SD_GND03	SerDes 1 and SerDes 2 Ground	AG14	---	---	---
SD_GND04	SerDes 1 and SerDes 2 Ground	AG15	---	---	---
SD_GND05	SerDes 1 and SerDes 2 Ground	AG16	---	---	---
SD_GND06	SerDes 1 and SerDes 2 Ground	AG17	---	---	---
SD_GND07	SerDes 1 and SerDes 2 Ground	AG18	---	---	---
SD_GND08	SerDes 1 and SerDes 2 Ground	AG19	---	---	---
SD_GND09	SerDes 1 and SerDes 2 Ground	AG20	---	---	---
SD_GND10	SerDes 1 and SerDes 2 Ground	AG21	---	---	---
SD_GND11	SerDes 1 and SerDes 2 Ground	AG22	---	---	---
SD_GND12	SerDes 1 and SerDes 2 Ground	AG23	---	---	---
SD_GND13	SerDes 1 and SerDes 2 Ground	AG24	---	---	---
SD_GND14	SerDes 1 and SerDes 2 Ground	AG25	---	---	---
SD_GND15	SerDes 1 and SerDes 2 Ground	AH16	---	---	---
SD_GND16	SerDes 1 and SerDes 2 Ground	AH19	---	---	---
SD_GND17	SerDes 1 and SerDes 2 Ground	AH22	---	---	---
SD_GND18	SerDes 1 and SerDes 2 Ground	AH25	---	---	---
SD_GND19	SerDes 1 and SerDes 2 Ground	AH27	---	---	---
SD_GND20	SerDes 1 and SerDes 2 Ground	AJ12	---	---	---
SD_GND21	SerDes 1 and SerDes 2 Ground	AK10	---	---	---
SD_GND22	SerDes 1 and SerDes 2 Ground	AK11	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND23	SerDes 1 and SerDes 2 Ground	AK12	---	---	---
SD_GND24	SerDes 1 and SerDes 2 Ground	AK13	---	---	---
SD_GND25	SerDes 1 and SerDes 2 Ground	AK14	---	---	---
SD_GND26	SerDes 1 and SerDes 2 Ground	AK15	---	---	---
SD_GND27	SerDes 1 and SerDes 2 Ground	AK16	---	---	---
SD_GND28	SerDes 1 and SerDes 2 Ground	AK17	---	---	---
SD_GND29	SerDes 1 and SerDes 2 Ground	AK18	---	---	---
SD_GND30	SerDes 1 and SerDes 2 Ground	AK19	---	---	---
SD_GND31	SerDes 1 and SerDes 2 Ground	AK20	---	---	---
SD_GND32	SerDes 1 and SerDes 2 Ground	AK21	---	---	---
SD_GND33	SerDes 1 and SerDes 2 Ground	AK22	---	---	---
SD_GND34	SerDes 1 and SerDes 2 Ground	AK23	---	---	---
SD_GND35	SerDes 1 and SerDes 2 Ground	AK24	---	---	---
SD_GND36	SerDes 1 and SerDes 2 Ground	AK25	---	---	---
SD_GND37	SerDes 1 and SerDes 2 Ground	AK26	---	---	---
SD_GND38	SerDes 1 and SerDes 2 Ground	AK27	---	---	---
SD_GND39	SerDes 1 and SerDes 2 Ground	AL9	---	---	---
SD_GND40	SerDes 1 and SerDes 2 Ground	AL11	---	---	---
SD_GND41	SerDes 1 and SerDes 2 Ground	AL13	---	---	---
SD_GND42	SerDes 1 and SerDes 2 Ground	AL15	---	---	---
SD_GND43	SerDes 1 and SerDes 2 Ground	AL17	---	---	---
SD_GND44	SerDes 1 and SerDes 2 Ground	AL19	---	---	---
SD_GND45	SerDes 1 and SerDes 2 Ground	AL21	---	---	---
SD_GND46	SerDes 1 and SerDes 2 Ground	AL23	---	---	---
SD_GND47	SerDes 1 and SerDes 2 Ground	AL25	---	---	---
SD_GND48	SerDes 1 and SerDes 2 Ground	AL27	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND49	SerDes 1 and SerDes 2 Ground	AM9	---	---	---
SD_GND50	SerDes 1 and SerDes 2 Ground	AM11	---	---	---
SD_GND51	SerDes 1 and SerDes 2 Ground	AM13	---	---	---
SD_GND52	SerDes 1 and SerDes 2 Ground	AM15	---	---	---
SD_GND53	SerDes 1 and SerDes 2 Ground	AM17	---	---	---
SD_GND54	SerDes 1 and SerDes 2 Ground	AM18	---	---	---
SD_GND55	SerDes 1 and SerDes 2 Ground	AM19	---	---	---
SD_GND56	SerDes 1 and SerDes 2 Ground	AM21	---	---	---
SD_GND57	SerDes 1 and SerDes 2 Ground	AM23	---	---	---
SD_GND58	SerDes 1 and SerDes 2 Ground	AM25	---	---	---
SD_GND59	SerDes 1 and SerDes 2 Ground	AM27	---	---	---
SD_GND60	SerDes 1 and SerDes 2 Ground	AN8	---	---	---
SD_GND61	SerDes 1 and SerDes 2 Ground	AN10	---	---	---
SD_GND62	SerDes 1 and SerDes 2 Ground	AN12	---	---	---
SD_GND63	SerDes 1 and SerDes 2 Ground	AN13	---	---	---
SD_GND64	SerDes 1 and SerDes 2 Ground	AN14	---	---	---
SD_GND65	SerDes 1 and SerDes 2 Ground	AN16	---	---	---
SD_GND66	SerDes 1 and SerDes 2 Ground	AN18	---	---	---
SD_GND67	SerDes 1 and SerDes 2 Ground	AN20	---	---	---
SD_GND68	SerDes 1 and SerDes 2 Ground	AN22	---	---	---
SD_GND69	SerDes 1 and SerDes 2 Ground	AN23	---	---	---
SD_GND70	SerDes 1 and SerDes 2 Ground	AN24	---	---	---
SD_GND71	SerDes 1 and SerDes 2 Ground	AN26	---	---	---
SD_GND72	SerDes 1 and SerDes 2 Ground	AN28	---	---	---
SD_GND73	SerDes 1 and SerDes 2 Ground	AP8	---	---	---
SD_GND74	SerDes 1 and SerDes 2 Ground	AP10	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND75	SerDes 1 and SerDes 2 Ground	AP12	---	---	---
SD_GND76	SerDes 1 and SerDes 2 Ground	AP14	---	---	---
SD_GND77	SerDes 1 and SerDes 2 Ground	AP16	---	---	---
SD_GND78	SerDes 1 and SerDes 2 Ground	AP18	---	---	---
SD_GND79	SerDes 1 and SerDes 2 Ground	AP20	---	---	---
SD_GND80	SerDes 1 and SerDes 2 Ground	AP22	---	---	---
SD_GND81	SerDes 1 and SerDes 2 Ground	AP24	---	---	---
SD_GND82	SerDes 1 and SerDes 2 Ground	AP26	---	---	---
SD_GND83	SerDes 1 and SerDes 2 Ground	AP28	---	---	---
SD_GND84	SerDes 1 and SerDes 2 Ground	AR9	---	---	---
SD_GND85	SerDes 1 and SerDes 2 Ground	AR10	---	---	---
SD_GND86	SerDes 1 and SerDes 2 Ground	AR11	---	---	---
SD_GND87	SerDes 1 and SerDes 2 Ground	AR12	---	---	---
SD_GND88	SerDes 1 and SerDes 2 Ground	AR14	---	---	---
SD_GND89	SerDes 1 and SerDes 2 Ground	AR15	---	---	---
SD_GND90	SerDes 1 and SerDes 2 Ground	AR16	---	---	---
SD_GND91	SerDes 1 and SerDes 2 Ground	AR17	---	---	---
SD_GND92	SerDes 1 and SerDes 2 Ground	AR18	---	---	---
SD_GND93	SerDes 1 and SerDes 2 Ground	AR19	---	---	---
SD_GND94	SerDes 1 and SerDes 2 Ground	AR20	---	---	---
SD_GND95	SerDes 1 and SerDes 2 Ground	AR21	---	---	---
SD_GND96	SerDes 1 and SerDes 2 Ground	AR22	---	---	---
SD_GND97	SerDes 1 and SerDes 2 Ground	AR24	---	---	---
SD_GND98	SerDes 1 and SerDes 2 Ground	AR25	---	---	---
SD_GND99	SerDes 1 and SerDes 2 Ground	AR26	---	---	---
SD_GND100	SerDes 1 and SerDes 2 Ground	AR27	---	---	---
SD_GND101	SerDes 1 and SerDes 2 Ground	AT9	---	---	---
SD_GND102	SerDes 1 and SerDes 2 Ground	AT11	---	---	---
SD_GND103	SerDes 1 and SerDes 2 Ground	AT13	---	---	---
SD_GND104	SerDes 1 and SerDes 2 Ground	AT15	---	---	---
SD_GND105	SerDes 1 and SerDes 2 Ground	AT17	---	---	---
SD_GND106	SerDes 1 and SerDes 2 Ground	AT19	---	---	---
SD_GND107	SerDes 1 and SerDes 2 Ground	AT21	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND108	SerDes 1 and SerDes 2 Ground	AT23	---	---	---
SD_GND109	SerDes 1 and SerDes 2 Ground	AT25	---	---	---
SD_GND110	SerDes 1 and SerDes 2 Ground	AT27	---	---	---
SD_GND111	SerDes 1 and SerDes 2 Ground	AU9	---	---	---
SD_GND112	SerDes 1 and SerDes 2 Ground	AU11	---	---	---
SD_GND113	SerDes 1 and SerDes 2 Ground	AU13	---	---	---
SD_GND114	SerDes 1 and SerDes 2 Ground	AU15	---	---	---
SD_GND115	SerDes 1 and SerDes 2 Ground	AU17	---	---	---
SD_GND116	SerDes 1 and SerDes 2 Ground	AU19	---	---	---
SD_GND117	SerDes 1 and SerDes 2 Ground	AU21	---	---	---
SD_GND118	SerDes 1 and SerDes 2 Ground	AU23	---	---	---
SD_GND119	SerDes 1 and SerDes 2 Ground	AU25	---	---	---
SD_GND120	SerDes 1 and SerDes 2 Ground	AU27	---	---	---
SD_GND121	SerDes 1 and SerDes 2 Ground	AV8	---	---	---
SD_GND122	SerDes 1 and SerDes 2 Ground	AV10	---	---	---
SD_GND123	SerDes 1 and SerDes 2 Ground	AV12	---	---	---
SD_GND124	SerDes 1 and SerDes 2 Ground	AV14	---	---	---
SD_GND125	SerDes 1 and SerDes 2 Ground	AV16	---	---	---
SD_GND126	SerDes 1 and SerDes 2 Ground	AV18	---	---	---
SD_GND127	SerDes 1 and SerDes 2 Ground	AV20	---	---	---
SD_GND128	SerDes 1 and SerDes 2 Ground	AV22	---	---	---
SD_GND129	SerDes 1 and SerDes 2 Ground	AV24	---	---	---
SD_GND130	SerDes 1 and SerDes 2 Ground	AV26	---	---	---
SD_GND131	SerDes 1 and SerDes 2 Ground	AV28	---	---	---
SD_GND132	SerDes 1 and SerDes 2 Ground	AW8	---	---	---
SD_GND133	SerDes 1 and SerDes 2 Ground	AW10	---	---	---
SD_GND134	SerDes 1 and SerDes 2 Ground	AW12	---	---	---
SD_GND135	SerDes 1 and SerDes 2 Ground	AW14	---	---	---
SD_GND136	SerDes 1 and SerDes 2 Ground	AW16	---	---	---
SD_GND137	SerDes 1 and SerDes 2 Ground	AW18	---	---	---
SD_GND138	SerDes 1 and SerDes 2 Ground	AW20	---	---	---
SD_GND139	SerDes 1 and SerDes 2 Ground	AW22	---	---	---
SD_GND140	SerDes 1 and SerDes 2 Ground	AW24	---	---	---
SD_GND141	SerDes 1 and SerDes 2 Ground	AW26	---	---	---
SD_GND142	SerDes 1 and SerDes 2 Ground	AW28	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD3_GND01	SerDes3 core logic ground	A12	---	---	---
SD3_GND02	SerDes3 core logic ground	A14	---	---	---
SD3_GND03	SerDes3 core logic ground	A16	---	---	---
SD3_GND04	SerDes3 core logic ground	A18	---	---	---
SD3_GND05	SerDes3 core logic ground	A20	---	---	---
SD3_GND06	SerDes3 core logic ground	A22	---	---	---
SD3_GND07	SerDes3 core logic ground	B14	---	---	---
SD3_GND08	SerDes3 core logic ground	B16	---	---	---
SD3_GND09	SerDes3 core logic ground	B18	---	---	---
SD3_GND10	SerDes3 core logic ground	B20	---	---	---
SD3_GND11	SerDes3 core logic ground	B22	---	---	---
SD3_GND12	SerDes3 core logic ground	C13	---	---	---
SD3_GND13	SerDes3 core logic ground	C15	---	---	---
SD3_GND14	SerDes3 core logic ground	C17	---	---	---
SD3_GND15	SerDes3 core logic ground	C19	---	---	---
SD3_GND16	SerDes3 core logic ground	C21	---	---	---
SD3_GND17	SerDes3 core logic ground	D13	---	---	---
SD3_GND18	SerDes3 core logic ground	D15	---	---	---
SD3_GND19	SerDes3 core logic ground	D17	---	---	---
SD3_GND20	SerDes3 core logic ground	D19	---	---	---
SD3_GND21	SerDes3 core logic ground	D21	---	---	---
SD3_GND22	SerDes3 core logic ground	E13	---	---	---
SD3_GND23	SerDes3 core logic ground	E14	---	---	---
SD3_GND24	SerDes3 core logic ground	E15	---	---	---
SD3_GND25	SerDes3 core logic ground	E16	---	---	---
SD3_GND26	SerDes3 core logic ground	E18	---	---	---
SD3_GND27	SerDes3 core logic ground	E19	---	---	---
SD3_GND28	SerDes3 core logic ground	E20	---	---	---
SD3_GND29	SerDes3 core logic ground	E21	---	---	---
SD3_GND30	SerDes3 core logic ground	F12	---	---	---
SD3_GND31	SerDes3 core logic ground	F14	---	---	---
SD3_GND32	SerDes3 core logic ground	F16	---	---	---
SD3_GND33	SerDes3 core logic ground	F18	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD3_GND34	SerDes3 core logic ground	F20	---	---	---
SD3_GND35	SerDes3 core logic ground	F22	---	---	---
SD3_GND36	SerDes3 core logic ground	G12	---	---	---
SD3_GND37	SerDes3 core logic ground	G14	---	---	---
SD3_GND38	SerDes3 core logic ground	G16	---	---	---
SD3_GND39	SerDes3 core logic ground	G17	---	---	---
SD3_GND40	SerDes3 core logic ground	G18	---	---	---
SD3_GND41	SerDes3 core logic ground	G20	---	---	---
SD3_GND42	SerDes3 core logic ground	G22	---	---	---
SD3_GND43	SerDes3 core logic ground	H13	---	---	---
SD3_GND44	SerDes3 core logic ground	H15	---	---	---
SD3_GND45	SerDes3 core logic ground	H17	---	---	---
SD3_GND46	SerDes3 core logic ground	H19	---	---	---
SD3_GND47	SerDes3 core logic ground	H21	---	---	---
SD3_GND48	SerDes3 core logic ground	H22	---	---	---
SD3_GND49	SerDes3 core logic ground	J13	---	---	---
SD3_GND50	SerDes3 core logic ground	J15	---	---	---
SD3_GND51	SerDes3 core logic ground	J17	---	---	---
SD3_GND52	SerDes3 core logic ground	J19	---	---	---
SD3_GND53	SerDes3 core logic ground	J21	---	---	---
SD3_GND54	SerDes3 core logic ground	K13	---	---	---
SD3_GND55	SerDes3 core logic ground	K14	---	---	---
SD3_GND56	SerDes3 core logic ground	K15	---	---	---
SD3_GND57	SerDes3 core logic ground	K16	---	---	---
SD3_GND58	SerDes3 core logic ground	K17	---	---	---
SD3_GND59	SerDes3 core logic ground	K18	---	---	---
SD3_GND60	SerDes3 core logic ground	K19	---	---	---
SD3_GND61	SerDes3 core logic ground	K20	---	---	---
SD3_GND62	SerDes3 core logic ground	K21	---	---	---
SD3_GND63	SerDes3 core logic ground	L14	---	---	---
SD3_GND64	SerDes3 core logic ground	L21	---	---	---
SD3_GND65	SerDes3 core logic ground	N14	---	---	---
SD3_GND66	SerDes3 core logic ground	N15	---	---	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD3_GND67	SerDes3 core logic ground	N16	---	---	---
SD3_GND68	SerDes3 core logic ground	N17	---	---	---
SD3_GND69	SerDes3 core logic ground	N18	---	---	---
SD3_GND70	SerDes3 core logic ground	N19	---	---	---
SD3_GND71	SerDes3 core logic ground	N20	---	---	---
OVDD01	General I/O supply	N21	---	OV_{DD}	---
OVDD02	General I/O supply	N22	---	OV_{DD}	---
OVDD03	General I/O supply	N23	---	OV_{DD}	---
OVDD04	General I/O supply	N24	---	OV_{DD}	---
OVDD05	General I/O supply	N25	---	OV_{DD}	---
OVDD06	General I/O supply	R11	---	OV_{DD}	---
OVDD07	General I/O supply	T11	---	OV_{DD}	---
OVDD08	General I/O supply	U11	---	OV_{DD}	---
OVDD09	General I/O supply	V11	---	OV_{DD}	---
OVDD10	General I/O supply	W11	---	OV_{DD}	---
OVDD11	General I/O supply	Y12	---	OV_{DD}	---
OVDD12	General I/O supply	Y28	---	OV_{DD}	---
EVDD	SDHC 1.8V	T12	---	EV_{DD}	---
G1VDD01	DDR supply for port 1	A38	---	$G1V_{DD}$	---
G1VDD02	DDR supply for port 1	B36	---	$G1V_{DD}$	---
G1VDD03	DDR supply for port 1	B39	---	$G1V_{DD}$	---
G1VDD04	DDR supply for port 1	D38	---	$G1V_{DD}$	---
G1VDD05	DDR supply for port 1	F38	---	$G1V_{DD}$	---
G1VDD06	DDR supply for port 1	H38	---	$G1V_{DD}$	---
G1VDD07	DDR supply for port 1	J39	---	$G1V_{DD}$	---
G1VDD08	DDR supply for port 1	K37	---	$G1V_{DD}$	---
G1VDD09	DDR supply for port 1	L39	---	$G1V_{DD}$	---
G1VDD10	DDR supply for port 1	M37	---	$G1V_{DD}$	---
G1VDD11	DDR supply for port 1	N29	---	$G1V_{DD}$	---
G1VDD12	DDR supply for port 1	P29	---	$G1V_{DD}$	---
G1VDD13	DDR supply for port 1	P38	---	$G1V_{DD}$	---
G1VDD14	DDR supply for port 1	R29	---	$G1V_{DD}$	---
G1VDD15	DDR supply for port 1	T29	---	$G1V_{DD}$	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
G1VDD16	DDR supply for port 1	T38	---	$G1V_{DD}$	---
G1VDD17	DDR supply for port 1	U29	---	$G1V_{DD}$	---
G1VDD18	DDR supply for port 1	V29	---	$G1V_{DD}$	---
G1VDD19	DDR supply for port 1	V38	---	$G1V_{DD}$	---
G1VDD20	DDR supply for port 1	W29	---	$G1V_{DD}$	---
G2VDD01	DDR supply for port 2	AA29	---	$G2V_{DD}$	---
G2VDD02	DDR supply for port 2	AB29	---	$G2V_{DD}$	---
G2VDD03	DDR supply for port 2	AB38	---	$G2V_{DD}$	---
G2VDD04	DDR supply for port 2	AC29	---	$G2V_{DD}$	---
G2VDD05	DDR supply for port 2	AD29	---	$G2V_{DD}$	---
G2VDD06	DDR supply for port 2	AD38	---	$G2V_{DD}$	---
G2VDD07	DDR supply for port 2	AE29	---	$G2V_{DD}$	---
G2VDD08	DDR supply for port 2	AF29	---	$G2V_{DD}$	---
G2VDD09	DDR supply for port 2	AF38	---	$G2V_{DD}$	---
G2VDD10	DDR supply for port 2	AG29	---	$G2V_{DD}$	---
G2VDD11	DDR supply for port 2	AH37	---	$G2V_{DD}$	---
G2VDD12	DDR supply for port 2	AJ39	---	$G2V_{DD}$	---
G2VDD13	DDR supply for port 2	AK37	---	$G2V_{DD}$	---
G2VDD14	DDR supply for port 2	AL39	---	$G2V_{DD}$	---
G2VDD15	DDR supply for port 2	AM38	---	$G2V_{DD}$	---
G2VDD16	DDR supply for port 2	AP38	---	$G2V_{DD}$	---
G2VDD17	DDR supply for port 2	AT38	---	$G2V_{DD}$	---
G2VDD18	DDR supply for port 2	AV36	---	$G2V_{DD}$	---
G2VDD19	DDR supply for port 2	AV39	---	$G2V_{DD}$	---
G2VDD20	DDR supply for port 2	AW38	---	$G2V_{DD}$	---
FA1_CVL	Internal Use Only	AJ28	---	FA1_CVL	12
FA2_DVL	Internal Use Only	L28	---	FA2_DVL	12
PROG_MTR	Internal Use Only	M27	---	PROG_MTR	12
TA_PROG_SFP	SFP Fuse Programming Override supply	M26	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G23	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	N27	---	V_{DD}	---
VDD02	Supply for cores and platform	P22	---	V_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD03	Supply for cores and platform	P24	---	V_{DD}	---
VDD04	Supply for cores and platform	P26	---	V_{DD}	---
VDD05	Supply for cores and platform	R13	---	V_{DD}	---
VDD06	Supply for cores and platform	R15	---	V_{DD}	---
VDD07	Supply for cores and platform	R17	---	V_{DD}	---
VDD08	Supply for cores and platform	R19	---	V_{DD}	---
VDD09	Supply for cores and platform	R21	---	V_{DD}	---
VDD10	Supply for cores and platform	R23	---	V_{DD}	---
VDD11	Supply for cores and platform	R25	---	V_{DD}	---
VDD12	Supply for cores and platform	T14	---	V_{DD}	---
VDD13	Supply for cores and platform	T16	---	V_{DD}	---
VDD14	Supply for cores and platform	T18	---	V_{DD}	---
VDD15	Supply for cores and platform	T20	---	V_{DD}	---
VDD16	Supply for cores and platform	T22	---	V_{DD}	---
VDD17	Supply for cores and platform	T24	---	V_{DD}	---
VDD18	Supply for cores and platform	T26	---	V_{DD}	---
VDD19	Supply for cores and platform	U13	---	V_{DD}	---
VDD20	Supply for cores and platform	U15	---	V_{DD}	---
VDD21	Supply for cores and platform	U17	---	V_{DD}	---
VDD22	Supply for cores and platform	U19	---	V_{DD}	---
VDD23	Supply for cores and platform	U21	---	V_{DD}	---
VDD24	Supply for cores and platform	U23	---	V_{DD}	---
VDD25	Supply for cores and platform	U25	---	V_{DD}	---
VDD26	Supply for cores and platform	V12	---	V_{DD}	---
VDD27	Supply for cores and platform	V14	---	V_{DD}	---
VDD28	Supply for cores and platform	V16	---	V_{DD}	---
VDD29	Supply for cores and platform	V18	---	V_{DD}	---
VDD30	Supply for cores and platform	V20	---	V_{DD}	---
VDD31	Supply for cores and platform	V22	---	V_{DD}	---
VDD32	Supply for cores and platform	V24	---	V_{DD}	---
VDD33	Supply for cores and platform	V26	---	V_{DD}	---
VDD34	Supply for cores and platform	W13	---	V_{DD}	---
VDD35	Supply for cores and platform	W15	---	V_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD36	Supply for cores and platform	W17	---	V_{DD}	---
VDD37	Supply for cores and platform	W19	---	V_{DD}	---
VDD38	Supply for cores and platform	W21	---	V_{DD}	---
VDD39	Supply for cores and platform	W23	---	V_{DD}	---
VDD40	Supply for cores and platform	W25	---	V_{DD}	---
VDD41	Supply for cores and platform	Y14	---	V_{DD}	---
VDD42	Supply for cores and platform	Y16	---	V_{DD}	---
VDD43	Supply for cores and platform	Y18	---	V_{DD}	---
VDD44	Supply for cores and platform	Y20	---	V_{DD}	---
VDD45	Supply for cores and platform	Y22	---	V_{DD}	---
VDD46	Supply for cores and platform	Y24	---	V_{DD}	---
VDD47	Supply for cores and platform	Y26	---	V_{DD}	---
VDD48	Supply for cores and platform	AA13	---	V_{DD}	---
VDD49	Supply for cores and platform	AA15	---	V_{DD}	---
VDD50	Supply for cores and platform	AA17	---	V_{DD}	---
VDD51	Supply for cores and platform	AA19	---	V_{DD}	---
VDD52	Supply for cores and platform	AA21	---	V_{DD}	---
VDD53	Supply for cores and platform	AA23	---	V_{DD}	---
VDD54	Supply for cores and platform	AA25	---	V_{DD}	---
VDD55	Supply for cores and platform	AB14	---	V_{DD}	---
VDD56	Supply for cores and platform	AB16	---	V_{DD}	---
VDD57	Supply for cores and platform	AB18	---	V_{DD}	---
VDD58	Supply for cores and platform	AB20	---	V_{DD}	---
VDD59	Supply for cores and platform	AB22	---	V_{DD}	---
VDD60	Supply for cores and platform	AB24	---	V_{DD}	---
VDD61	Supply for cores and platform	AB26	---	V_{DD}	---
VDD62	Supply for cores and platform	AC13	---	V_{DD}	---
VDD63	Supply for cores and platform	AC15	---	V_{DD}	---
VDD64	Supply for cores and platform	AC17	---	V_{DD}	---
VDD65	Supply for cores and platform	AC19	---	V_{DD}	---
VDD66	Supply for cores and platform	AC21	---	V_{DD}	---
VDD67	Supply for cores and platform	AC23	---	V_{DD}	---
VDD68	Supply for cores and platform	AC25	---	V_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD69	Supply for cores and platform	AD12	---	V_{DD}	---
VDD70	Supply for cores and platform	AD14	---	V_{DD}	---
VDD71	Supply for cores and platform	AD16	---	V_{DD}	---
VDD72	Supply for cores and platform	AD18	---	V_{DD}	---
VDD73	Supply for cores and platform	AD20	---	V_{DD}	---
VDD74	Supply for cores and platform	AD22	---	V_{DD}	---
VDD75	Supply for cores and platform	AD24	---	V_{DD}	---
VDD76	Supply for cores and platform	AD26	---	V_{DD}	---
VDD77	Supply for cores and platform	AE13	---	V_{DD}	---
VDD78	Supply for cores and platform	AE15	---	V_{DD}	---
VDD79	Supply for cores and platform	AE17	---	V_{DD}	---
VDD80	Supply for cores and platform	AE19	---	V_{DD}	---
VDD81	Supply for cores and platform	AE21	---	V_{DD}	---
VDD82	Supply for cores and platform	AE23	---	V_{DD}	---
VDD83	Supply for cores and platform	AE25	---	V_{DD}	---
VDD84	Supply for cores and platform	AF26	---	V_{DD}	---
TA_BB_VDD	Low Power Security Monitor supply	J26	---	TA_BB_V_{DD}	---
SD3_SVDD1	SerDes3 core logic supply	P14	---	SD3_SV_{DD}	---
SD3_SVDD2	SerDes3 core logic supply	P15	---	SD3_SV_{DD}	---
SD3_SVDD3	SerDes3 core logic supply	P16	---	SD3_SV_{DD}	---
SD3_SVDD4	SerDes3 core logic supply	P17	---	SD3_SV_{DD}	---
SD3_SVDD5	SerDes3 core logic supply	P18	---	SD3_SV_{DD}	---
SD3_SVDD6	SerDes3 core logic supply	P19	---	SD3_SV_{DD}	---
SD3_SVDD7	SerDes3 core logic supply	P20	---	SD3_SV_{DD}	---
AVDD1	Platform PLL supply	J23	---	AV_{DD}	---
AVDD_SD3_PLLF	SerDes3 Analog PLL fast supply	L16	---	AV_{DD} _SD3_PLLF	---
AVDD_SD3_PLLS	SerDes3 Analog PLL slow supply	L19	---	AV_{DD}_SD3_PLLS	---
AVDD2	Core/platform PLL supply	L23	---	AV_{DD}	---
AVDD3	Core/platform PLL supply	L24	---	AV_{DD}	---
AVDD4	Core/platform PLL supply	L25	---	AV_{DD}	---
AVDD5	Core/platform PLL supply	L26	---	AV_{DD}	---
AVDD_D1	DDR PHY1 PLL supply	T28	---	AV_{DD} _D1	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
AVDD_D2	DDR PHY2 PLL supply	AC28	---	AV_{DD}_D2	---
AVDD_SD1_PLLS	SerDes1 Analog PLL slow supply	AJ16	---	AV_{DD}_SD1_PLLS	---
AVDD_SD1_PLLF	SerDes1 Analog PLL slow supply	AJ19	---	AV_{DD}_SD1_PLLF	---
AVDD_SD2_PLLF	SerDes2 Analog PLL fast supply	AJ22	---	AV_{DD}_SD2_PLLF	---
AVDD_SD2_PLLS	SerDes2 Analog PLL fast supply	AJ25	---	AV_{DD}_SD2_PLLS	---
USB_HVDD1	High voltage supply for High Speed operation	M12	---	USB_HV_{DD}	---
USB_HVDD2	High voltage supply for High Speed operation	N11	---	USB_HV_{DD}	---
USB_SDVDD1	Analog and digital high speed low voltage supply	P11	---	USB_SDV_{DD}	---
USB_SDVDD2	Analog and digital high speed low voltage supply	P12	---	USB_SDV_{DD}	---
USB_SVDD1	Analog and digital super speed low voltage supply	M13	---	USB_SV_{DD}	---
USB_SVDD2	Analog and digital super speed low voltage supply	N13	---	USB_SV_{DD}	---
SD_SVDD01	SerDes 1 and SerDes2 core logic supply	AF12	---	SD_SV_{DD}	---
SD_SVDD02	SerDes 1 and SerDes2 core logic supply	AF13	---	SD_SV_{DD}	---
SD_SVDD03	SerDes 1 and SerDes2 core logic supply	AF14	---	SD_SV_{DD}	---
SD_SVDD04	SerDes 1 and SerDes2 core logic supply	AF15	---	SD_SV_{DD}	---
SD_SVDD05	SerDes 1 and SerDes2 core logic supply	AF16	---	SD_SV_{DD}	---
SD_SVDD06	SerDes 1 and SerDes2 core logic supply	AF17	---	SD_SV_{DD}	---
SD_SVDD07	SerDes 1 and SerDes2 core logic supply	AF18	---	SD_SV_{DD}	---
SD_SVDD08	SerDes 1 and SerDes2 core logic supply	AF19	---	SD_SV_{DD}	---
SD_SVDD09	SerDes 1 and SerDes2 core logic supply	AF20	---	SD_SV_{DD}	---
SD_SVDD10	SerDes 1 and SerDes2 core logic supply	AF21	---	SD_SV_{DD}	---
SD_SVDD11	SerDes 1 and SerDes2 core logic supply	AF22	---	SD_SV_{DD}	---

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_SVDD12	SerDes 1 and SerDes2 core logic supply	AF23	---	SD_SV_{DD}	---
SD_SVDD13	SerDes 1 and SerDes2 core logic supply	AF24	---	SD_SV_{DD}	---
SD_SVDD14	SerDes 1 and SerDes2 core logic supply	AF25	---	SD_SV_{DD}	---
SD_OVDD01	SerDes1 transceiver supply	AH12	---	SD_OV_{DD}	---
SD_OVDD02	SerDes1 transceiver supply	AH13	---	SD_OV_{DD}	---
SD_OVDD03	SerDes1 transceiver supply	AH14	---	SD_OV_{DD}	---
SD_OVDD04	SerDes1 transceiver supply	AH15	---	SD_OV_{DD}	---
SD_OVDD05	SerDes1 transceiver supply	AH17	---	SD_OV_{DD}	---
SD_OVDD06	SerDes1 transceiver supply	AH18	---	SD_OV_{DD}	---
SD_OVDD07	SerDes1 transceiver supply	AH20	---	SD_OV_{DD}	---
SD_OVDD08	SerDes1 transceiver supply	AH21	---	SD_OV_{DD}	---
SD_OVDD09	SerDes1 transceiver supply	AH23	---	SD_OV_{DD}	---
SD_OVDD10	SerDes1 transceiver supply	AH24	---	SD_OV_{DD}	---
SD3_OVDD1	SerDes3 transceiver supply	M14	---	$SD3\_OV_{DD}$	---
SD3_OVDD2	SerDes3 transceiver supply	M15	---	$SD3\_OV_{DD}$	---
SD3_OVDD3	SerDes3 transceiver supply	M16	---	$SD3\_OV_{DD}$	---
SD3_OVDD4	SerDes3 transceiver supply	M17	---	$SD3\_OV_{DD}$	---
SD3_OVDD5	SerDes3 transceiver supply	M18	---	$SD3\_OV_{DD}$	---
SD3_OVDD6	SerDes3 transceiver supply	M19	---	$SD3\_OV_{DD}$	---
SD3_OVDD7	SerDes3 transceiver supply	M20	---	$SD3\_OV_{DD}$	---
SENSEVDD_CA	VDD Sense pin	J25	---	SENSEVDD_CA	---
SENSEVDD_CB	VDD Sense pin	AG27	---	SENSEVDD_CB	---
SENSEVDD_PL	VDD Sense pin	AG10	---	SENSEVDD_PL	---
No Connection Pins					
NC_K11	No Connection	K11	---	---	10
NC_K22	No Connection	K22	---	---	10
NC_L8	No Connection	L8	---	---	10
NC_L9	No Connection	L9	---	---	10
NC_M5	No Connection	M5	---	---	10
NC_P28	No Connection	P28	---	---	10
NC_R5	No Connection	R5	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_R6	No Connection	R6	---	---	10
NC_R7	No Connection	R7	---	---	10
NC_R8	No Connection	R8	---	---	10
NC_R9	No Connection	R9	---	---	10
NC_R27	No Connection	R27	---	---	10
NC_T2	No Connection	T2	---	---	10
NC_T4	No Connection	T4	---	---	10
NC_T5	No Connection	T5	---	---	10
NC_T7	No Connection	T7	---	---	10
NC_T8	No Connection	T8	---	---	10
NC_T9	No Connection	T9	---	---	10
NC_U1	No Connection	U1	---	---	10
NC_U2	No Connection	U2	---	---	10
NC_U3	No Connection	U3	---	---	10
NC_U5	No Connection	U5	---	---	10
NC_U6	No Connection	U6	---	---	10
NC_U7	No Connection	U7	---	---	10
NC_U9	No Connection	U9	---	---	10
NC_U27	No Connection	U27	---	---	10
NC_V1	No Connection	V1	---	---	10
NC_V2	No Connection	V2	---	---	10
NC_V3	No Connection	V3	---	---	10
NC_V4	No Connection	V4	---	---	10
NC_V5	No Connection	V5	---	---	10
NC_V7	No Connection	V7	---	---	10
NC_V8	No Connection	V8	---	---	10
NC_V9	No Connection	V9	---	---	10
NC_V28	No Connection	V28	---	---	10
NC_W1	No Connection	W1	---	---	10
NC_W2	No Connection	W2	---	---	10
NC_W3	No Connection	W3	---	---	10
NC_W5	No Connection	W5	---	---	10
NC_W6	No Connection	W6	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_W7	No Connection	W7	---	---	10
NC_W9	No Connection	W9	---	---	10
NC_W27	No Connection	W27	---	---	10
NC_Y1	No Connection	Y1	---	---	10
NC_Y2	No Connection	Y2	---	---	10
NC_Y3	No Connection	Y3	---	---	10
NC_Y4	No Connection	Y4	---	---	10
NC_Y5	No Connection	Y5	---	---	10
NC_Y7	No Connection	Y7	---	---	10
NC_Y8	No Connection	Y8	---	---	10
NC_Y9	No Connection	Y9	---	---	10
NC_Y11	No Connection	Y11	---	---	10
NC_AA1	No Connection	AA1	---	---	10
NC_AA2	No Connection	AA2	---	---	10
NC_AA3	No Connection	AA3	---	---	10
NC_AA5	No Connection	AA5	---	---	10
NC_AA6	No Connection	AA6	---	---	10
NC_AA7	No Connection	AA7	---	---	10
NC_AA9	No Connection	AA9	---	---	10
NC_AA11	No Connection	AA11	---	---	10
NC_AA27	No Connection	AA27	---	---	10
NC_AB1	No Connection	AB1	---	---	10
NC_AB2	No Connection	AB2	---	---	10
NC_AB3	No Connection	AB3	---	---	10
NC_AB4	No Connection	AB4	---	---	10
NC_AB5	No Connection	AB5	---	---	10
NC_AB7	No Connection	AB7	---	---	10
NC_AB8	No Connection	AB8	---	---	10
NC_AB9	No Connection	AB9	---	---	10
NC_AB11	No Connection	AB11	---	---	10
NC_AB12	No Connection	AB12	---	---	10
NC_AC1	No Connection	AC1	---	---	10
NC_AC2	No Connection	AC2	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_AC3	No Connection	AC3	---	---	10
NC_AC5	No Connection	AC5	---	---	10
NC_AC6	No Connection	AC6	---	---	10
NC_AC7	No Connection	AC7	---	---	10
NC_AC9	No Connection	AC9	---	---	10
NC_AC11	No Connection	AC11	---	---	10
NC_AC12	No Connection	AC12	---	---	10
NC_AC27	No Connection	AC27	---	---	10
NC_AD1	No Connection	AD1	---	---	10
NC_AD2	No Connection	AD2	---	---	10
NC_AD3	No Connection	AD3	---	---	10
NC_AD4	No Connection	AD4	---	---	10
NC_AD5	No Connection	AD5	---	---	10
NC_AD7	No Connection	AD7	---	---	10
NC_AD8	No Connection	AD8	---	---	10
NC_AD9	No Connection	AD9	---	---	10
NC_AD11	No Connection	AD11	---	---	10
NC_AD28	No Connection	AD28	---	---	10
NC_AE1	No Connection	AE1	---	---	10
NC_AE2	No Connection	AE2	---	---	10
NC_AE3	No Connection	AE3	---	---	10
NC_AE5	No Connection	AE5	---	---	10
NC_AE6	No Connection	AE6	---	---	10
NC_AE7	No Connection	AE7	---	---	10
NC_AE9	No Connection	AE9	---	---	10
NC_AE11	No Connection	AE11	---	---	10
NC_AE27	No Connection	AE27	---	---	10
NC_AF1	No Connection	AF1	---	---	10
NC_AF2	No Connection	AF2	---	---	10
NC_AF3	No Connection	AF3	---	---	10
NC_AF4	No Connection	AF4	---	---	10
NC_AF5	No Connection	AF5	---	---	10
NC_AF7	No Connection	AF7	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_AF8	No Connection	AF8	---	---	10
NC_AF9	No Connection	AF9	---	---	10
NC_AF11	No Connection	AF11	---	---	10
NC_AF28	No Connection	AF28	---	---	10
NC_AG1	No Connection	AG1	---	---	10
NC_AG2	No Connection	AG2	---	---	10
NC_AG3	No Connection	AG3	---	---	10
NC_AG5	No Connection	AG5	---	---	10
NC_AG6	No Connection	AG6	---	---	10
NC_AG7	No Connection	AG7	---	---	10
NC_AG8	No Connection	AG8	---	---	10
NC_AG28	No Connection	AG28	---	---	10
NC_AH1	No Connection	AH1	---	---	10
NC_AH2	No Connection	AH2	---	---	10
NC_AH3	No Connection	AH3	---	---	10
NC_AH4	No Connection	AH4	---	---	10
NC_AH5	No Connection	AH5	---	---	10
NC_AH6	No Connection	AH6	---	---	10
NC_AH8	No Connection	AH8	---	---	10
NC_AH9	No Connection	AH9	---	---	10
NC_AH10	No Connection	AH10	---	---	10
NC_AJ1	No Connection	AJ1	---	---	10
NC_AJ2	No Connection	AJ2	---	---	10
NC_AJ3	No Connection	AJ3	---	---	10
NC_AJ4	No Connection	AJ4	---	---	10
NC_AJ6	No Connection	AJ6	---	---	10
NC_AJ7	No Connection	AJ7	---	---	10
NC_AJ8	No Connection	AJ8	---	---	10
NC_AJ9	No Connection	AJ9	---	---	10
NC_AK1	No Connection	AK1	---	---	10
NC_AK2	No Connection	AK2	---	---	10
NC_AK3	No Connection	AK3	---	---	10
NC_AK5	No Connection	AK5	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_AK6	No Connection	AK6	---	---	10
NC_AK8	No Connection	AK8	---	---	10
NC_AL1	No Connection	AL1	---	---	10
NC_AL2	No Connection	AL2	---	---	10
NC_AL3	No Connection	AL3	---	---	10
NC_AL4	No Connection	AL4	---	---	10
NC_AL6	No Connection	AL6	---	---	10
NC_AL7	No Connection	AL7	---	---	10
NC_AL8	No Connection	AL8	---	---	10
NC_AL18	No Connection	AL18	---	---	10
NC_AM1	No Connection	AM1	---	---	10
NC_AM2	No Connection	AM2	---	---	10
NC_AM4	No Connection	AM4	---	---	10
NC_AM5	No Connection	AM5	---	---	10
NC_AM6	No Connection	AM6	---	---	10
NC_AM7	No Connection	AM7	---	---	10
NC_AN1	No Connection	AN1	---	---	10
NC_AN2	No Connection	AN2	---	---	10
NC_AN3	No Connection	AN3	---	---	10
NC_AN4	No Connection	AN4	---	---	10
NC_AN5	No Connection	AN5	---	---	10
NC_AN7	No Connection	AN7	---	---	10
NC_AP1	No Connection	AP1	---	---	10
NC_AP2	No Connection	AP2	---	---	10
NC_AP4	No Connection	AP4	---	---	10
NC_AP6	No Connection	AP6	---	---	10
NC_AP7	No Connection	AP7	---	---	10
NC_AR1	No Connection	AR1	---	---	10
NC_AR2	No Connection	AR2	---	---	10
NC_AR3	No Connection	AR3	---	---	10
NC_AR4	No Connection	AR4	---	---	10
NC_AR5	No Connection	AR5	---	---	10
NC_AR6	No Connection	AR6	---	---	10

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
NC_AR7	No Connection	AR7	---	---	10
NC_AT1	No Connection	AT1	---	---	10
NC_AT2	No Connection	AT2	---	---	10
NC_AT3	No Connection	AT3	---	---	10
NC_AT5	No Connection	AT5	---	---	10
NC_AT7	No Connection	AT7	---	---	10
NC_AT8	No Connection	AT8	---	---	10
NC_AU1	No Connection	AU1	---	---	10
NC_AU2	No Connection	AU2	---	---	10
NC_AU4	No Connection	AU4	---	---	10
NC_AU5	No Connection	AU5	---	---	10
NC_AU6	No Connection	AU6	---	---	10
NC_AU7	No Connection	AU7	---	---	10
NC_AV1	No Connection	AV1	---	---	10
NC_AV2	No Connection	AV2	---	---	10
NC_AV3	No Connection	AV3	---	---	10
NC_AV5	No Connection	AV5	---	---	10
NC_AV7	No Connection	AV7	---	---	10
NC_AW3	No Connection	AW3	---	---	10
NC_AW4	No Connection	AW4	---	---	10
NC_AW5	No Connection	AW5	---	---	10
NC_AW6	No Connection	AW6	---	---	10
NC_AW7	No Connection	AW7	---	---	10

Notes:

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
2. This output is actively driven during reset rather than being tri-stated during reset.
3. MDIC is grounded through a 240 Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 240 Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. This pin is used for automatic calibration of the DDR4 IOs. The MDIC pin must be connected to 240 Ω precision 1% resistors.
4. This pin is a power-on-reset (POR) configuration pin. It has a weak internal pull-up resistor that is enabled during POR state only. The internal pull-up resistor allows the default value to be captured at POR de-assertion. This pull-up can be overpowered by an external pull-down resistor in case a change in the default value is required. Refer to the Design Checklist for details.
5. Recommend that a weak pull-up resistor be placed on this pin to the respective power supply. Refer to the Design Checklist for details.
6. This pin is an open-drain signal.

7. This pin has a weak internal pull-up P-FET that is always enabled.
8. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.
9. This pin requires a 200 Ω ± 1% pull-up resistor to respective power-supply.
10. Do not connect. These pins should be left floating.
11. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
12. These pins must be pulled to ground (GND).
13. This pin requires a 1.5 kΩ ± 1% pull-up resistor to respective power-supply.
14. These pins should be tied to ground if the diode is not utilized for temperature monitoring.
15. Attach 200 Ω ± 1% 100-ppm/C precision resistor-to-ground. Voltage range is between 0 to 250 mV.
16. Refer to the design checklist.
17. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
18. A 30.1 kΩ (±1%, ±100 ppm/ºC) resistor is required between the USBn_VBUS and the 5 V supply.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

2.2.1 DDR1 pins

See the DDR1 pins.

2.2.2 DDR2 pins

See the DDR2 pins.

2.2.3 I2C1 pins

See the I2C1 pins.

2.2.4 I2C2 pins

See the I2C2 pins.

2.2.5 I2C3 pins

See the I2C3 pins.

2.2.6 I2C4 pins

See the I2C4 pins.

2.2.7 I2C5 pins

See the I2C5 pins.

2.2.8 I2C6 pins

See the I2C6 pins.

2.2.9 I2C7 pins

See the I2C7 pins.

2.2.10 I2C8 pins

See the I2C8 pins.

2.2.11 XSPI1 pins

See the XSPI1 pins.

2.2.12 eSDHC1 pins

See the eSDHC1 pins.

2.2.13 eSDHC2 pins

See the eSDHC2 pins.

2.2.14 UART pins

See the UART pins.

2.2.15 Interrupt controller pins

See the Interrupt Controller pins.

2.2.16 Trust pins

See the Trust pins.

2.2.17 System control pins

See the system control pins.

2.2.18 Clocking pins

See the Clocking pins.

2.2.19 Debug pins

See the Debug pins.

2.2.20 DFT pins

See the DFT pins.

2.2.21 JTAG pins

See the JTAG pins.

2.2.22 Analog pins

See the Analog pins.

2.2.23 SerDes1 pins

See the SerDes1 pins.

2.2.24 SerDes2 pins

See the SerDes2 pins.

2.2.25 SerDes3 pins

See the SerDes3 pins.

2.2.26 USB PHY pins

See the USB PHY pins.

2.2.27 EC1 pins

See the EC1 pins.

2.2.28 EC2 pins

See the EC2 pins.

2.2.29 GPIO pins

See the GPIO pins.

2.2.30 FlexTimer pins

See the FlexTimer pins.

2.2.31 CAN pins

See the CAN pins.

2.2.32 Power-on-reset configuration pins

See the POR configuration pins.

2.2.33 SPI1 pins

See the SPI1 pins.

2.2.34 SPI2 pins

See the SPI2 pins.

2.2.35 SPI3 pins

See the SPI3 pins.

2.2.36 IEEE 1588 pins

See the IEEE 1588 pins.

2.2.37 Power and ground pins

See the Power and Ground pins.

2.2.38 No connect pins

See the NC pins.

3 ELECTRICAL CHARACTERISTICS

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings

Table 3. Absolute maximum ratings [5]

Characteristic	Symbol	Min	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3	0.88	V	1
PLL supply voltage (core, platform, DDR)	AV_{DD}, AV_{DD}_D1, AV_{DD}_D2	-0.3	1.98	V	-
SerDes analog PLL fast and PLL slow supply voltage	$AV_{DD}\_SD1\_PLLF$, $AV_{DD}\_SD2\_PLLF$, $AV_{DD}\_SD3\_PLLF$, $AV_{DD}\_SD1\_PLLS$, $AV_{DD}\_SD2\_PLLS$, $AV_{DD}\_SD3\_PLLS$	-0.3	0.99	V	-
SerDes 1 and SerDes 2 core logic supply	SD_SV_{DD}	-0.3	0.99	V	-
SerDes 3 core logic supply	$SD3\_SV_{DD}$	-0.3	0.99	V	-
SerDes 1 and SerDes 2 transceiver supply	SD_OV_{DD}	-0.3	1.98	V	-
SerDes 3 transceiver supply	$SD3\_OV_{DD}$	-0.3	1.98	V	-

Characteristic	Symbol	Min	Max Value	Unit	Notes
SFP fuse programming	TA_PROG_SFP	-0.3	1.98	V	-
Thermal monitor unit supply	TH_V_{DD}	-0.3	1.98	V	-
General I/O supply	OV_{DD}	-0.3	1.98	V	-
eSDHC1 supply (also includes some GPIO1 and SPI1 pins)	EV_{DD}	-0.3	1.8 V + 90 mV	V	-
DDR4 DRAM I/O voltage	$G1V_{DD}$, $G2V_{DD}$	-0.3	1.32	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	-0.3	3.63	V	-
USB PHY analog and digital HS supply	USB_SDV_{DD}	-0.3	0.88	V	-
USB PHY analog and digital SS supply	USB_SV_{DD}	-0.3	0.88	V	-
Low power security monitor supply	$TA\_BB\_V_{DD}$	-0.3	0.88	V	-
Input voltage for DDR4 DRAM signals	MV_{IN}	-0.3	GV_{DD} + 0.3	V	2
Input voltage for general I/O signals and interfaces powered by OV_{DD}	OV_{IN}	-0.3	OV_{DD} + 0.3	V	3, 4
Input voltage for SerDes signals	SV_{IN}	-0.4	SD_SV_{DD} + 0.3	V	4
Input voltage for USB PHY 3.3 HS signals	USB_HV_{IN}	-0.3	USB_HV_{DD} + 0.3	V	4
Input voltage for USB PHY SS signals	USB_SV_{IN}	-0.3	USB_SV_{DD} + 0.3	V	4
Input voltage for USBn_ID	USB_ID_{IN}	-0.3	1.8	V	
Input voltage for USBn_VBUS	USB_VBUS_{IN}	-0.3	3.3	V	
Input voltage for eSDHC1, GPIO1, and SPI1 signals powered by EV_{DD}	EV_{IN}	-0.3	EV_{DD} + 0.3	V	-
Storage temperature range	T_{STG}	-55	150	°C	6

Notes:

1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M, O, S)V_{IN}, and $USBn\_HV_{IN}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in the Overshoot/undershoot voltage figure at the end of this section.
5. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operations at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
6. Not to exceed 1008 hours cumulative at 150°C.

3.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip.

Warning

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed

Table 4. Recommended operating conditions 6

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VID core and platform supply voltage at boot	V_{DD}	0.850 - 30 mV	0.850	0.850 + 30 mV	V	1, 2, 3
VID core and platform supply voltage during normal operation	V_{DD}	VID - 30 mV	VID	VID + 30 mV	V	1, 2, 3
PLL supply voltage (core, platform, DDR)	AV_{DD}, AV_{DD}_D1, AV_{DD}_D2	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	4
SerDes analog PLL fast and PLL slow supply voltage	AV_{DD}_SD1_PLLF, AV_{DD}_SD2_PLLF, AV_{DD}_SD3_PLLF, AV_{DD}_SD1_PLLS, AV_{DD}_SD2_PLLS, AV_{DD}_SD3_PLLS	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	-
SerDes 1 and SerDes 2 core logic supply	SD_SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	-
SerDes 3 core logic supply	SD3_SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	-
SerDes 1 and SerDes 2 transceiver supply	SD_OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
SerDes 3 transceiver supply	SD3_OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
SFP fuse programming	TA_PROG_SFP	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
Thermal monitor unit supply	TH_V_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
General I/O supply	OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
eSDHC1 supply (also includes some GPIO1 and SPI1 pins)	EV_{DD}	1.8 V - 90 mV	1.8 V	1.8 V + 90 mV	V	-
DDR4 DRAM I/O voltage	G1V_{DD}, G2V_{DD}	1.2V - 60 mV	1.2	1.2 V + 60 mV	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	3.3 - 165 mV	3.3	3.3 V + 165 mV	V	-
USB PHY analog and digital HS supply	USB_SDV_{DD}	0.8 V - 30 mV	0.8	0.8 V + 50 mV	V	-

Parameter	Symbol	Min	Typ	Max	Unit	Notes
USB PHY analog and digital SS supply	USB_SV_{DD}	0.8 V - 30 mV	0.8	0.8 V + 50 mV	V	-
Low power supply monitor when connected to V_{DD} supply	$TA\_BB\_V_{DD}$	VDD	VDD	VDD	V	-
Low power supply monitor when powered by battery	$TA\_BB\_V_{DD}$	0.8 V - 30 mV	0.8	0.8+50mV	V	-
Input voltage for DDR4 DRAM signals	MV_{IN}		GND to GnV_{DD}		V	-
Input voltage for general I/O signals and interfaces powered by OV_{DD}	OV_{IN}	-	GND to OV_{DD}	-	V	-
Input voltage for SerDes signals	SV_{IN}	-	-400 mV to +400 mV	-	V	-
Input voltage for USB PHY 3.3 HS signals	USB_HV_{IN}	-	GND to USB_HV_{DD}	-	V	-
Input voltage for USB PHY SS signals	USB_SV_{IN}	-	GND to USB_SV_{DD}			
Input voltage for eSDHC1, GPIO1, and SPI1 signals powered by EV_{DD}	EV_{IN}	-	GND to EV_{DD}	-	V	-
Range "A" operating temperature	T_A/T_J	T_A = -40	-	T_J = 105	°C	-
Range "F" operating temperature	T_A/T_J	T_A = -40	-	T_J = 125	°C	-
Range "M" operating temperature	T_A/T_J	T_A = -55	-	T_A = 125	°C	-
Secure boot fuse programming operating temperature range	T_A/T_J	T_A = 0	-	T_J = 70	°C	5

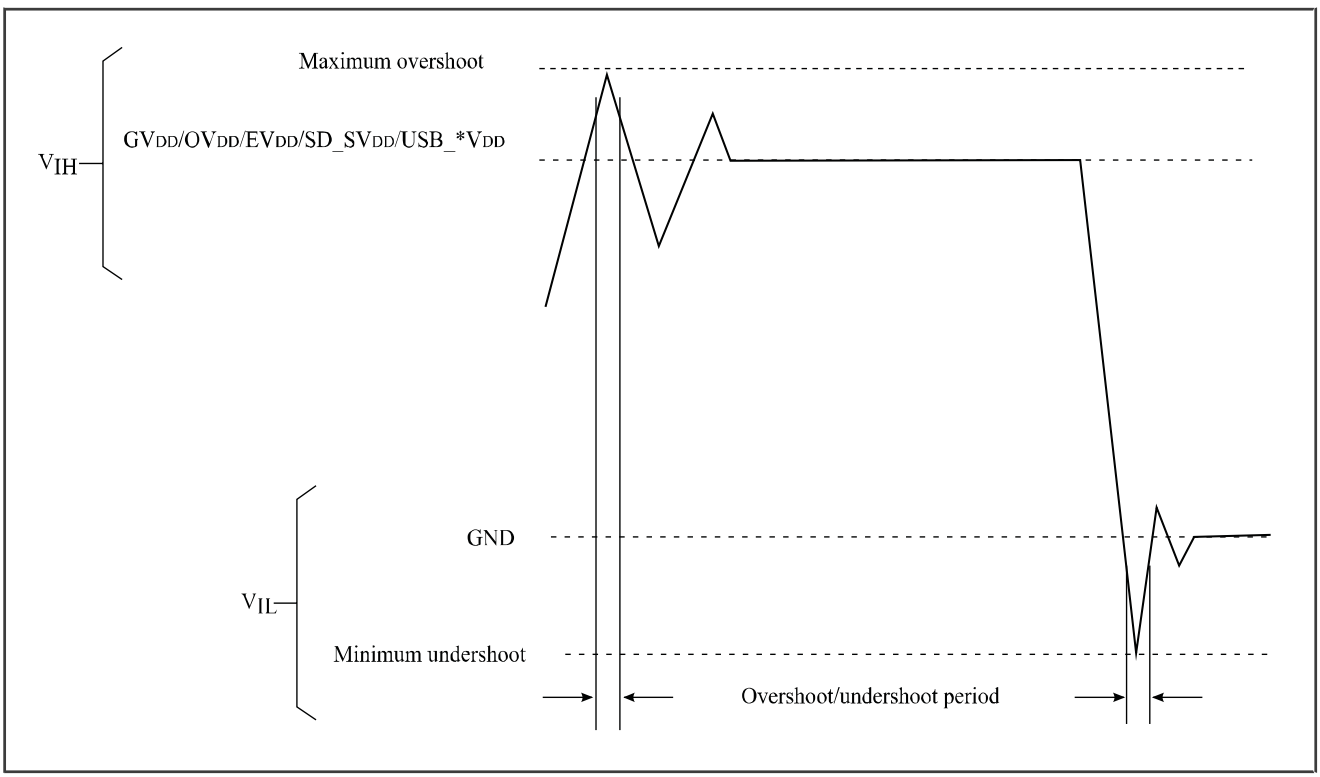
Notes:

1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
2. Operation at 0.88V is allowable for up to 25 ms at initial power on.
3. Voltage ID (VID) operating range is between 0.775 V to 0.85 V. It is highly recommended to select a PMBus style regulator with a V_{out} range of at least 0.7 V to 0.9 V, with resolution of 12.5 mV or better.
4. AV_{DD}, AV_{DD}_D1, and AV_{DD}_D2 are measured at the input to the filter and not at the pin of the device.
5. TA_PROG_SFP must be supplied 1.8V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power Sequencing.
6. See Figure 9.
7. Only available on automotive grade parts.
8. The T_J must not exceed 105°C. Proper thermal solution should be applied to meet this requirement.

See the Recommended operating conditions table for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in the Recommended operating conditions table. The input voltage threshold scales with respect to the associated I/O supply voltage. OVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the internally generated VREF signal. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip

Figure 9. Overshoot/undershoot voltage for GVDD/OVDD/EVDD/SD_SVDD/USB_HVDD/USB_SVDD



Note:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period

3.1.3 Output drive capabilities

This chip provides information on the characteristics of the output driver strengths.

Table 5. Output drive capability[1,2]

Driver Type	Minimum 1	Typ	Maximum 2	Supply_Vol tage
General I/O signals	30	45	60	OVDD = 1.8V

Notes:

1. Minimum values reflect estimated numbers based on best-case processed device.
2. Maximum values reflect estimated numbers based on worst-case processed device.

3.2 General AC timing

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 6. General AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1

Note

1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply.

3.3 Power sequencing

For power up, the following sequence should be followed:

1. During V_{DD} ramping, PORESET_B must be held low and TA_PROG_SFP must be grounded. All other power supplies (G*n*V_{DD}, OV_{DD}, EV_{DD}, USB_HV_{DD}, USB_SV_{DD}, USB_SDV_{DD}, SD_SV_{DD}, SD_OV_{DD}, $TA\_BB\_V_{DD}$, TH_V_{DD}, AV_{DD} (cores, platform, DDR), and AV_{DD}_SD*m*_PLL*n*) have no ordering requirement with respect to one another and with respect to V_{DD}. All supplies must be at their stable values within 400 ms.
2. Negate PORESET_B input as long as the required assertion/hold time has been met per the RESET initialization table.
3. For secure boot fuse programming, use the following steps:
   a. After negation of PORESET_B, drive TA_PROG_SFP = 1.80 V after a required minimum delay per Table 7.
   b. After fuse programming is completed, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7. See Security fuse processor, for additional details.

NOTE

If using Trust Architecture Security Monitor battery backed features, prior to V_{DD} ramping up to 0.5 V level, ensure that SD_SV_{DD} is properly ramped and DIFF_SYSCLK_P / DIFF_SYSCLK_N is running. The clock should have a frequency of 100 MHz

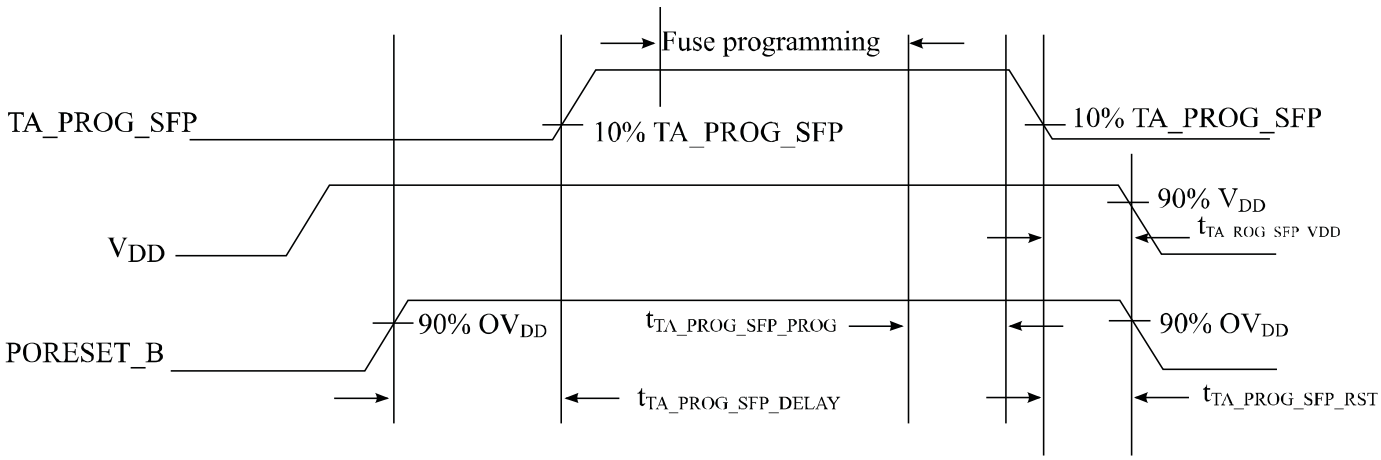
Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates.

This figure provides the TA_PROG_SFP timing diagram.

Figure 10. TA_PROG_SFP timing diagram



NOTE: TA_PROG_SFP must be stable at 1.80 V prior to initiating fuse programming.

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 7. TA_PROG_SFP timing (5)

Drivertype	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	100	—	SYSCLKs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	—	µs	2
$t_{TA\_PROG\_SFP\_VDD}$	0	—	µs	3
$t_{TA\_PROG\_SFP\_RST}$	0	—	µs	4

Notes

1. Delay required from the de-assertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.
2. Delay required from fuse programming finished to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.80 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is completed, it is required to return TA_PROG_SFP = GND.
3. Delay required from TA_PROG_SFP ramp down complete to V_{DD} ramp down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} is at 90% V_{DD}.
4. Delay required from TA_PROG_SFP ramp down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

Warning

TA_PROG_SFP ramp up slew rate must not exceed 18,000V/s. Ramp down does not have a slew rate constraint.

3.4 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.3 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 8. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies except those noted below	—	25	V/ms	1, 2
Required ramp rate for GnV_{DD} and AV_{DD}_Dn supplies	—	5	V/ms	1, 2
Required ramp rate for TA_PROG_SFP supply	—	18	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Recommended Operating Conditions).

3.6 Power characteristics

This table shows the thermal VDD power at 85°C.

Table 9. Thermal VDD power at 85°C

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency (MHz)	DDR data rate (MHz)	Power (W)		
				LX2160A	LX2120A	LX2080A
2.2 GHz	1500	750	3200	26.9	24.4	21.8
2.0 GHz	1400	700	2900	20.4	18.0	15.7
1.8 GHz	1300	650	2600	19.1	17.0	14.8

Note:

1. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform. VDD must run at VID voltage level.

This table shows the estimated power dissipation on the TA_BB_V_{DD} supply for the LX2160A at allowable voltage levels.

Table 10. TA_BB_VDD power dissipation

Supply	Maximum	Unit	Notes
TA_BB_V_{DD} (LX2xx0A off, 70°C)	36	uW	1
TA_BB_V_{DD} (LX2xx0A off, 40°C)	5	uW	1

Note:

1. When the device is off, TA_BB_VDD may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_V_{DD} to battery when SoC powered down. See the device reference manual trust architecture chapter for more information.

3.7 Input clocks

3.7.1 USB reference clock specifications

The reference clock of the USB PHY is the DIFF_SYSCLK_P/DIFF_SYSCLK_N. Refer to the Differential system clock (DIFF_SYSCLK_P/DIFF_SYSCLK_N) timing specifications for the USB AC timing specifications.

3.7.2 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with OV_{DD} = 1.8 V.

Table 11. EC_GTX_CLK125 DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OVDD	—	—	V	2
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	µA	3

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min VIL and max VIH values are based on the respective min and max VIN values found in Recommended Operating Conditions.
3. The symbol VIN, in this case, represents the OV_{IN} symbol referenced in Recommended Operating Conditions.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 12. EC_GTX_CLK125 AC timing specifications (1)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3

Notes:

1. At recommended operating conditions with OV_{DD} = 1.8 V ± 90mV. See Recommended Operating Conditions.
2. Rise and fall times for EC_GTX_CLK125 are measured from 0.36 and 1.44 V for OV_{DD} = 1.8 V
3. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks. The frequency of EC*n*_RX_CLK (input) should not exceed the frequency of EC_GTX_CLK125/EC*n*_TX_CLK (input) by more than 300 ppm.

3.7.3 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.3.1 DDRCLK DC electrical characteristics

This table provides the DDR clock (DDRCLK) DC electrical characteristics.

Table 13. DDRCLK DC electrical characteristics (3)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (VIN= 0V or VIN = OVDD)	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended Operating Conditions.
3. At recommended operating conditions with OV_{DD} = 1.8 V. See Recommended Operating Conditions.

3.7.3.2 DDRCLK AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 14. DDRCLK AC timing specifications5

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}		100		MHz	1, 2
DDRCLK frequency offset	F_{DDRCLK_OFFSET}	-300.0	—	300.0	ppm	
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	42.5	50	57.5	%	2
DDRCLK slew rate	—	1.0	—	10	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	4

Notes:

1. **Caution:** The memory controller complex PLL multiplier/ratio (RCW[MEM_PLL_RAT]) must be chosen such that the resulting DDR data rate does not exceed its respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from 0.25 x OV_{DD} to 0.75 x OV_{DD}.
4. Peak period jitter is calculated according to the JEDEC standard expression 8.22 * RMS jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V. See Recommended Operating Conditions.

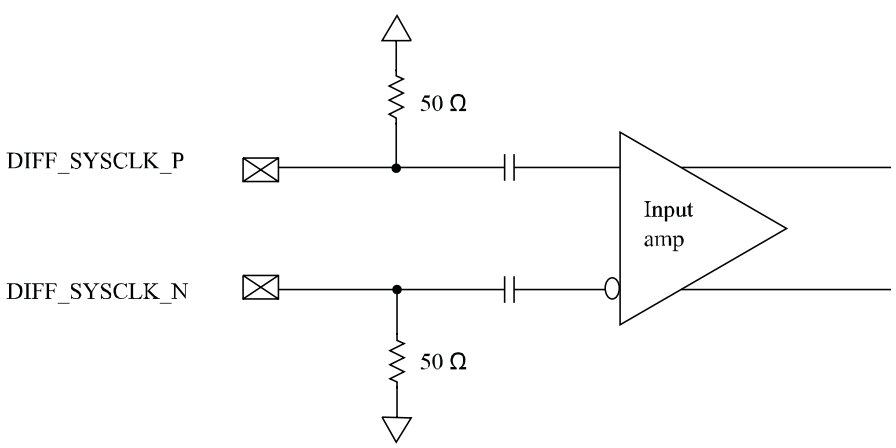
3.7.4 Differential system clock (DIFF_SYSCLK_P/DIFF_SYSCLK_N) timing specifications

The differential system clocking mode requires an on-board oscillator to provide reference clock input to the differential system clock pair (DIFF_SYSCLK_P/DIFF_SYSCLK_N).

This differential clock pair can be configured to provide the clock to core, platform, and USB PLLs.

This figure shows a receiver reference diagram of the differential system clock.

Figure 11. DIFF_SYSCLK_P/DIFF_SYSCLK_N receiver



This section provides the differential system clock DC and AC timing specifications.

3.7.4.1 Differential system clock DC electrical characteristics

For DC electrical characteristics, see DC-level requirement for SerDes reference clocks.

The differential system clock receiver's power supply voltage requirements ($SD3\_SV_{DD)}$ are specified in Recommended Operating Conditions.

3.7.4.2 Differential system clock AC timing specifications

This table provides the differential system clock AC timing specificiatons.

For additional AC timing specifications, see SerDes reference clocks AC timing specifications.

Table 15. Differential System Clock AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency	f_{SYSCLK}	-	100	-	MHz	-
Reference clock frequency- offset	F_{REF_OFFSET}	-300.0	-	300.0	ppm	-
Reference clock random jitter (RMS)	$JRMS_{REF\_CLK}$	-	-	2.6	ps	1, 2
Reference clock cycle-to- cycle jitter	DJ_{REF_CLK}	-	-	150.0	ps	3
Reference clock duty cycle	t_{KHK}/t_{SYSCLK}	40	-	60	%	-

Notes:
1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.
2. The peak-to-peak Rj specification is calculated at 14.069 times the RJ_{RMS} for 10^{-12} BER.
3. DJ across all frequencies.

3.7.5 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, see the specific interface section.

3.8 Reset initialization timing specifications

This table provides the RESET initialization timing specifications.

Table 16. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of PORESET_B after SYSCLK/DIFF_SYSCLK and all power rails are stable	1.0	-	ms	1
Required input assertion time of HRESET_B	32.0	-	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	-	10.0	SYSCLK	4
Maximum rise/fall time of PORESET_B	-	1	SYSCLK	4
Input setup time for POR configs with respect to negation of PORESET_B	4.0	-	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2.0	-	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5.0	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. The DIFF_SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequence of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.9 Battery-backed security monitor and tamper detect

This section describes the DC and AC electrical characteristics for the battery-backed security monitor interface, which includes the TA_BB_TMP_DETECT_B pin. It also describes the DC electrical characteristics for the TA_TMP_DETECT_B pin.

3.9.1 Battery-backed security monitor and tamper detect DC electrical characteristics

This table provides the DC electrical characteristics for the battery-backed security monitor interface (TA_BB_TMP_DETECT_B) operating at TA_BB_V_{DD}.

Table 17. Battery-backed security monitor interface DC electrical characteristics (TA_BB_V DD = VID)1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.75 x TA_BB_VDD			V	2, 4
Input low voltage	V_{IL}		-	0.30 x TA_BB_VDD	V	2
Input current (V_{IN} = 0V or V_{IN} = TA_BB_V_{DD})	I_{IN}	-	-	50.0	µA	3

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TA_BB_V_{IN} values found in Recommended Operating Conditions.
3. The symbol TA_BB_V_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.
4. If the signal falls below V_{IH}, it can cause a false trigger.

This table provides the DC electrical characteristics for the tamper detect security monitor (TA_TMP_DETECT_B) operating at OV_{DD}.

Table 18. Tamper detect monitor interface DC electrical characteristics (OV_{DD} = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OVDD			V	2, 4
Input low voltage	V_{IL}		-	0.3 x OVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{IN})	I_{IN}	-	-	50.0	µA	3

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.
4. If the signal falls below VIH, it can cause a false trigger.

3.9.2 Battery-backed security monitor AC timing specifications

This table provides the AC timing specifications for the battery-backed security monitor interface.

Table 19. Battery-backed security monitor interface AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
TA_BB_TMP_DETECT_B	t_{TMP}	100.0	-	ns	1

Note:
1. TA_BB_TMP_DETECT_B is asynchronous to any clock.

3.10 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required GV_{DD} (typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

Note: When operating at a DDR data rate of 2600 MT/s or higher, only one dual-ranked module per memory controller is supported.

3.10.1 DDR4 SDRAM controller DC electrical characteristics

This table provides the recommended opearting conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 20. DDR4 SDRAM interface DC electrical characteristics (GV DD = 1.2V)[1, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	VREF + 0.085	—	V	2, 3
Input low voltage	V_{IL}		VREF - 0.085	V	2, 3
I/O leakage current	I_{IN}/I_{OZ}	-50	50	µA	4, 5

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
3. Internal VREF is trained.
4. Refer to IBIS model for the complete output IV curve characteristics.
5. Output leakage is measured with all outputs diabled, 0 V ≤ V_{OUT} ≤ GV_{DD}. Applies to each pin.
6. GV_{DD} is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source. GV_{DD} min = 1.14 V, GV_{DD} max = 1.26 V, and GV_{DD} typ = 1.2 V.
7. VTT and VREFCA are applied directly to the DRAM device. Both VTT and VREFCA voltages must track $GV_{DD}/2$

3.10.2 DDR4 SDRAM controller AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 21. DDR4 SDRAM interface input AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	-	VREF - 0.085	V	Internal VREF is trained.
AC input high voltage	V_{IHAC}	VREF + 0.085	-	V	Internal VREF is trained.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

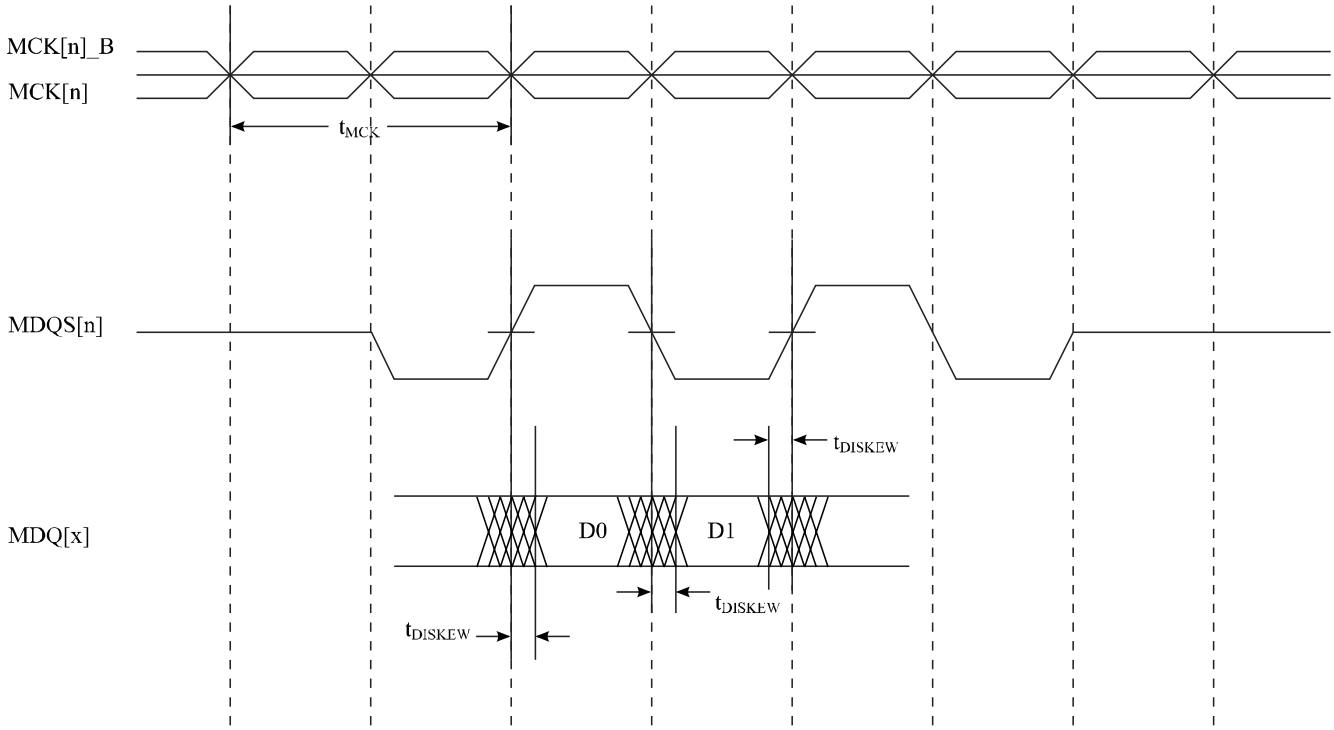
Table 22. DDR4 SDRAM interface input AC timing specifications 3

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-125.0	125.0		1
Data Rate of 1600 MT/s in DDR4		-112.0	112.0		1
Data Rate of 1800 MT/s in DDR4		-93.0	93.0		1
Data Rate of 2100 MT/s in DDR4		-82.0	82.0		1
Data Rate of 2400 MT/s in DDR4		-78.0	78.0		1
Data Rate of 2600 MT/s in DDR4		-74.0	74.0		1
Data Rate of 2900 MT/s in DDR4		-69.0	69.0		1
Data Rate of 3200 MT/s in DDR4		-65.0	65.0		1
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-250.0	250.0		2
Data Rate of 1600 MT/s in DDR4		-200.0	200.0		2
Data Rate of 1800 MT/s in DDR4		-175.0	175.0		2
Data Rate of 2100 MT/s in DDR4		-152.0	152.0		2
Data Rate of 2400 MT/s in DDR4		-130.0	130.0		2
Data Rate of 2600 MT/s in DDR4		-114.0	114.0		2
Data Rate of 2900 MT/s in DDR4		-102.0	102.0		2
Data Rate of 3200 MT/s in DDR4		-92.0	92.0		2, 3

Notes:

1. t_{CISKEW} represents the amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = +/-(T / 4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. See Figure 12

Figure 12. DDR4 SDRAM interface input timing diagram



This table contains the output AC timing targets for the DDR4 SDRAM interface

Table 23. DDR4 SDRAM interface output AC timing specifications

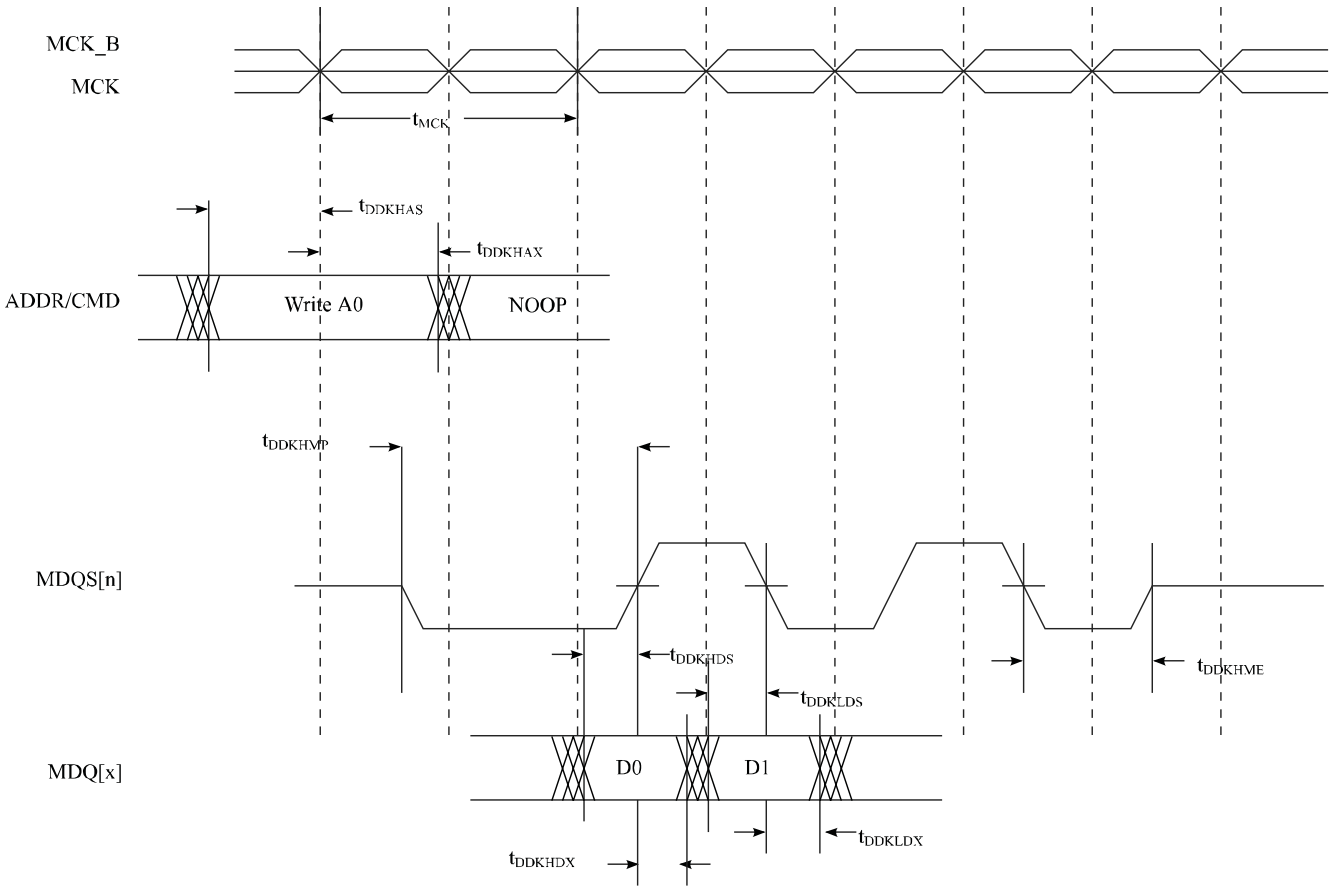
Parameter	Symbol	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	625.0	1500.0	ps	1
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		3, 4
Data Rate of 1600 MT/s in DDR4		495.0	-		3, 4
Data Rate of 1800 MT/s in DDR4		410.0	-		3, 4
Data Rate of 2100 MT/s in DDR4		350.0	-		3, 4
Data Rate of 2400 MT/s in DDR4		321.0	-		3, 4
Data Rate of 2600 MT/s in DDR4		289.0	-		3, 4
Data Rate of 2900 MT/s in DDR4		263.0	-		3, 4
Data Rate of 3200 MT/s in DDR4		210.0	-		3, 4
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		3, 4
Data Rate of 1600 MT/s in DDR4		495.0	-		3, 4
Data Rate of 1800 MT/s in DDR4		390.0	-		3, 4
Data Rate of 2100 MT/s in DDR4		350.0	-		3, 4
Data Rate of 2400 MT/s in DDR4		321.0	-		3, 4
Data Rate of 2600 MT/s in DDR4		289.0	-		3, 4
Data Rate of 2900 MT/s in DDR4		263.0	-		3, 4
Data Rate of 3200 MT/s in DDR4		210.0	-		3, 4
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		500.0	-		4, 5
Data Rate of 1600 MT/s in DDR4		400.0	-		4, 5
Data Rate of 1800 MT/s in DDR4		350.0	-		4, 5
Data Rate of 2100 MT/s in DDR4		320.0	-		4, 5
Data Rate of 2400 MT/s in DDR4		280.0	-		4, 5

Parameter	Symbol	Min	Max	Unit	Notes
Data Rate of 2600 MT/s in DDR4		250.0	-		4, 5
Data Rate of 2900 MT/s in DDR4		225.0	-		4, 5
Data Rate of 3200 MT/s in DDR4		205.0	-		4, 5
MDQS preamble	t_{DDKHMP}	0.9 * t_{MCK}	-	ps	4
MDQS postamble	t_{DDKHME}	0.4 * t_{MCK}	0.6 * t_{MCK}	ps	4

Notes:

1. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
2. See Figure 12.
3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, and MDQ/MECC/MDM/MDQS/MDQS_B.
4. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, tDDKHAS symbolizes DDR timing (DD) for the time tMCK memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.
5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
6. See Figure 13.

Figure 13. DDR4 SDRAM interface output timing diagram



3.11 Universal asynchronous receiver/transmitter (UART)

3.11.1 UART DC electrical characteristics

This table provides the DC electrical characteristics for the UART interface.

Table 24. UART DC electrical characteristics (OV DD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.45	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.11.2 UART AC timing specifications

This table provides the AC timing specifications for the UART interface.

Table 25. UART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Baud rate	baud	300.0	921600.0	bits/se c	1, 2

Notes:
1. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
2. The actual attainable baud rate is limited by the latency of interrupt processing.

3.12 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.12.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 26. eSDHC DC electrical characteristics (EVDD/OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}/OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x EV_{DD}/OV_{DD}	V	2
Input/output leakage current	I_{IN}/I_{OZ}	-	-250/+50	µA	-
Output high voltage (I_{OH} = -2mA at EV_{DD}/OV_{DD} min)	V_{OH}	EV_{DD}/OV_{DD} - 0.45	-	V	-
Output low voltage (I_{OL} = 2mA at EV_{DD}/OV_{DD} min)	V_{OL}	-	0.45	V	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN}/OV_{IN} values found in Recommended Operating Conditions.

3.12.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 27. eSDHC AC timing specifications (full-speed mode) 1, 3, 5

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO	f_{SHSCK}	0.0	25.0	MHz	1, 2, 3
SDHC_CLK frequency eMMC	f_{SHSCK}	0.0	26.0	MHz	1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	10.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	10.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of t (first two letters of functional block)(signal)(state) (reference)(state) for inputs and t (first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an MMC card.
3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.
4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.
5. See Figure 19.

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 28. eSDHC AC timing specifications (high-speed mode) [1,3,5,6,7]

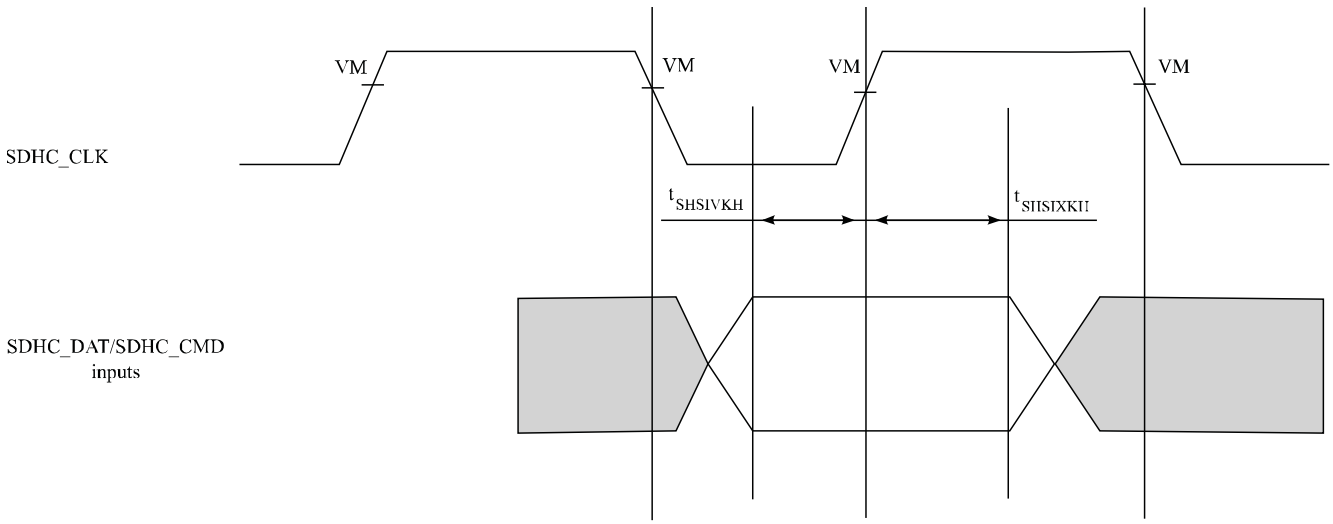
Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO	f_{SHSCK}	0.0	50.0	MHz	1, 2, 3
SDHC_CLK frequency eMMC	f_{SHSCK}	0.0	52.0	MHz	1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	7.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	7.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of t (first two letters of functional block)(signal)(state) (reference)(state) for inputs and t (first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.
3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.
4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.
5. See Figure 19.
6. See Figure 14.
7. See Figure 15

This figure provides the input AC timing diagram for high-speed mode.

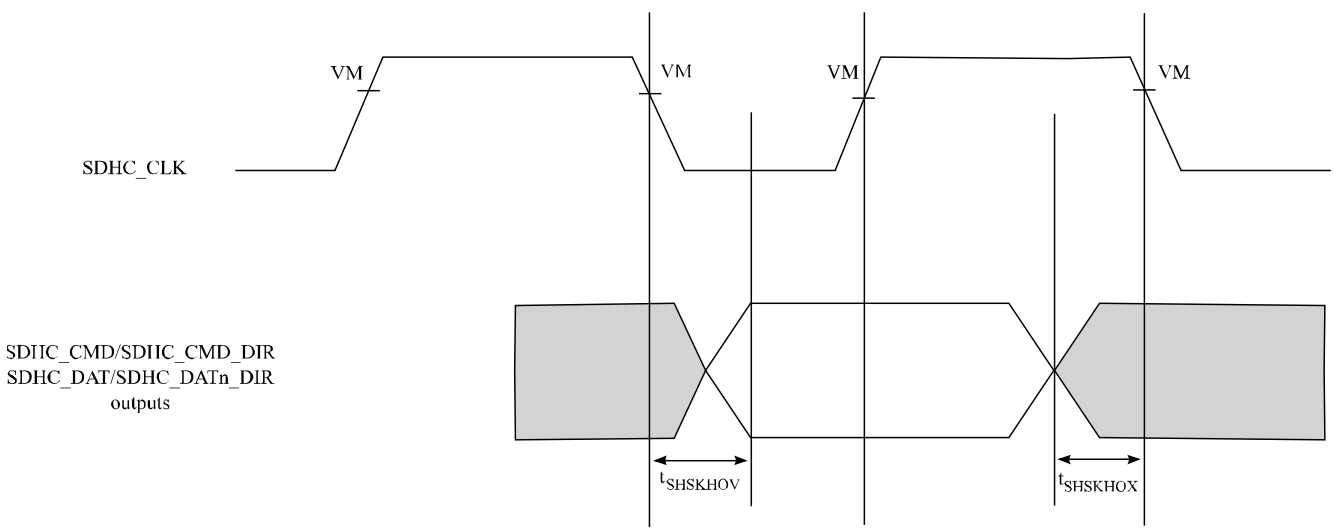
Figure 14. eSDHC high-speed mode input AC timing diagram



VM = Midpoint Voltage (Respective supply / 2)

This figure provides the output AC timing diagram for high-speed mode.

Figure 15. eSDHC high-speed mode output AC timing diagram



VM = Midpoint Voltage (Respective supply / 2)

This table provides the eSDHC AC timing specifications for SDR50 mode on devices with a voltage translator.

Table 29. eSDHC AC timing specifications (SDR50 mode with voltage translator) 2, 3, 4

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHSCK}	0.0	100.0	MHz	-
SDHC_CLK rise and fall times	t_{SHSCKR}/t_{SHSCKF}	-	2.0	ns	1
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHSIVKH}$	1.9	-	ns	1, 5, 6
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHSIXKH}$	0.7	-	ns	1, 5, 6
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	1.6	-	ns	1, 5, 6
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	5.7	ns	1, 5, 6

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and CL = $C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. See Figure 20.
4. See Figure 21.
5. Voltage translator with board skew: -0.8 ns to 0.8 ns
6. The voltage translator parameters are based on:
   . Channel-to-channel skew is min -0.5 ns, max +0.5 ns
   . CLK_Feedback to DAT/CMD delay is min -0.5 ns, max +0.5 ns

This table provides the SDHC1 and SDHC2 AC timing specifications for DDR50 and DDR (3.3V) mode with voltage translator.

Table 30. SDHC1 and SDHC2 AC timing specifications (DDR50 and DDR (3.3V) mode with voltage translator) [3, 4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO DDR50 mode		-	50.0		1
eMMC DDR mode		-	50.0		2
SDHC_CLK rise and fall times	t_{SHCKR}/t_{SHCKF}	-	-	ns	-
SD/SDIO DDR50 mode		-	4.0		1
eMMC DDR mode		-	2.0		2
Input setup times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIVKH}$	-	-	ns	-
SD/SDIO DDR50 mode		1.6	-		1, 7, 9
eMMC DDR mode		1.6	-		2, 7, 9
Input hold times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIXKH}$	0.7	-	ns	1, 7, 9
Output hold time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOX}$	-	-	ns	-
SD/SDIO DDR50 mode		2.2	-		1, 7, 9
eMMC DDR mode		3.9	-		2, 7, 9
Output delay time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOV}$	-	-	ns	-
SD/SDIO DDR50 mode		-	5.6		1, 7, 9
eMMC DDR mode		-	6.1		2, 7, 9
Input setup time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIVKH}$	-	-	ns	-
SD/SDIO DDR50 mode		4.8	-		1, 8, 9
eMMC DDR mode		4.5	-		2, 8, 9
Input hold time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIXKH}$	0.7	-	ns	1, 7, 9

Parameter	Symbol	Min	Max	Unit	Notes
Output hold time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOX}$	-	-	ns	-
SD/SDIO DDR50 mode		2.2	-		1, 7, 9
eMMC DDR mode		4.4	-		2, 7, 9
Output delay time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOV}$	-	-	ns	-
SD/SDIO DDR50 mode		-	12.6		1, 7, 9
eMMC DDR mode		-	15.3		2, 7, 9

Notes:

1. $C_{CARD} \leq 10pF$, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 20$ pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.
3. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
4. See Figure 22.
5. See Figure 23.
6. Assumes no skew between CLK to and CLK_SYNC_OUT
7. Voltage translator with board skew: -0.8 ns to 0.8 ns.
8. Voltage translator with board skew: -0.8 ns to 0.9 ns.
9. The voltage translator parameters are based on:
   Channel-to-channel skew is min -0.5 ns, max +0.5 ns.
   CLK_Feedback to DAT/CMD delay is min -0.5 ns, max +0.5 ns.

This table provides the SDHC1 and SDHC2 AC timing specifications for the DDR (1.8V) mode without voltage translator.

Table 31. SDHC1 and SDHC2 AC timing specifications (DDR (1.8V) mode without voltage translator) 1, 2, 3, 4

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
SDHC_CLK frequency	f_{SHCK}		50.0	MHz	
SDHC_CLK rise and fall times	t_{SHCKR}/t_{SHCKF}		2.0	ns	
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSKEW}				
SDHC1		-0.6	0.1	ns	
SDHC2		-0.2	0.2	ns	
Input setup times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIVKH}$	1.6		ns	5
Input hold times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIXKH}$	0.7		ns	5
Output hold time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOX}$	3.4		ns	5
Output delay time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOV}$		6.1	ns	5
Input setup time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIVKH}$	4.5		ns	5
Input hold time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIXKH}$	0.7		ns	5
Output hold time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOX}$	3.9		ns	5
Output delay time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOV}$		15.3	ns	5

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 20$ pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. See Figure 22.
4. See Figure 23.
5. Board skew: -0.2 to 0.2 ns

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 32. eSDHC AC timing specifications (SDR104/HS200 mode) [2,3]

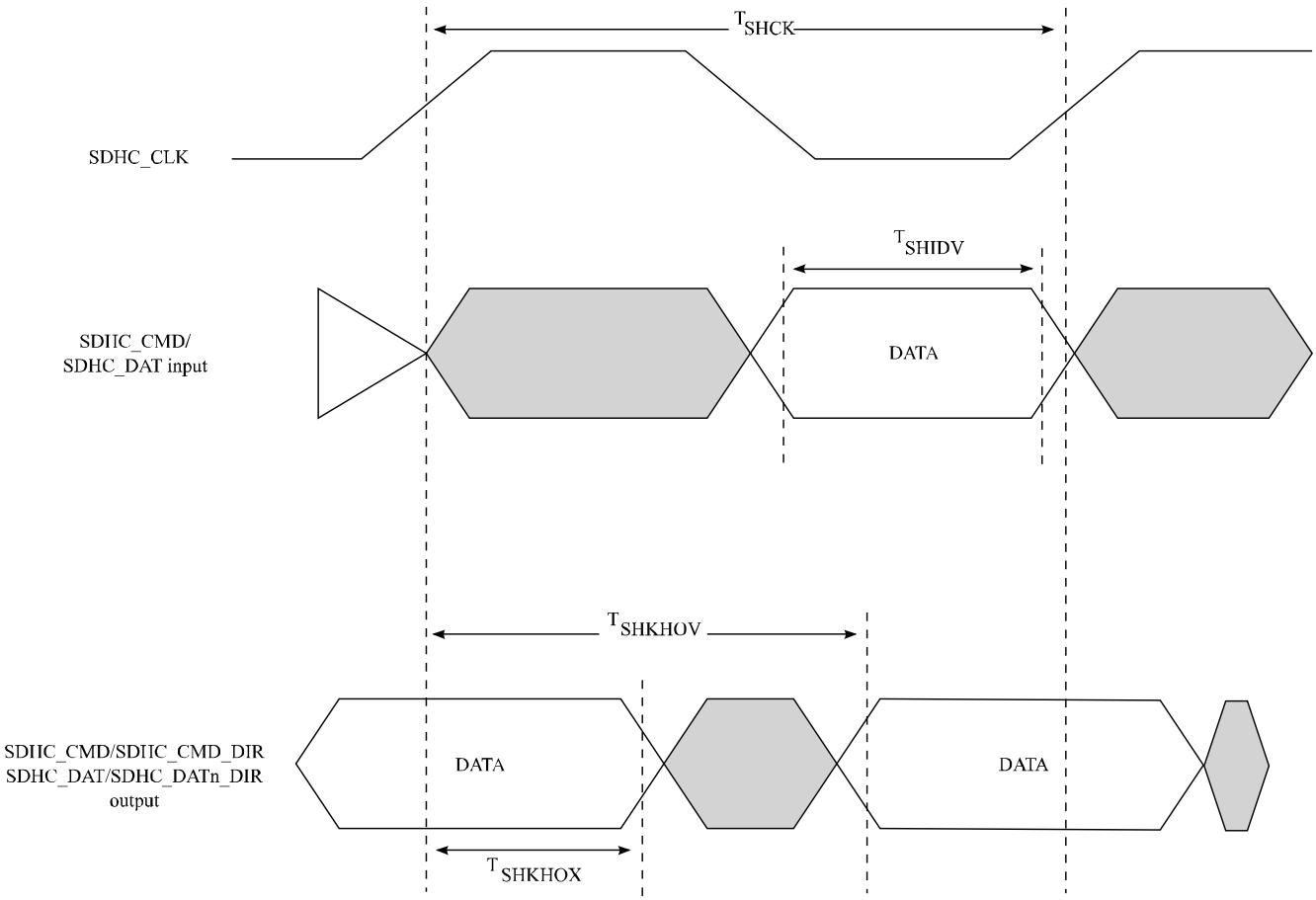
Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO SDR104 mode		-	208.0		-
eMMC HS200 mode		-	200.0		-
SDHC_CLK rise and fall times	t_{SHCKR}/t_{SHCKF}	-	1.0	ns	1
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	-	-	ns	-
SD/SDIO SDR104 mode		1.58	-		1
eMMC HS200 mode		1.6	-		1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	-	ns	-
SD/SDIO SDR104 mode		-	2.9		1
eMMC HS200 mode		-	2.95		1
Input data window (UI)	t_{SHIDV}	-	-	Unit interval	-
SD/SDIO SDR104 mode		0.5	-		1
eMMC HS200 mode		0.475	-		1

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. See Figure 16.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

Figure 16. eSDHC SDR104/HS200 mode timing diagram



This table provides the eSDHC AC timing specifications for eMMC HS400 mode.

Table 33. eSDHC AC timing specifications (HS400 mode) [2, 3, 4, 5]

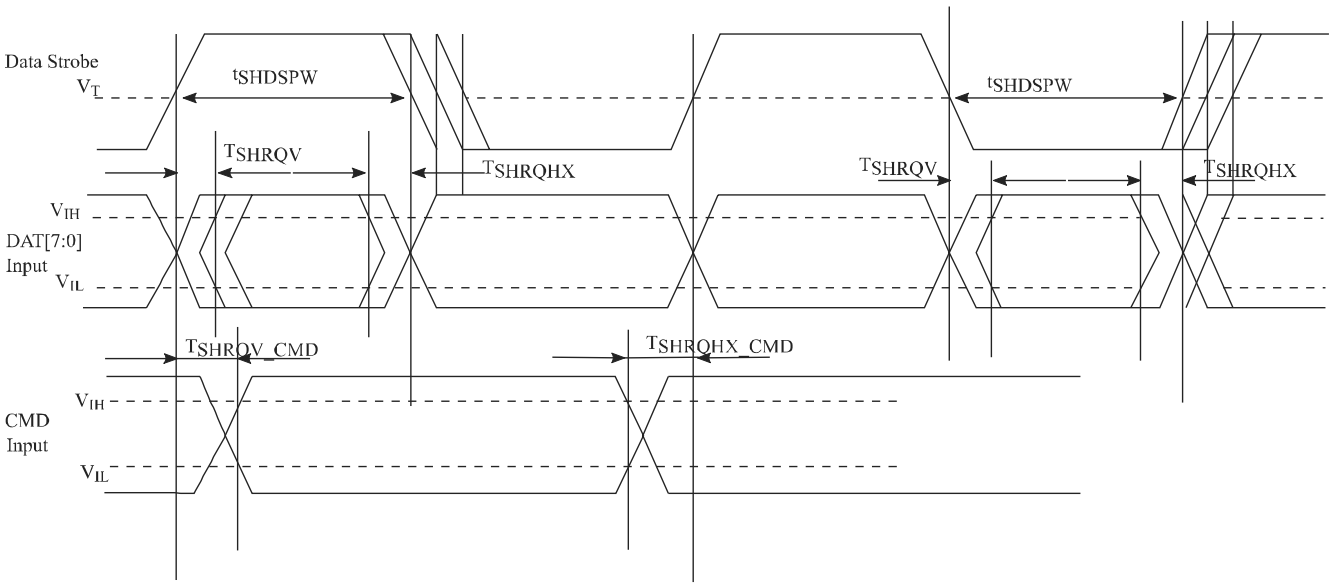
Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	200.0	MHz	-
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	0.75	-	ns	1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	1.75	ns	1
Data valid skew to DQS	T_{SHRQV}	-	0.45	ns	1
Data hold skew to DQS	T_{SHRQHX}	-	0.45	ns	1
Command valid skew to DQS	T_{SHRQV_CMD}	-	0.45	ns	1
Command hold skew to DQS	$T_{SHRQHX\_CM\ D}$	-	0.45	ns	1
DQS pulse width	$T_{SHDSPWS}$	1.97	-	ns	1
Duty cycle distortion	t_{SHSCK_DIS}	0.0	0.3	ns	1

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. For HS400 without enhanced strobe (DQS) command, see Figure 16.
4. See Figure 17.
5. See Figure 18.

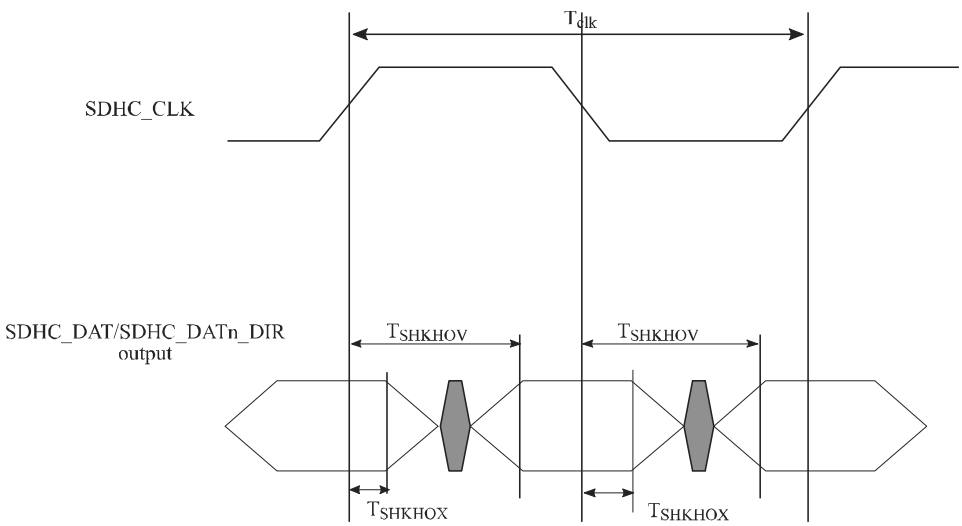
This figure provides the eSDHC HS400 mode input timing diagram.

Figure 17. eSDHC HS400 mode input timing diagram



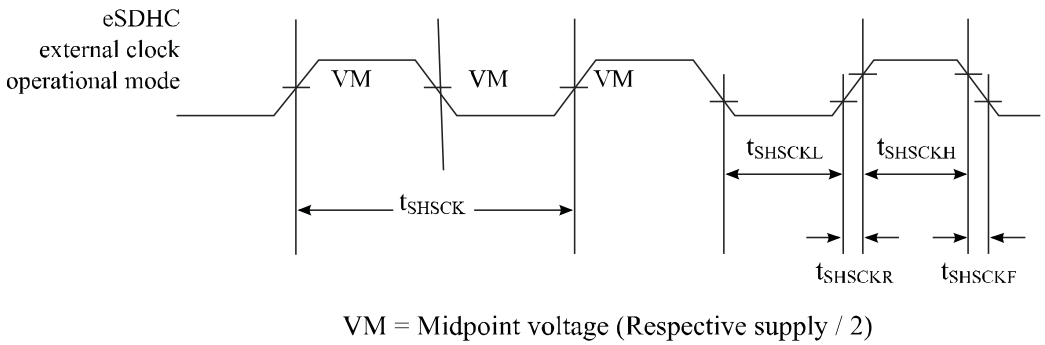
This figure provides the eSDHC HS400 mode output timing diagram.

Figure 18. eSDHC HS400 mode output timing diagram



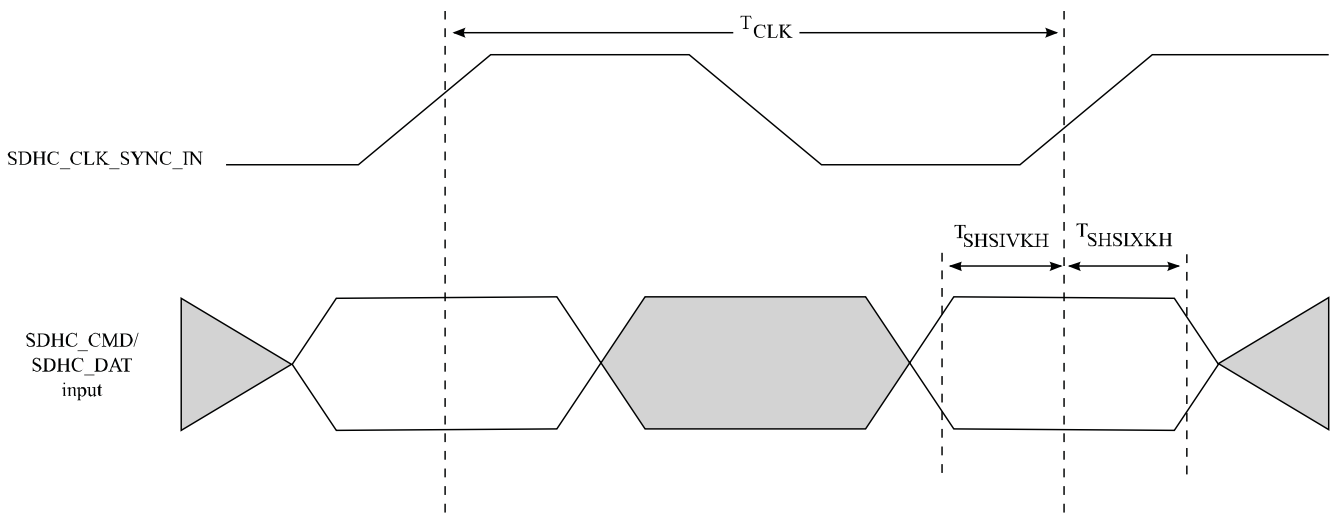
This figure provides the eSDHC clock input timing diagram.

Figure 19. eSDHC clock input timing diagram



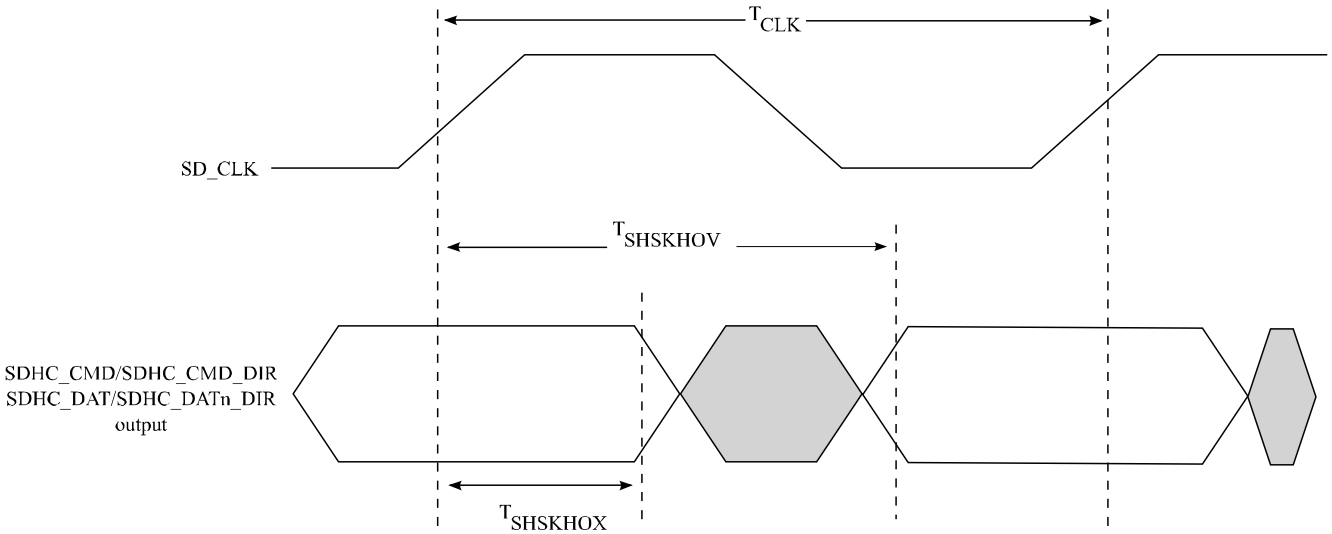
This figure provides the eSDHC input AC timing diagram for SDR50 mode.

Figure 20. eSDHC SDR50 mode input AC timing diagram



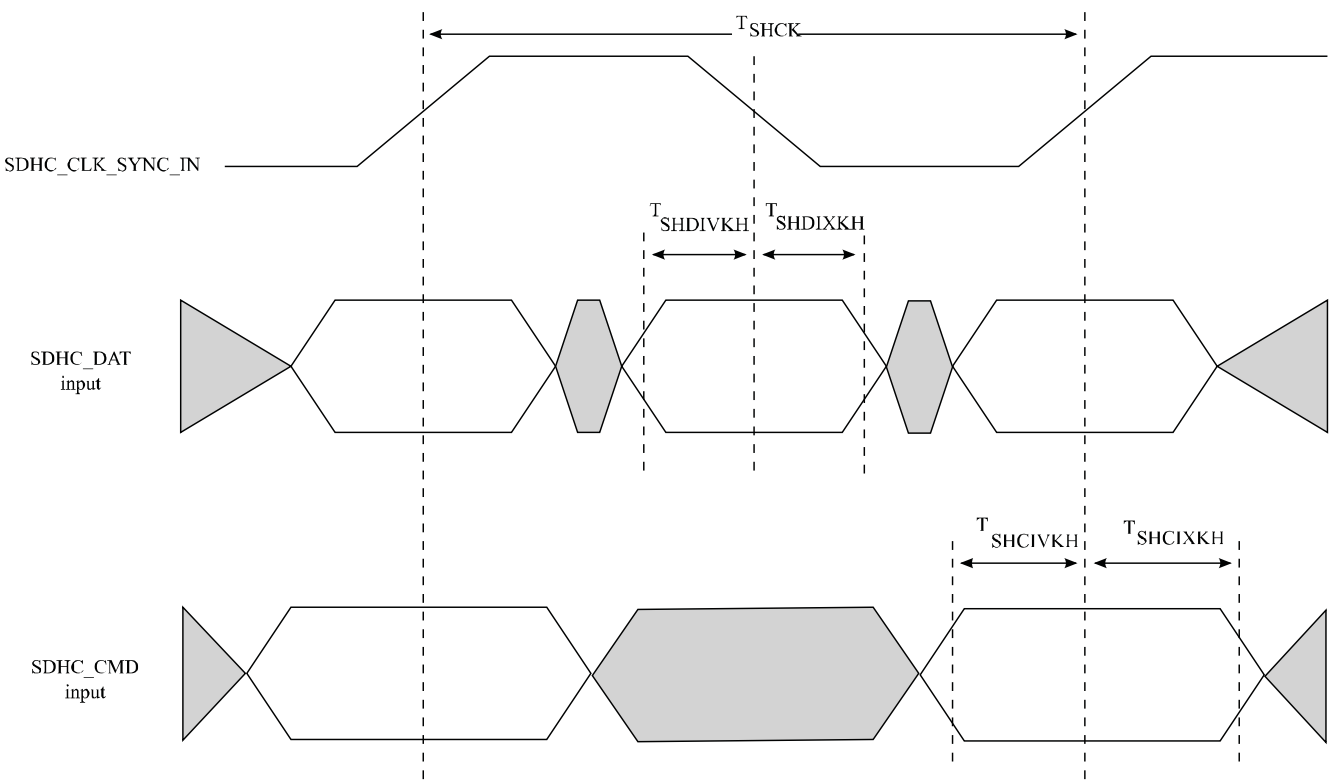
This figure provides the eSDHC output timing diagram for SDR50 mode

Figure 21. eSDHC SDR50 mode output timing diagram



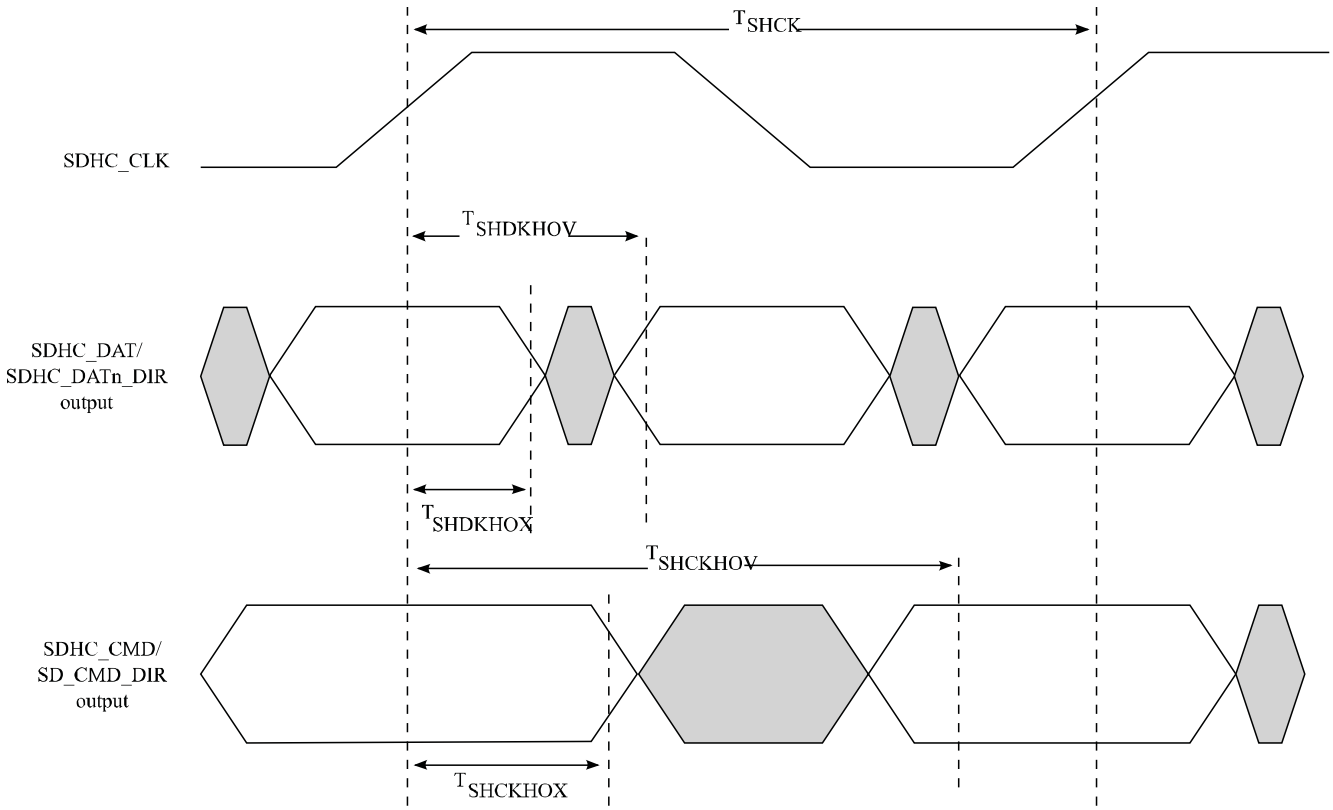
This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

Figure 22. eSDHC DDR50/DDR mode input AC timing diagram



This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

Figure 23. eSDHC DDR50/DDR mode output AC timing diagram



3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the EMI, RGMII, and IEEE Std 1588 interfaces

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI) interface.

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

3.13.1.1 EMI DC electrical characteristics

This table provides the EMI DC electrical characteristics.

Table 34. EMI DC electrical characteristics (OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.13.1.2 EMI AC timing specifications

This table provides the EMI AC timing specifications.

Table 35. EMI AC timing specifications [4, 5, 6]

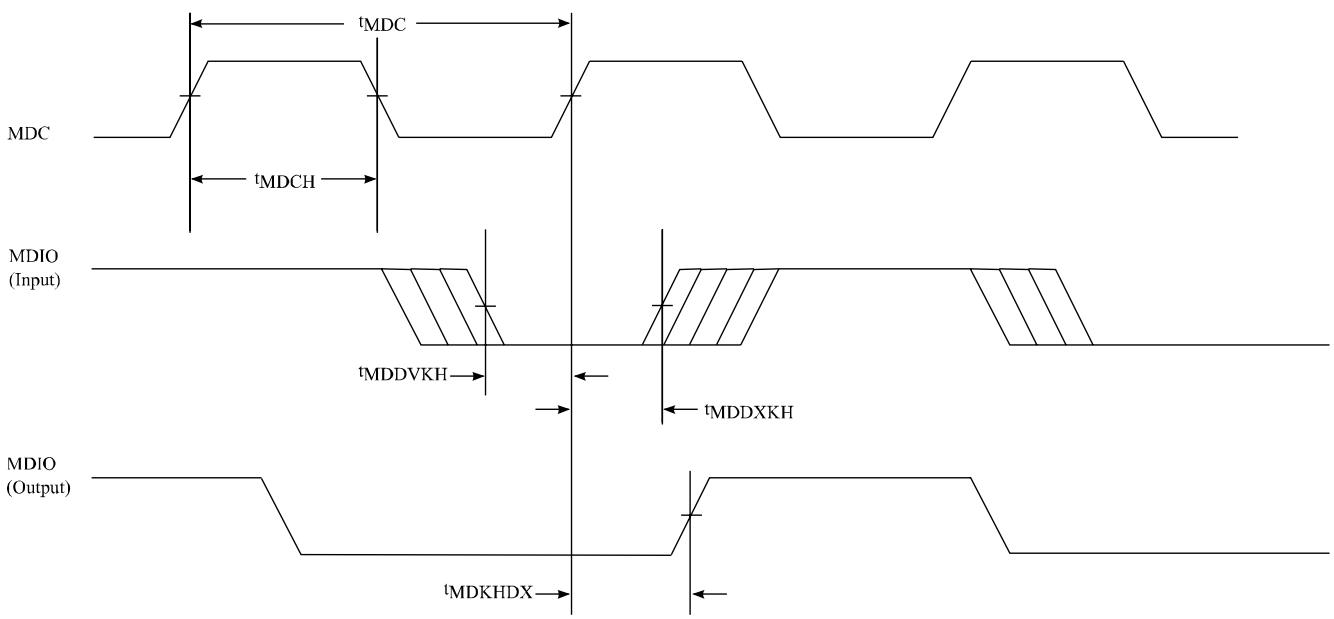
Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	5.0	MHz	1
MDC clock pulse width high	t_{MDCH}	80.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	Y x t_{enet_clk} - 3	Y x t_{enet_clk} + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	0.0	-	ns	-

Notes:

1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.
2. t_{enet_clk} is the Ethernet clock period x 2.
3. MDIO timing is configurable by programming the EMDIO_CFG register fields. The default value of Y = 5. Y is the value determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD], and MDIO[EHOLD]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time requirement of Ethernet PHY.
4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time tMDC from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the tMDC clock reference (K) going to the high (H) state or setup time.
5. Assumes a maximum load of 338 pF.
6. See Figure 24.

This figure shows the Ethernet management interface timing diagram.

Figure 24. Ethernet management interface timing diagram



3.13.2 Reduced media-independent interface (RGMII)

3.13.2.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface.

Table 36. RGMII DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN}=0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	µA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

3.13.2.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 37. RGMII AC timing specifications [7,8]

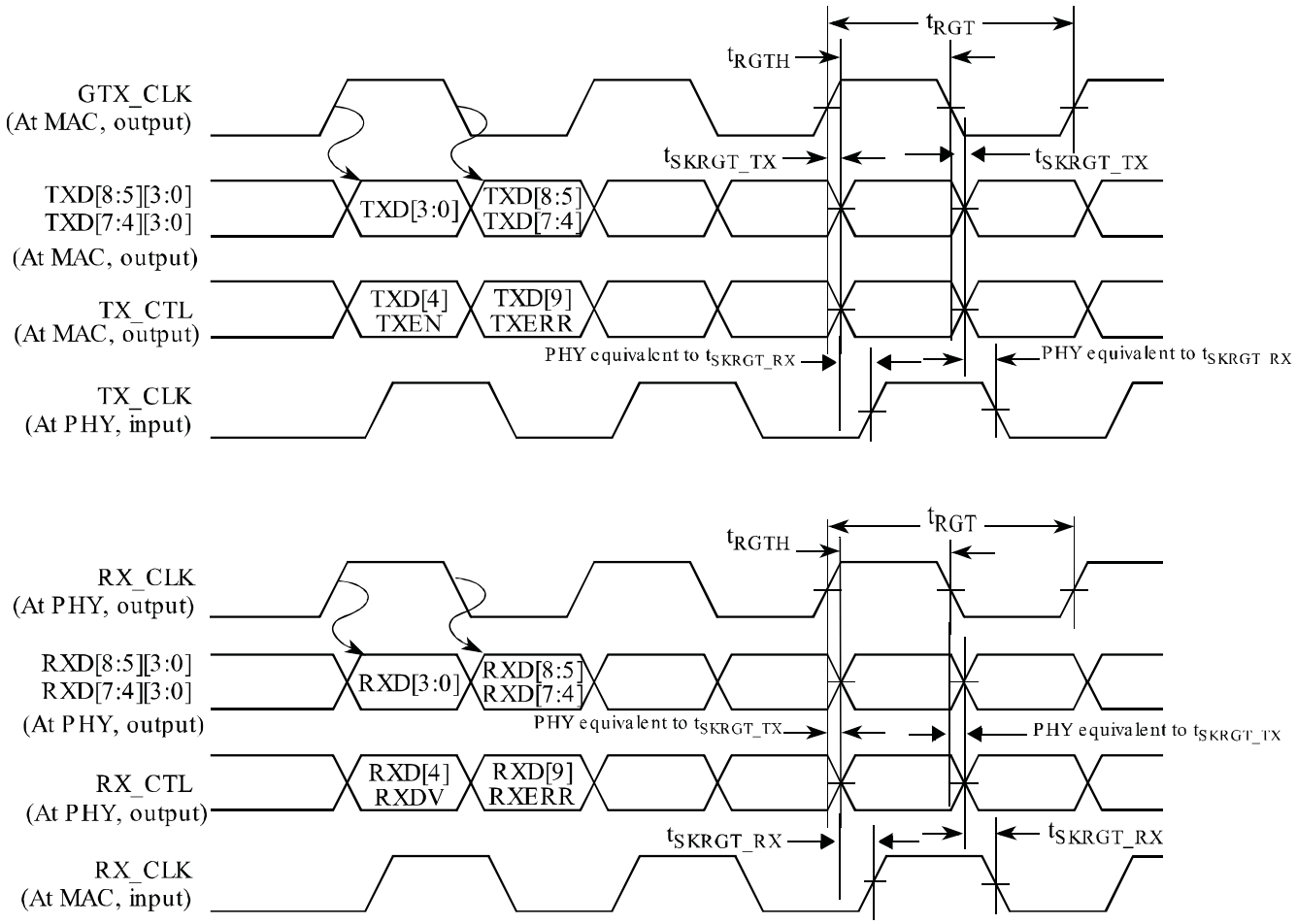
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500.0	0.0	500.0	ps	1
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{GTH}/t_{RGT}	40.0	50.0	60.0	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45.0	50.0	55.0	%	-
Rise time (20%-80%) OV_{DD} = 1.8V	t_{RGTR}	-	-	0.75	ns	5, 6
Fall time (20%-80%) OV_{DD} = 1.8V	t_{RGTF}	-	-	0.75	ns	5, 6

Notes:

1. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.
5. Applies to inputs and outputs.
6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
8. See Figure 25.

NOTE: NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC. This figure shows the RGMII AC timing and multiplexing diagrams

Figure 25. RGMII AC timing and multiplexing diagrams



3.13.3 IEEE 1588

3.13.3.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics.

Table 38. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OVIN represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.13.3.2 IEEE 1588 AC timing specifications

This table provides the AC timing specifications for the IEEE 1588 interface.

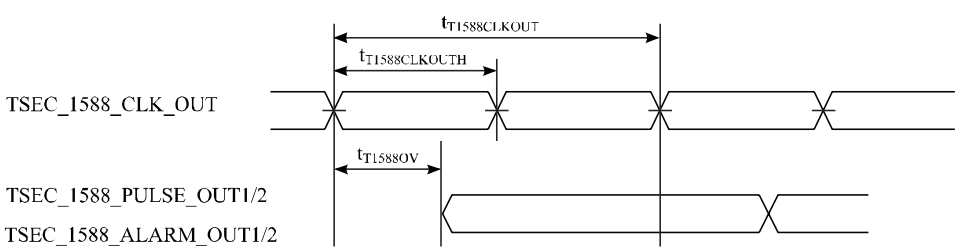
Table 39. IEEE 1588 AC timing specifications 2, 3

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{1588CLK}$	6.0	-		ns	-
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40.0	50.0	60.0	%	-
TSEC_1588_CLK_IN peak-to- peak jitter	$t_{T1588CLKI\ NJ}$	-	-	250.0	ps	-
Rise time TSEC_1588_CLK_IN (20% to 80%)	$t_{T1588CLKI\ NR}$	1.0	-	2.0	ns	-
Fall time TSEC_1588_CLK_IN (80% to 20%)	$t_{T1588CLKI\ NF}$	1.0	-	2.0	ns	-
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKO\ UT}$	2 x $t_{1588CLK}$	-	-	ns	-
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKO\ UT}$	30.0	50.0	70.0	%	-
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	-	4.0	ns	-
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIG\ H}$	2 x $t_{1588CLK}$	-	-	ns	1

Notes:
1. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. See Figure 26.
3. See Figure 27.

This figure shows the data and command output AC timing diagram.

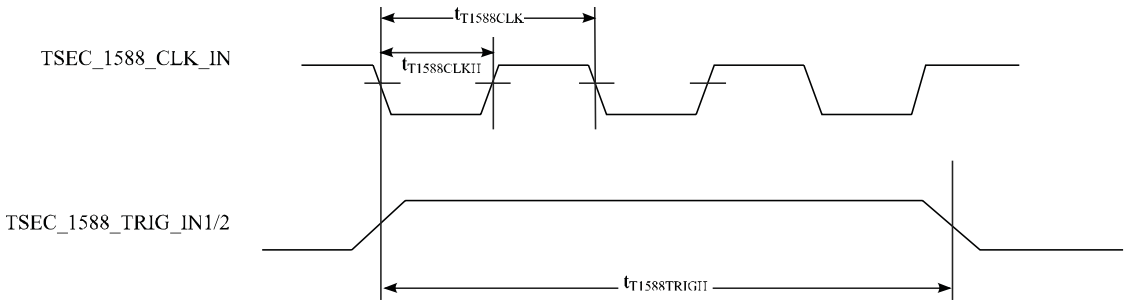
Figure 26. IEEE 1588 output AC timing



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

This figure shows the data and command input AC timing diagram.

Figure 27. IEEE 1588 input AC timing



3.14 General purpose input/output (GPIO)

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 40. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	µA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.14.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

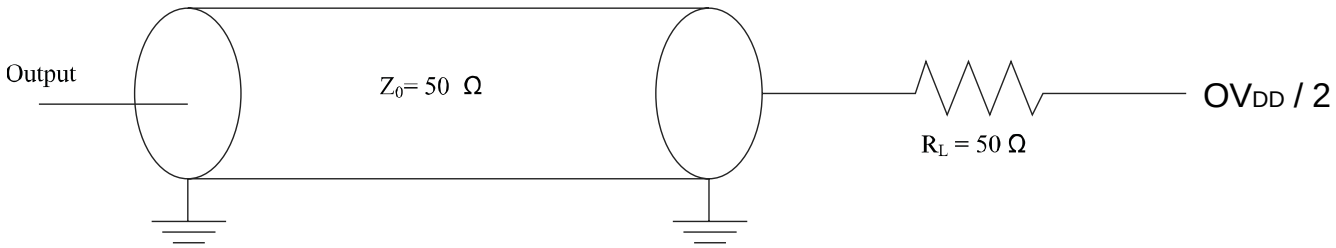
Table 41. GPIO AC timing specifications 2

Parameter	Symbol	Min	Max	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	1

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
2. See Figure 28.

The figure below provides the AC test load for the GPIO.

Figure 28. GPIO AC test load



3.15 Flextimer interface

3.15.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for the Flextimer interface.

Table 42. Flextimer DC electrical characteristics (OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.15.2 Flextimer AC timing specifications

This table provides the Flextimer input and output AC timing specifications.

Table 43. Flextimer AC timing specifications[2]

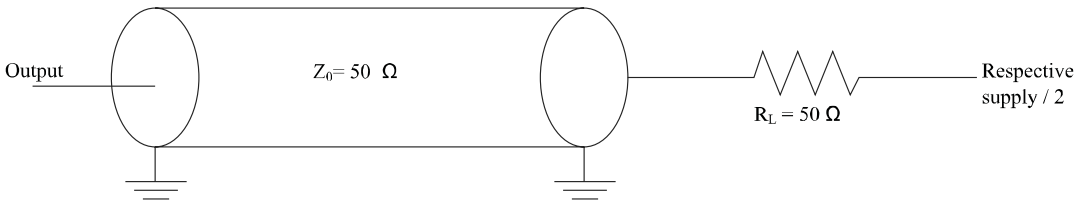
Parameter	Symbol	Min	Max	Unit	Notes
Flextimer inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	1

Notes:

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs must be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
2. See Figure 29.

The figure below provides the AC test load for the Flextimer.

Figure 29. Flextimer AC test load



3.16 Generic interrupt controller (GIC)

3.16.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for the GIC interface.

Table 44. GIC DC electrical characteristics (OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.16.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications.

Table 45. GIC AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3.0	-	SYSCLKs	1

Note:

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

3.17 I2C

3.17.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I2C interface.

Table 46. I^2C DC electrical characteristics (OV_{DD} = 1.8V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Output low voltage (OV_{DD} = min, IOL = 2 mA, OV_{DD} ≤ 2V)	V_{OL}	0.0	0.36	V	-
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	3
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} (min) and 0.9 x OV_{DD} (max))	I_I	-	±50	µA	4
Capacitance for each I/O pin	C_I	-	10.0	pF	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if the supply is switched off.

3.17.2 I2C AC timing specifications

This table provides the AC timing specifications for the I2C interface

Table 47. I^2C AC timing specifications [5,6,7]

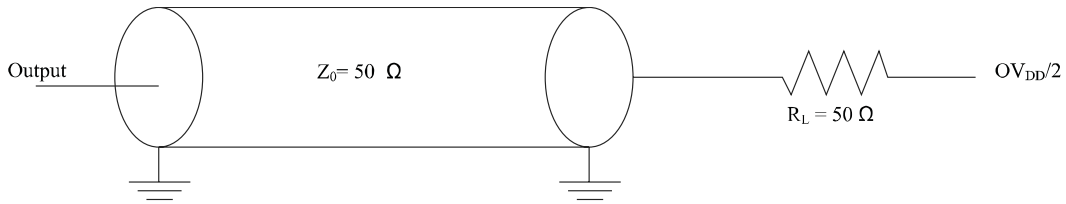
Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Max. Frequency	f_{I2C}		100	-	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	4.7		1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	4		0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	4.7		0.6	-	µs	-
Hold time (repeated) START condition	t_{I2SXKL}	4		0.6	-	µs	-
Setup time	t_{I2DVKH}	250		100.0	-	ns	1
Input hold time	t_{I2DXKL}	0.0		0.0	-	µs	2
Master output delay time	t_{I2OVKL}		3.45		0.9	µs	3
Input setup time for STOP condition	t_{I2PVKH}	4	-	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	4.7		1.3	-	µs	-
Capacitive load for each bus line	Cb		400.0	-	400.0	pF	4

Notes:

1. A Fast-mode I^2C-bus device can be used in a Standard-modeI^2C-bus system, but the requirement of Setup time of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line max rise time + data Setup Time = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released.
2. A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.
3. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Cb = Total capacitance of one bus line in pF
5. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high
6. (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition
7. (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
8. See Figure 30.
9. See Figure 31.

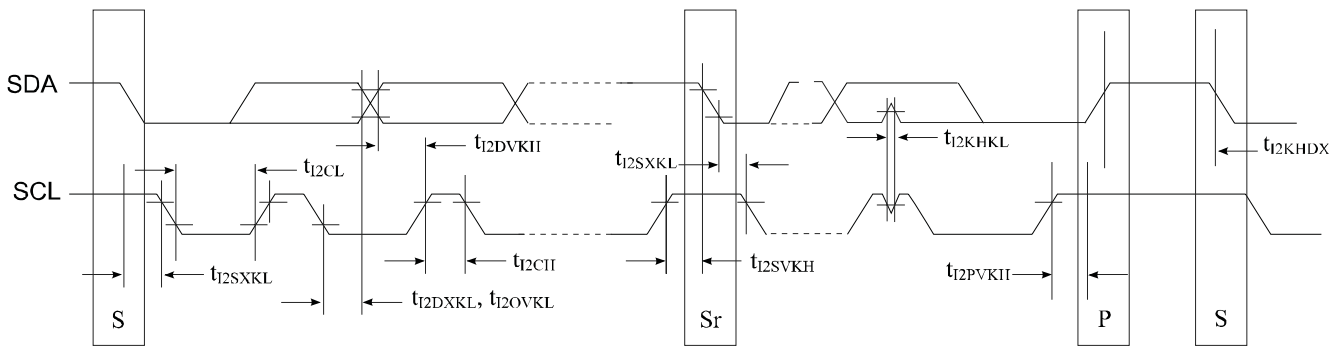
This figure shows the AC test load for the I2C.

Figure 30. I2C AC test load



This figure shows the AC timing diagram for the I^2C bus.

Figure 31. I2C bus AC timing diagram



3.18 JTAG

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.18.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG (IEEE 1149.1) interface.

Table 48. JTAG DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	-	V	2
Input low voltage	V_{IL}	-	0.6	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	µA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.18.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 32, Figure 33, Figure 34, and Figure 35.

Table 49. JTAG AC timing specifications [3, 4, 5, 6, 7]

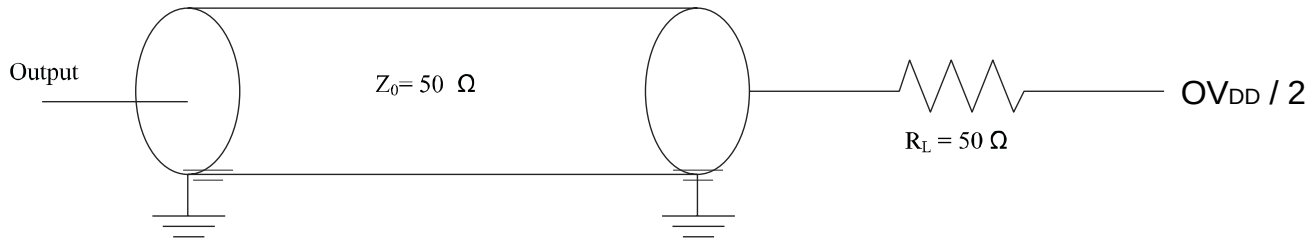
Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0	25	MHz	-
JTAG external clock cycle time	t_{JTG}	40	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	20	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	1
Input setup times	t_{JTDVKH}	6	-	ns	-
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	20.0	ns	2
Output valid times: TDO	t_{JTKLDV}	-	14	ns	2
Output hold times	t_{JTKLDX}	0.0	-	ns	2

Notes:

1. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
2. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
3. The symbols used for timing specifications follow these patterns: t(first two letters of functional block)(signal)(state)(reference) (state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, tJTDXKH symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
4. See Figure 32.
5. See Figure 33.
6. See Figure 34.
7. See Figure 35.

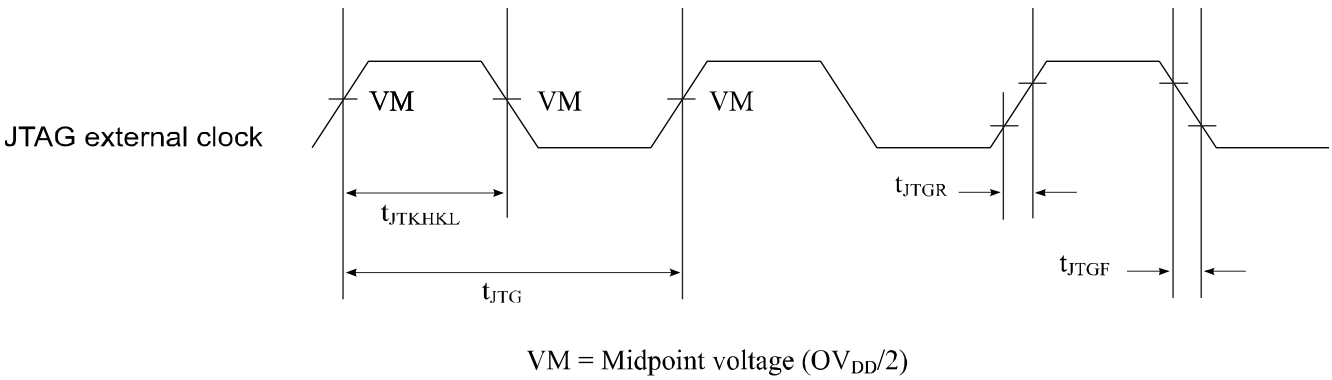
This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

Figure 32. AC test load for the JTAG interface



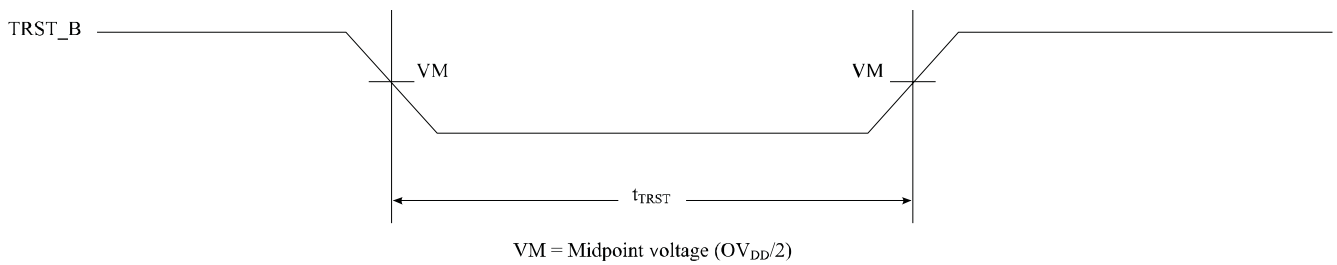
This figure shows the JTAG clock input timing diagram.

Figure 33. JTAG clock input timing diagram



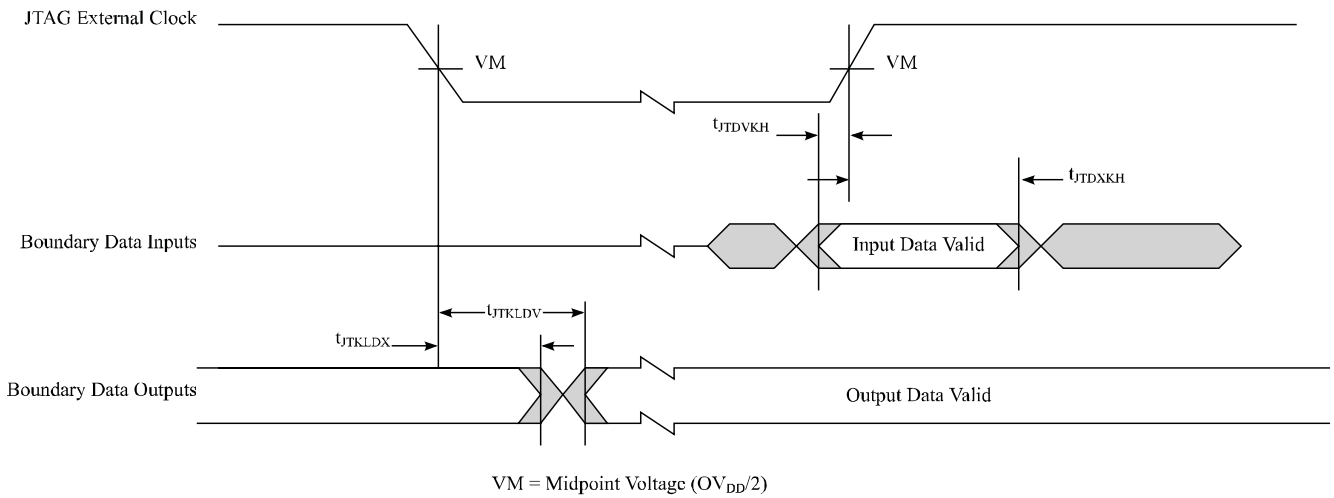
This figure shows the TRST_B timing diagram.

Figure 34. TRST_B timing diagram



This figure shows the boundary-scan timing diagram.

Figure 35. Boundary-scan timing diagram



3.19 Flex serial peripheral interface (FlexSPI)

3.19.1 FlexSPI DC electrical characteristics

This table provides the DC electrical characteristics for the FlexSPI interface.

Table 50. FlexSPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (0V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.19.2 FlexSPI AC timing specifications

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0

Table 51. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	55	%	-
CS output hold time	$t_{FSKHOX2}$	FLSHxyCR1[TCSH] * T - 0.15	-	ns	1, 5
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCS S]+ 0.5) * T) - 5.15	-	ns	1, 5
Setup time for incoming data-without DQS	t_{FSIVKH}	2.4	-	ns	5
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

Notes:

1. Refer the FLSHxyCR1 QorIQ LX2160ARM for more details, where x: A or B, y: 1 or 2
2. See Figure 37.
3. See Figure 38.
4. See Figure 39.
5. T = FlexSPI clock period

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2

Table 52. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	55	%	-
CS output hold time	$t_{FSKHOX2}$	FLSHxyCR1[TCSH] * T - 0.15	-	ns	1, 5
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCS S] + 0.5) * T) - 5.15	-	ns	1, 5
Setup time for incoming data- without DQS	t_{FSIVKH}	2.4	-	ns	-
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

Notes:
1. Refer the FLSHxyCR1 QorIQ LX2160ARM for more details, where x: A or B, y: 1 or 2
2. See Figure 37.
3. See Figure 38.
4. See Figure 39.
5. T = FlexSPI clock period

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2.

Table 53. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1, or 0x2 4, 5, 6

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	75	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	47	53	%	-
CS output hold time	$t_{FSKHOX2}$	((FLSHxyCR1[TCS H] + 0.5) * T/2) - 0.15	-	ns	1, 7
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCS S] + 0.5) * T/2) - 5.15	-	ns	1, 7
Data Valid Window	t_{FSIDVW}	0.3	-	UI	2, 3
Output data delay	t_{FSKHOV}/ t_{FSKLOV}	-	3.94	ns	-
Output data hold	t_{FSKHOX}/ t_{FSKLOX}	2.8 for Rev 1.0 3.0 for Rev 2.0	-	ns	-

Notes:
1. Refer the FLSHxyCR1 QorIQ LX2160ARM for more details, where x: A or B, y: 1 or 2
2. For DDR, Unit Internval (UI) is half of period. For example, 5 ns for 100 MHz
3. See "Data Learning Feature" section in QorIQ LXxxxxARM for details
4. See Figure 37.
5. See Figure 38.
6. See Figure 40.
7. T = FlexSPI clock period

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3.

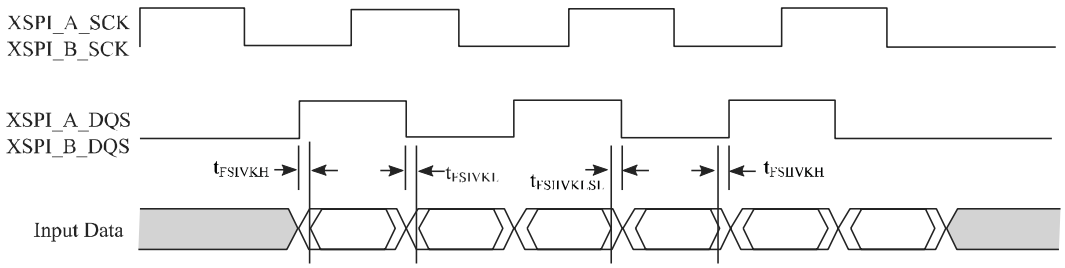
Table 54. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3 [2, 3, 4, 5]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock frequency	F_{SCK}	-	-	200.0	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	-	55	%	-
CS output hold time	$t_{FSKHOX2}$	((FLSHxyCR1[T CSH] + 0.5) * T/2) - 0.15	-	-	ns	1, 6
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[T CSH] + 0.5) * T/2) - 5.15	-	-	ns	1, 6
DQS to data skew	t_{FSIVKH}/t_{FSIVKL}	-		0.6	ns	7
DQS to data hold skew	$t_{FSIIVKH}/t_{FSIIVKL}$	-		0.9	ns	7
Output data delay	t_{FSKHOV}/t_{FSKLOV}	-	-	1.7	ns	-
Output data hold	t_{FSKHOX}/t_{FSKLOX}	0.8	-	-	ns	-

Notes:
1. Refer the FLSHxyCR1 QorIQ LX2160ARM for more details, where x: A or B, y: 1 or 2
2. See Figure 37.
3. See Figure 38.
4. See Figure 40.
5. See Figure 36.
6. T = FlexSPI clock period
7. When DLLxCR = 0x0000_1100, where x: A or B.

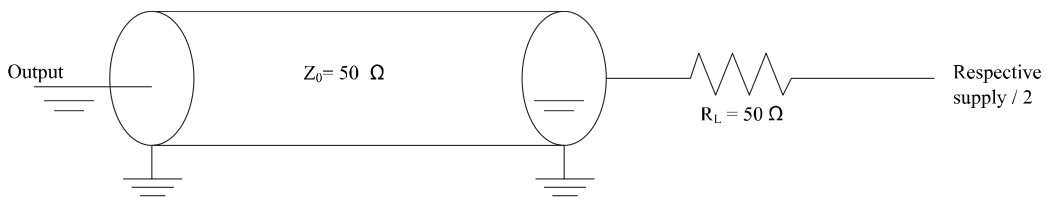
This figure shows the FlexSPI data input timing in DDR mode with an external DQS.

Figure 36. FlexSPI input AC timing-DDR mode with an external DQS



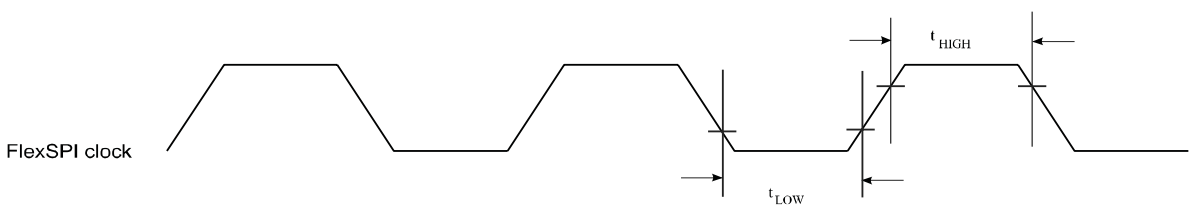
This figure shows the AC test load for the FlexSPI interface.

Figure 37. AC test load for FlexSPI



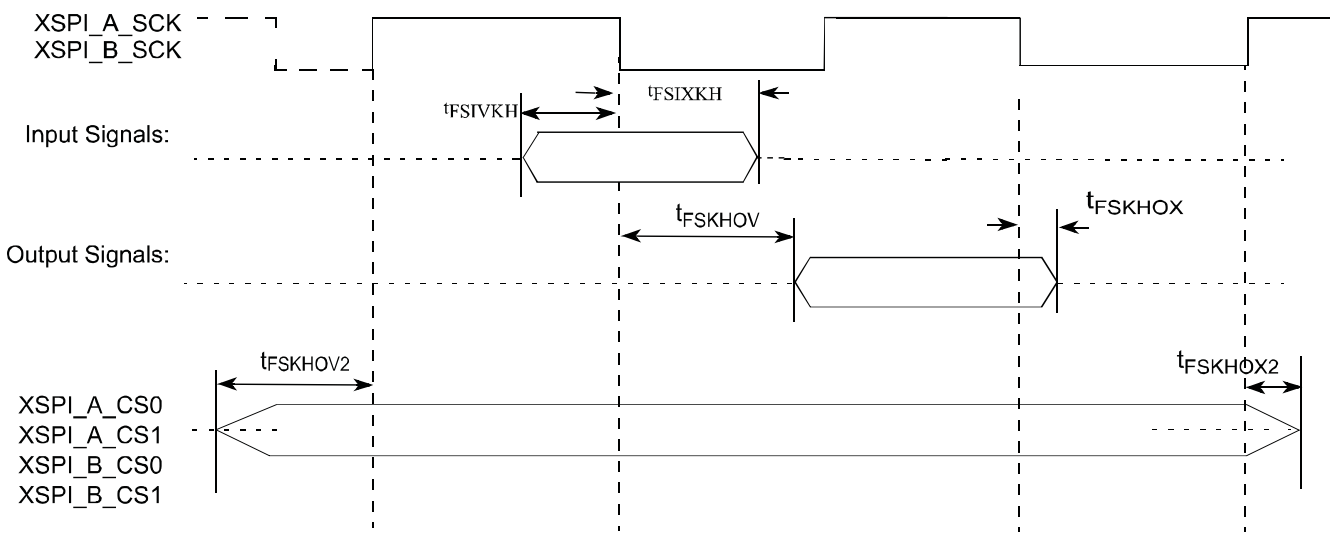
This figure shows the FlexSPI clock input timing diagram.

Figure 38. FlexSPI clock input timing diagram



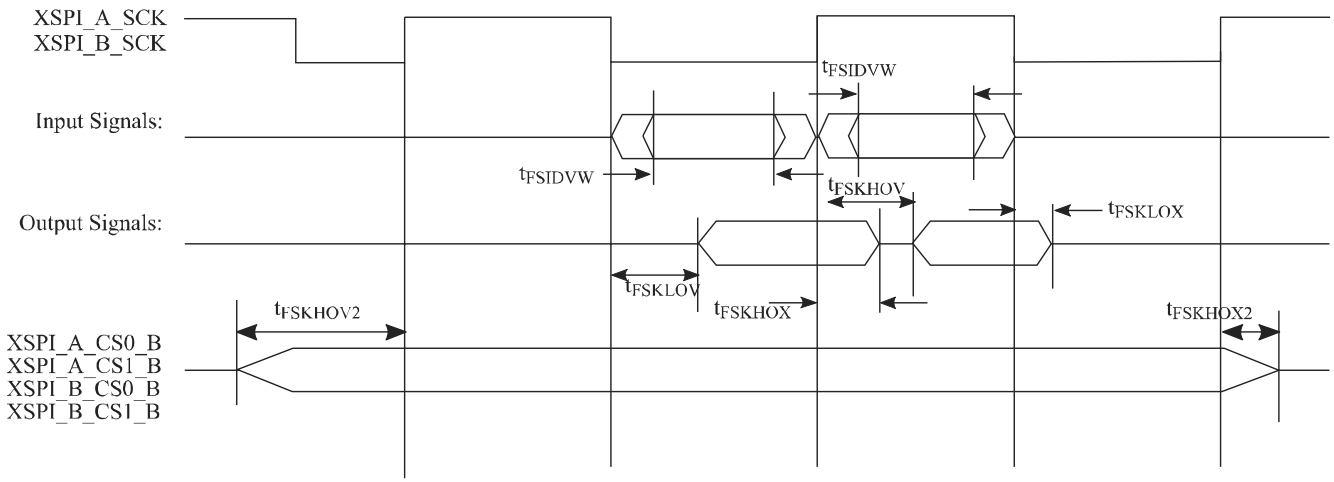
This figure shows the FlexSPI AC timing diagram for SDR mode.

Figure 39. FlexSPI SDR mode AC timing diagram



This figure shows the FlexSPI AC timing diagram for DDR mode 1 and 2.

Figure 40. FlexSPI DDR mode 1 and 2 AC timing diagram



3.20 Serial peripheral interface (SPI)

3.20.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface when operating with a single master device.

Table 55. SPI DC electrical characteristics (OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.20.2 SPI AC timing specifications

This table provides the SPI timing specifications when operating with a single master device.

Table 56. SPI AC timing specifications [6,7]

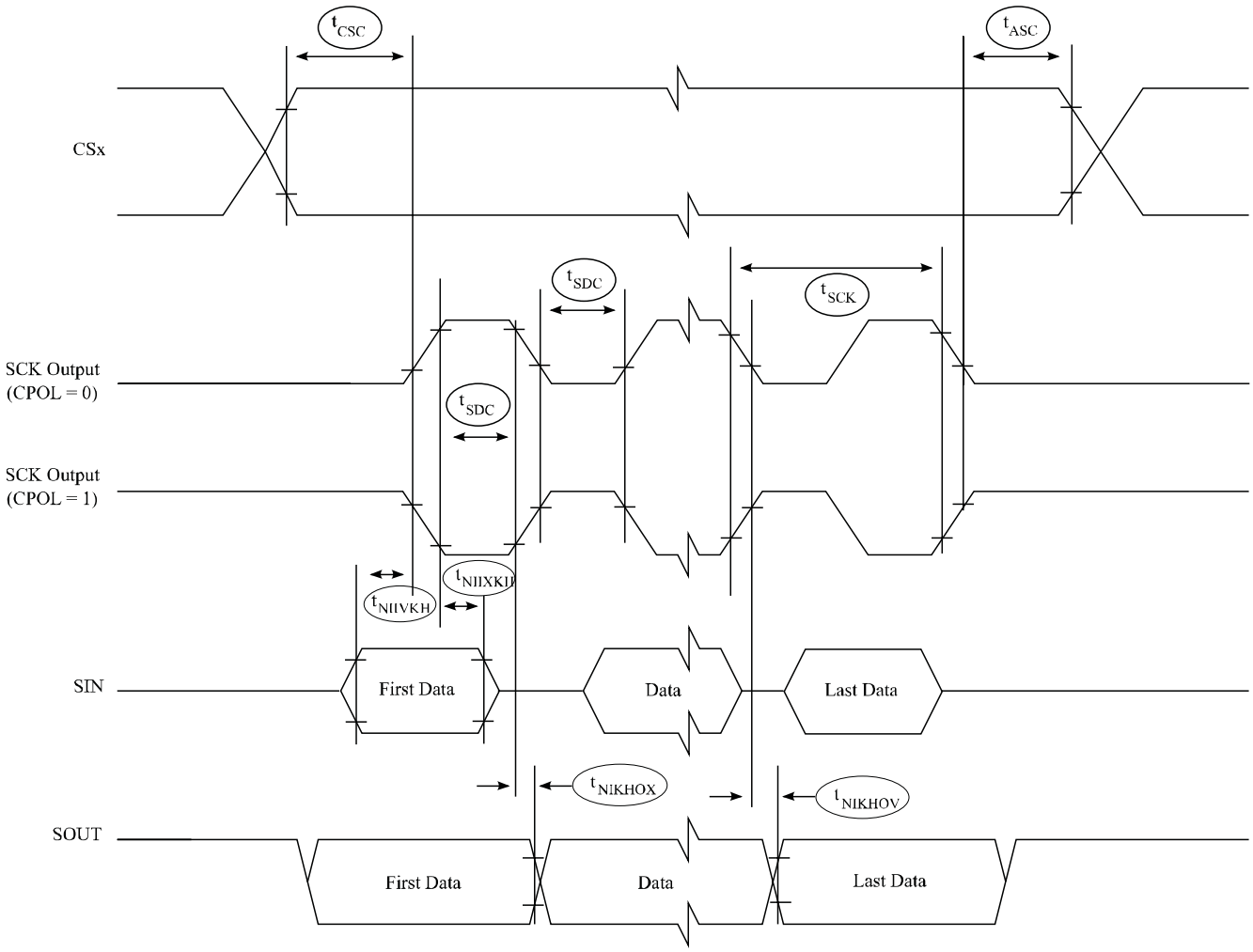
Parameter	Symbol	Min	Max	Unit	Notes
SCK cycle time	t_{SCK}	t_{SYS} * 2	-	ns	1
SCK clock pulse width	t_{SDC}	40.0	60.0	%	-
CS to SCK delay	t_{CSC}	tp*2 - 1.85	-	ns	2, 3, 4
After SCK delay	t_{ASC}	tp*2 + 0.06	-	ns	2, 5, 4
Data setup time for inputs	t_{NIIVKH}	9.0	-	ns	2
Data hold time for inputs	t_{NIIXKH}	0.0	-	ns	2
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	5.0	ns	2
Data hold time for outputs	t_{NIKHOX}	0.0	-	ns	2

Notes:

1. t_{SYS} = 10 ns
2. Master mode
3. Refer the CTARx register in QorIQ LX2160ARM for more details. The tCSC = tp * (Delay Scaler Value) * CTARx[PCSSCK] - 1.85, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tCSC = tp * 4 * 3 - 1.85 when CTARx[PCSSCK] = 0b01, CTARx[CSSCK]=0b0001
4. tp is the input clock period for the SPI controller.
5. Refer the CTARx register in QorIQ LX2160ARM for more details. The tASC = tp * (Delay Scaler Value) * CTARx[PASC] + 0.06, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tASC = tp * 8 * 3 + 0.06 when CTARx[PASC] = 0b01, CTARx[ASC]=0b0010
6. See Figure 41.
7. See Figure 42.

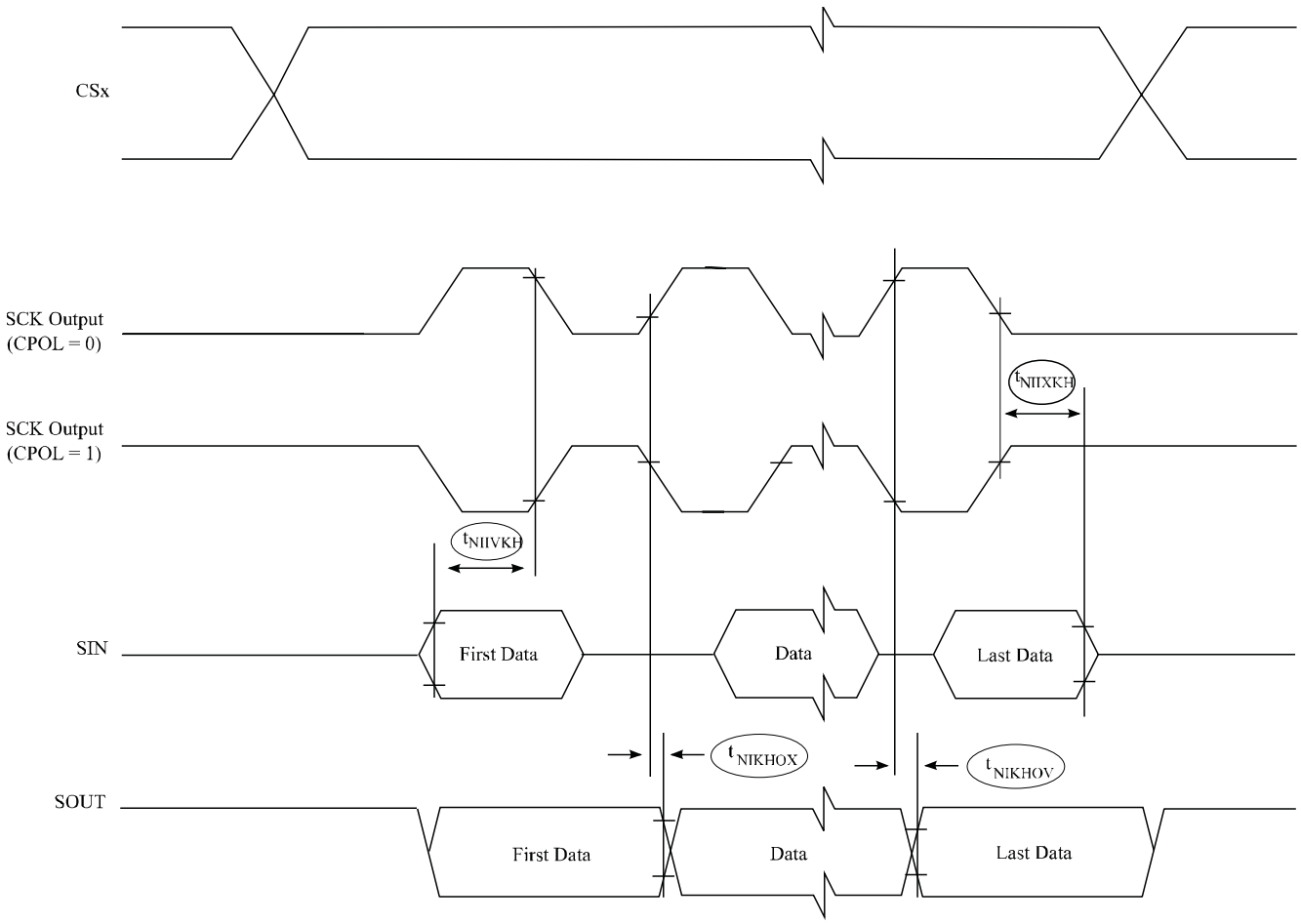
This figure shows the SPI timing master when CPHA = 0.

Figure 41. SPI timing master, CPHA = 0



This figure shows the SPI timing master when CPHA = 1.

Figure 42. SPI timing master, CPHA = 1



3.21 Universal serial bus 3.0 (USB)

This section describes the specification for the on-chip Super Speed (SS) USB 3.0 PHY signals. For High Speed (HS), Full Speed (FS) and Low Speed (LS) specifications of the USB PHY signals, see Chapter 7 in the Universal Serial Bus Revision 2.0 Specification for more information.

3.21.1 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at the package pins.

Table 57. USB 3.0 transmitter DC electrical characteristics (USB_HV_{DD} = 3.3V, USB_SV_{DD} = 0.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800.0	1000.0	1200.0	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400.0	-	1200.0	$mV_{p\text{-}p}$
Transmit de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3.0	-	4.0	dB

Parameter	Symbol	Min	Typ	Max	Unit
Differential impedance	Z_{diffTX}	72.0	100.0	120.0	Ω
Transmit common mode impedance	R_{TX-DC}	18.0	-	30.0	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX-CM-DC-ACTIVEIDLE-DELTA}$	-	-	200.0	mV
DC electrical idle differential output voltage	$V_{TX-IDLE-DIFF-DC}$	0.0	-	10.0	mV

Note:
1. For recommended operating conditions, see Recommended Operating Conditions

This table provides the USB 3.0 receiver DC electrical characteristics at the receiver package pins.

Table 58. USB 3.0 receiver DC electrical characteristics (USB_HV_{DD} = 3.3V, USB_SV_{DD} = 0.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX-DIFF-DC}$	72.0	100.0	120.0	Ω	-
Receiver DC common mode impedance	R_{RX-DC}	18.0	-	30.0	Ω	-
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX-HIGH-IMP-DC}$	25000.0	-	-	Ω	-
LFPS detect threshold	$V_{TRX-IDLE-DET-DC-DIFFpp}$	100.0	-	300.0	mV	2

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Below the minimum is noise. Must wake up above the maximum.

3.21.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 59. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	f_{USB}	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	200.0	200.06	ps	1
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-

Note:
1. UI does not account for SSC-caused variations.

This table provides the USB 3.0 receiver AC timing specifications at the receiver package pins.

Table 60. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1

Note:
1. UI does not account for SSC-caused variations.

This table provides the key LFPS electrical specifications at the transmitter.

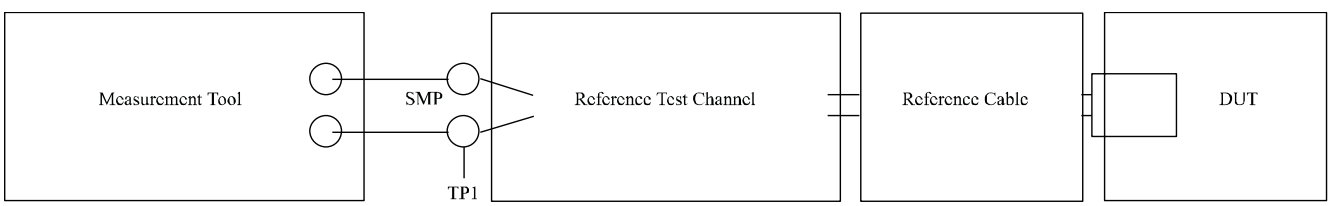
Table 61. LFPS electrical specifications at the transmitter 2

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-
Peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps}$	800.0	1200.0	mV	-
Rise/fall time	$t_{rise/fall}$	-	4.0	ns	1
Duty cycle	DC_{LFPS}	40.0	60.0	%	1, 2

Notes:
1. Measured at compliance TP1. See the Transmit normative setup figure below for details.
2. See Figure 43.

This figure shows the transmit normative setup with reference channel as per USB 3.0 specifications.

Figure 43. Transmit normative setup



3.22 Controller Automatic Network interface (CAN)

3.22.1 CAN DC electrical characteristics

This table provides the DC electrical characteristics for CAN-FD pins operating at OVDD = 1.8 V.

Table 62. DC electrical characteristics for CAN-FD (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x OVDD	V	2
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	µA	3

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, IOL = -0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions

3.22.2 CAN AC electrical characteristics

This table provides the CAN-FD AC timing specifications.

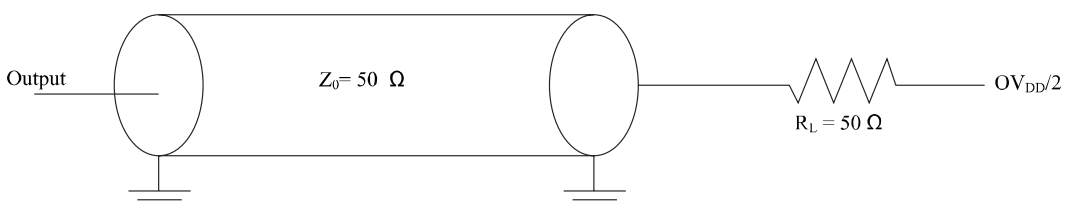
Table 63. CAN-FD AC timing specifications 1

Parameter	Min	Max	Unit
Baud rate	10.0	8000.0	kbps

Note:
1. See Figure 44.

This figure provides the CAN-FD AC test load.

Figure 44. FlexCAN AC test load



3.23 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, 1000Base-KX, USXGMII, XFI, SFI, 10GBase-KR, 25G-AUI, XLAUI, 40GBase-KR, 50GAUI-2, CAUI-4, and serial ATA (SATA) data transfers.

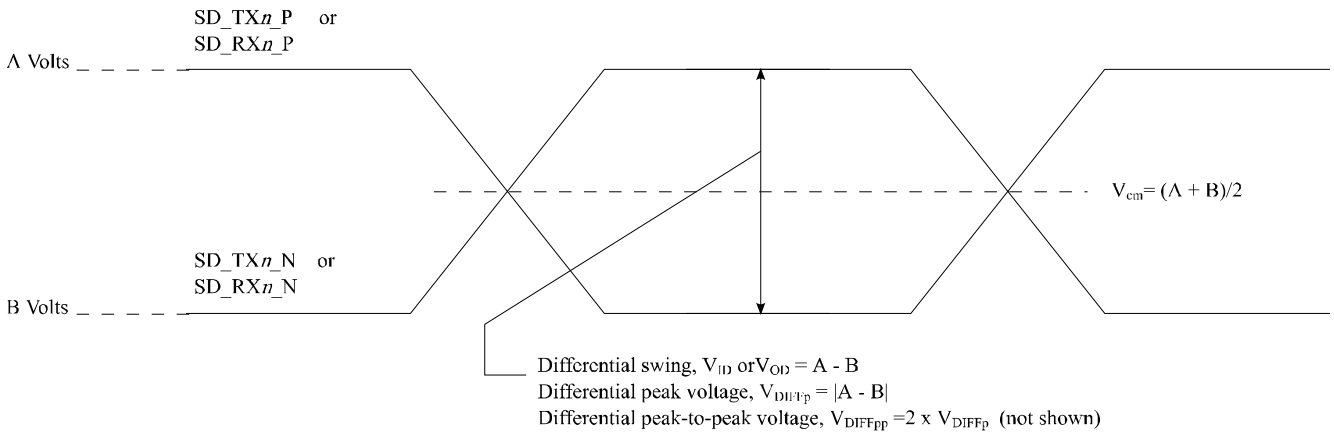
This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.23.1 Signal terms definitions

The SerDes uses differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

Figure 45. Differential voltage definitions for transmitter or receiver



Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing	The transmitter output signals and the receiver input signals SD_TXn_P, SD_TXn_N, SD_RXn_P and SD_RXn_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing)	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TX\ n}$_P - V_{SD_TXn}_N. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, VDIFFp	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, VDIFFp = |A - B| volts.
Differential Peak-to-Peak, VDIFFp-p	Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, VDIFFp-p = 2 x VDIFFp = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as VTX-DIFFp-p = 2 x |VOD|.
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal (SD_TXn_N, for example) from the non-inverting signal (SD_TXn_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 50 as an example for differential waveform.
Common Mode Voltage, Vcmv	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, Vcm_out = (VSD_TXn_P + VSD_TXn_N) ÷ 2 = (A + B) ÷ 2, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different

between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (VOD) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, VOD is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (VDIFFp) is 500 mV. The peak-to-peak differential voltage (VDIFFp-p) is 1000 mV p-p.

3.23.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_PLLF_REF_CLK_P/SD1_PLLF_REF_CLK_N

and SD1_PLLS_REF_CLK_P/SD1_PLLS_REF_CLK_N for SerDes 1, SD2_PLLF_REF_CLK_P/SD2_PLLF_REF_CLK_N and SD2_PLLS_REF_CLK_P/SD2_PLLS_REF_CLK_N for SerDes 2, and SD3_PLLF_REF_CLK_P/SD3_PLLF_REF_CLK_N and SD3_PLLS_REF_CLK_P/SD3_PLLS_REF_CLK_N for SerDes 3.

SerDes 1-3 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: SGMII, PCIe, USXGMII/XFI/SFI, 100GE, 50GE, 40GE, 25GE
- SerDes 2: SGMII, PCIe, USXGMII/XFI/SFI, SATA
- SerDes 3: PCIe

The following sections describe the SerDes reference clock requirements and provide application information.

3.23.2.1 SerDes spread-spectrum clock source recommendations

SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 64. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum- supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 64. SerDes spread-spectrum clock source recommendations 1

Parameter	Min	Max	Unit	Notes
Frequency modulation	**30**	**33**	**kHz**	**—**
Frequency spread	**+0**	**-0.5**	**%**	**2**

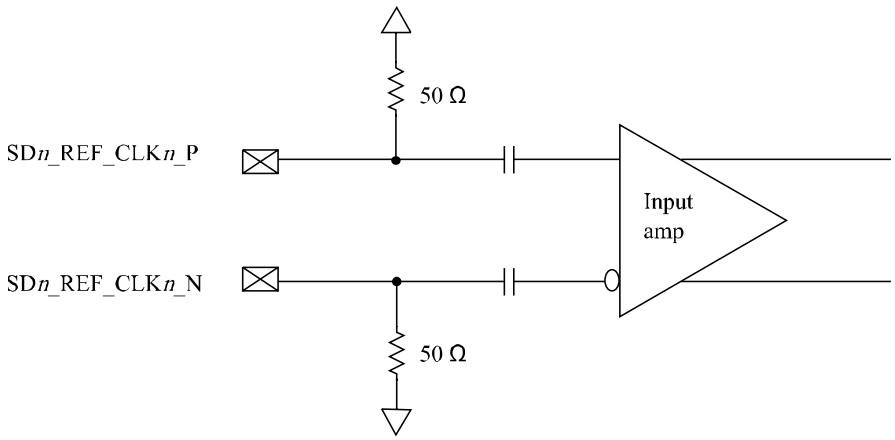
Notes:

1. At recommended operating conditions. See Recommended Operating Conditions.
2. Only down-spreading is allowed.

3.23.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

Figure 46. Receiver of SerDes reference clocks



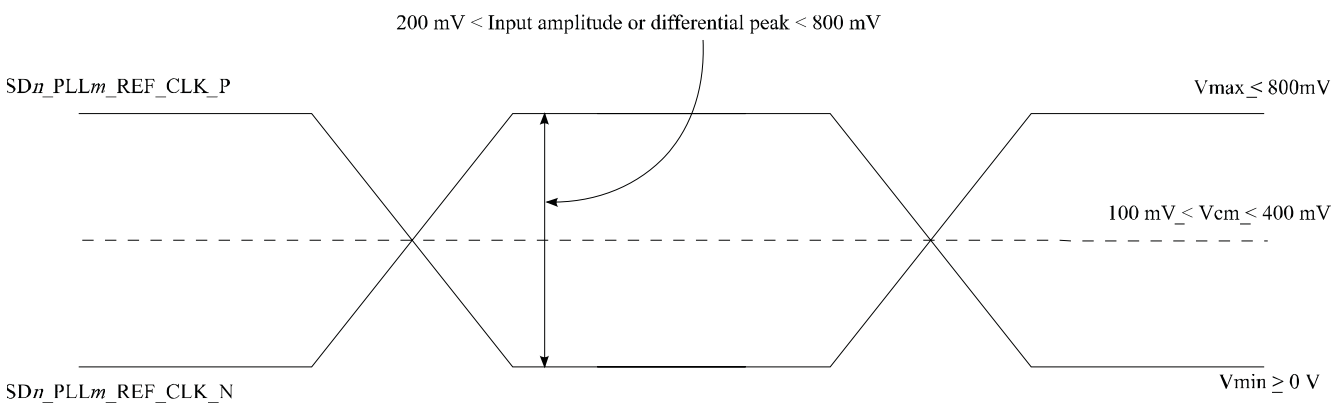
3.23.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

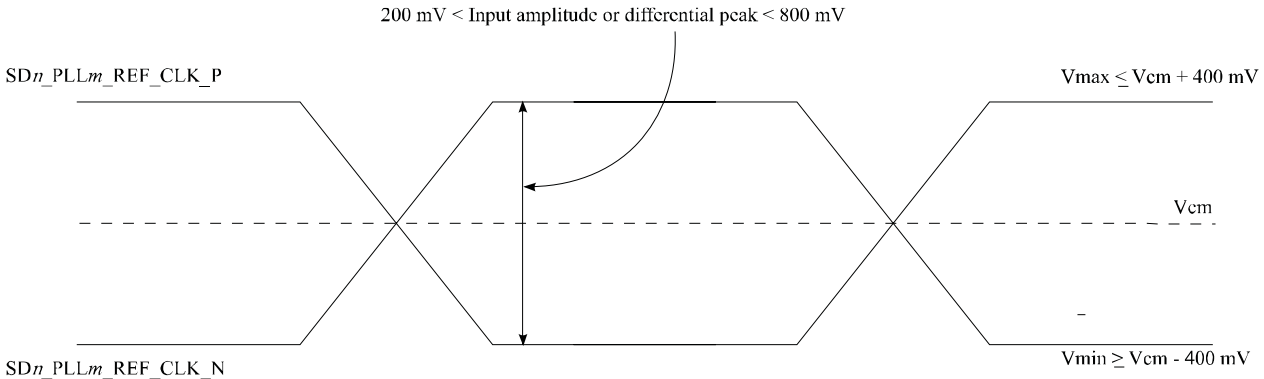
- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.
  Figure 47 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

Figure 47. Differential reference clock input DC requirements (external DC-coupled)



- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD_GND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SD_GND).
  Figure 48 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

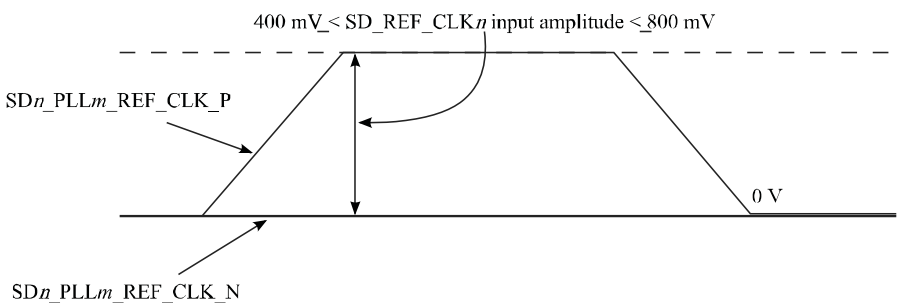
Figure 48. Differential reference clock input DC requirements (external AC-coupled)



Single-ended mode:

- The reference clock can also be single-ended. The SDn_PLLm_REF_CLK_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SDn_PLLm_REF_CLK_N either left unconnected or tied to ground.
- The SDn_PLLm_REF_CLK_P input average voltage must be between 200 and 400 mV. Figure 49 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SDn_PLLm_REF_CLK_N) through the same source impedance as the clock input (SDn_PLLm_REF_CLK_P) in use.

Figure 49. Single-ended reference clock input DC requirements



3.23.2.4 SerDes reference clocks AC timing specifications

For protocols with data rates up to 5 Gb/s where there is not reference clock jitter specification (ex: SGMII), use the PCIe 2.5G clock jitter requirements.

For protocols with data rates greater than 5 Gb/s and less than 8 Gb/s where there is no reference clock jitter specification, use the PCIe 5G clock jitter requirements.

For protocols with data rates greater than 8 Gb/s and less than 16 Gb/s where there is no reference clock jitter specification (ex: XLAUI, USXGMII-10.31.25G), use the PCIe 8G or XFI clock jitter requirements.

For protocols with data rates greater than 16 Gb/s where there is no reference clock jitter specification (ex: CAUI-4/50GAUI-2/25G- AUI use the PCIe 16G clock jitter requirements).

Use the protocol's reference clock frequency tolerance specification (ex: +/-100 ppm for SGMII/USXGMII/XFI/SFI/10GBaseKR/ 1000Base-KX/XLAUI/CAUI-4/50GAUI-2/25G-AUI and +/-300 ppm for PCIe).

This table defines the AC requirements for SerDes reference clocks for PCI Express. SerDes reference clocks need to be verified by the customer's application design.

Table 65. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for PCI Express

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_PLLm_REF_CLK_P/SDn_PLLm_REF_CLK_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	-
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N clock frequency tolerance	t_{CLK_TOL}	-300.0	-	300.0	ppm	1
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	2
PCIe 2.5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42.0	ps P-P	3, 4
PCIe 2.5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N total reference clock jitter at 10^{-6} BER	t_{CLK_TJ}	-	-	86.0	ps P-P	3, 4
PCIe 5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK-LF-RMS}$	-	-	3.0	ps RMS	5
PCIe 5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK-HF-RMS}$	-	-	3.1	ps RMS	5
PCIe 8G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N RMS reference clock jitter	$t_{REFCLK-RMS-DC}$	-	-	1.0	ps RMS	6
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N rising/ falling edge rate	t_{CLKRR}/ t_{CLKFR}	0.6	-	4.0	V/ns	7, 8
Differential input high voltage	V_{IH}	150.0	-	-	mV	2
Differential input low voltage	V_{IL}	-	-	-150.0	mV	2
Rising edge rate (SDn_PLLm_REF_CLK_P) to falling edge rate (SDn_PLLm_REF_CLK_N) matching	Rise-Fall matching	-	-	20.0	%	9, 10, 11

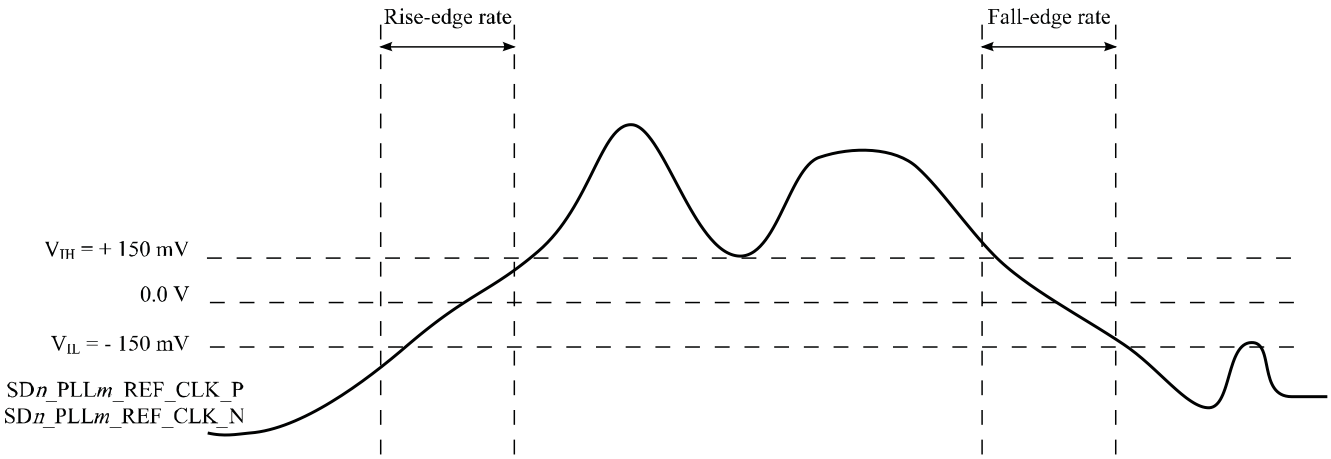
Notes:

1. For PCI Express (2.5, 5, and 8 GT/s).
2. Measurement taken from differential waveform.
3. Limits from PCI Express CEM Rev 2.0.
4. For PCI Express 2.5 GT/s
5. For PCI Express 5 GT/s
6. For PCI Express 8 GT/s
7. Measured from -150 mV to +150 mV on the differential waveform (derived from SDn_PLLm_REF_CLK_P minus SDn_PLLm_REF_CLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.
8. See Figure 50.

9. Measurement taken from single-ended waveform.
10. Matching applies to rising edge for SDn_PLLm_REF_CLK_P and falling edge rate for SDn_PLLm_REF_CLK_N. It is measured using a +/- 75 mV window centered on the median cross point where SDn_PLLm_REF_CLK_P rising meets SDn_PLLm_REF_CLK_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SDn_PLLm_REF_CLK_P must be compared to the fall edge rate of SDn_PLLm_REF_CLK_N, the maximum allowed difference should not exceed 20% of the slowest edge rate.
11. See Figure 51.

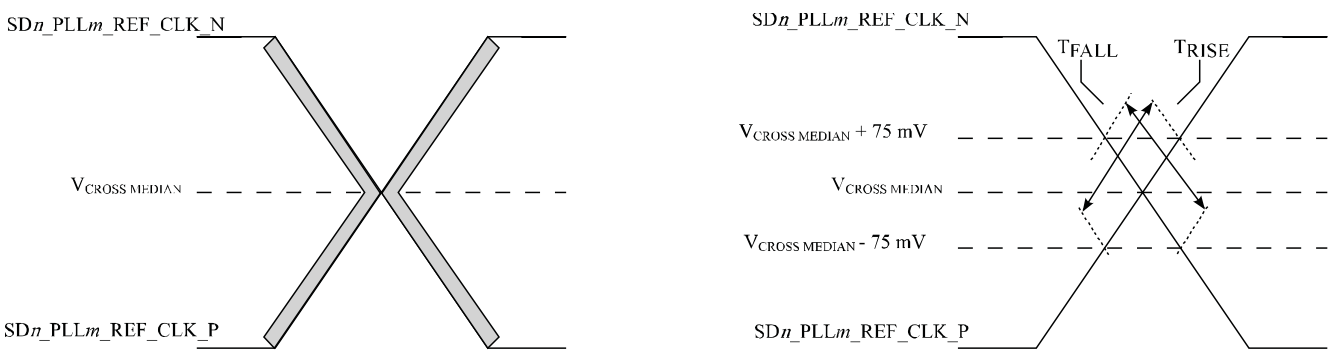
This figure shows the differential measurement points for rise and fall time.

Figure 50. Differential measurement points for rise and fall time



This figure shows the single-ended measurement points for rise and fall time matching.

Figure 51. Single-ended measurement points for rise and fall time matching



This table defines the AC requirements for SerDes reference clocks for XFI, SFI, XLAUI, and CAUI-4/50GAUI-2/25G-AUI. SerDes reference clocks need to be verified by the customer's application design.

Table 66. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for XFI, SFI, XLAUI, and CAUI-4/50GAUI-2/25G-AUI

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	t_{CLK_REF}	-	156.25/ 161.1328125	-	SFI MHz	-
Clock frequency tolerance	t_{CLK_TOL}	-100.0	-	100.0	ppm	-
Reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	1
Single side band noise at 1 kHz	at 1 kHz	-	-	-85.0	dBC/Hz	2
Single side band noise at 10 kHz	at 10 kHz	-	-	-108.0	dBC/Hz	2
Single side band noise at 100 kHz	at 100 kHz	-	-	-128.0	dBC/Hz	2
Single side band noise at 1 MHz	at 1 MHz	-	-	-138.0	dBC/Hz	2
Single side band noise at 10 MHz	at 10 MHz	-	-	-138.0	dBC/Hz	2
Random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
Total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11.0	ps	-
Spurious noise (1.2 MHz to 15 MHz)	NA	-	-	-75.0	dBC	-

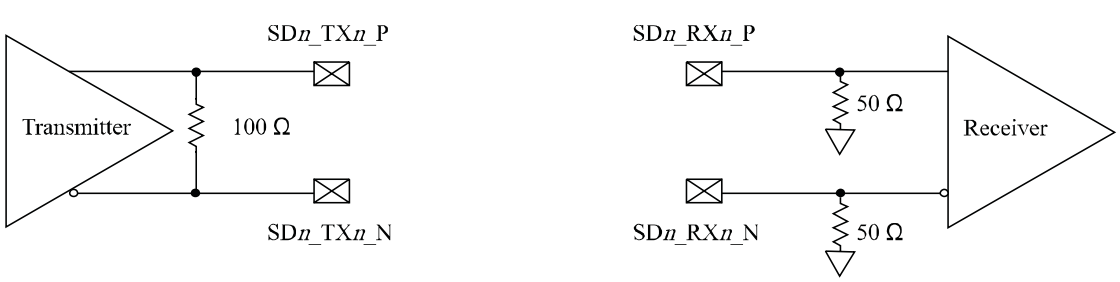
Notes:

1. Measurement taken from differential waveform.
2. Per XFP specification, Rev 4.5, the Module Jitter Generation spec at XFI optical output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode, the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

3.23.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 52. SerDes transmitter and receiver reference circuits



The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- SATA
- SGMII
- USXGMII
- XFI
- SFI
- 10GBase-KR
- CAUI-4, 50GAUI-2, 25G-AUI
- XLAUI
- 40GBase-KR

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.23.4 PCI Express

3.23.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.23.4.2 PCI Express clocking requirements for SDn_PLLF_REF_CLK and SDn_PLLS_REF_CLK

SerDes 1/2/3 SD[1:3]_PLLF_REF_CLK/SD[1:3]_PLLF_REF_CLK_B and SD[1:3]_PLLS_REF_CLK/SD[1:3]_PLLS_REF_CLK_B

may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is supported on SerDes 1, 2, and 3.

For more information on these specifications, see SerDes reference clocks.

3.23.4.3 PCI Express DC electrical characteristics

This section describes the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 1.0 (2.5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 67. PCI Express 1.0 (2.5 GT/s) differential transmitter output DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFP\text{-}P}$	800.0	1000.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	3
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40.0	50.0	60.0	Ω	5

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{TX\_DIFFp-p} = 2 \times | V_{TX-D+} - V_{TX-D-} |$
3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
4. Transmitter DC differential mode low impedance
5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 68. PCI Express 1.0 (2.5 GT/s) differential receiver input DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	175.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{RX\_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$
3. Measured at the package pins with a test load of 50Ω to GND on each pin.
4. Receiver DC differential mode impedance.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.
6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).
7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.
8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.
9. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

This table defines the PCI Express 2.0 (5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 69. PCI Express 2.0 (5 GT/s) differential transmitter output DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFP-P}$	800.0	1000.0	1200.0	mV	2
Low power differential peak-peak output voltage	$V_{TX-DIFFP-P-LOW}$	400.0	500.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	3
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	5

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{TX\_DIFFp-p} = 2 \times | V_{TX-D+} - V_{TX-D-} |$
3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
4. Transmitter DC differential mode low impedance
5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 70. PCI Express 2.0 (5 GT/s) differential receiver input DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	120.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{RX\_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$
3. Measured at the package pins with a test load of 50Ω to GND on each pin.
4. Receiver DC differential mode impedance.

5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.
6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).
7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.
8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.
9. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times | V_{RX\text{-}D+} - V_{RX\text{-}D-} |$

This table defines the PCI Express 3.0 (8 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 71 PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$	800.0	-	1300.0	mVp-p	2
Reduced swing transmitter voltage with no TX Eq	$V_{TX\text{-}RS\text{-}NO\text{-}EQ}$	400.0	-	1300.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	3
Minimum swing during EIEOS for full swing	$V_{TX\text{-}EIEOS\text{-}FS}$	250.0	-	-	mVp-p	4
Minimum swing during EIEOS for reduced swing	$V_{TX\text{-}EIEOS\text{-}RS}$	232.0	-	-	mVp-p	4
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80.0	100.0	120.0	Ω	5
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40.0	50.0	60.0	Ω	6

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage measurements for $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ and $V_{TX\text{-}RS\text{-}NO\text{-}EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.
3. Ratio of $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
4. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV $_{P\text{-}P}$ at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.
5. Transmitter DC differential mode low impedance
6. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 72. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	2, 3
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	4, 5, 3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	6, 7
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	8, 5
Generator launch voltage	$V_{RX-LAUNCH-8G}$	-	800.0	-	mV	9
Eye height (-20dB channel)	$V_{RX-SV-8G}$	25.0	-	-	mV	10
Eye height (-12dB channel)	$V_{RX-SV-8G}$	50.0	-	-	mV	10
Eye height (-3dB channel)	$V_{RX-SV-8G}$	200.0	-	-	mV	10

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Receiver DC differential mode impedance.
3. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.
4. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).
5. Measured at the package pins with a test load of 50Ω to GND on each pin.
6. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.
7. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.
8. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$
9. Measured at TP1 per PCI Express base specification Rev 3.0.
10. Measured at TP2 per PCI Express base specification Rev 3.0. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. In the parameter names, "SV" refers to stressed voltage. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2.

3.23.4.4 PCI Express AC timing specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 1.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The ACtiming specifications do not include RefClk jitter.

Table 73. PCI Express 1.0 (2.5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	6, 3, 4, 5
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

Notes:

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.
3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.
4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
5. See Figure 53.
6. Jiiter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI.
7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the AC timing specifications for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	3, 4, 5

Notes:

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.
3. Jitter is defined as the measurement variation of the crossing points (VRX-DIFFp-p = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI.
4. A T RX-EYE = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T RX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 75. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	6
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

Notes:

1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.

3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.
4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
5. See Figure 53.
6. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
7. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
8. Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps.

This table defines the AC timing specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 76. PCI Express 2.0 (5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.4	200.0	200.06	ps	1
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	-
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.3	UI	-

Note:
1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1
AC coupling capacitor	C_{TX}	176.0	-	265.0	nF	2, 3
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12.0	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24.0	ps p-p	4, 5
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10.0	ps p-p	4, 5
Data-dependent jitter	T_{TX-DDJ}	-	-	18.0	ps p-p	4, 5, 6

Notes:

1. Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. Measured with optimized preset value after de-embedding to transmitter pin.
5. PWJ parameters shall be measured after data-dependent jitter (DDJ) separation.
6. The AC specifications do not include Refclk jitter

This table defines the AC timing specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications

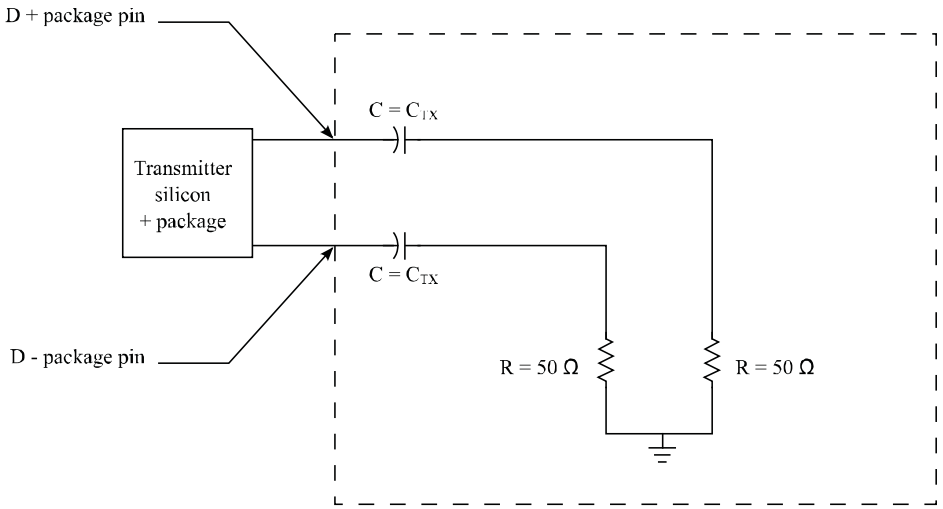
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1, 2
Eye width at TP2P	$T_{RX-SV-8G}$	0.3	-	0.35	UI	2
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14.0	-	-	mV	3
Sinusoidal jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	-	-	0.1	UI p-p	4, 5
Random jitter	$T_{RX-SV-RJ-8G}$	-	-	2.0	ps RMS	6, 5

Notes:

1. Each UI is 125 ps ± 300 ppm. UI does not account for spreadspectrum clock dictated variations.
2. T_{RX-SV} is referenced to TP2P and is obtained after post-processing data is captured at TP2. T_{RX-SV} includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
3. Frequency = 2.1GHz. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
4. Fixed at 100 MHz. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency.
5. See Figure 54.
6. Random jitter spectrally flat before filtering. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$

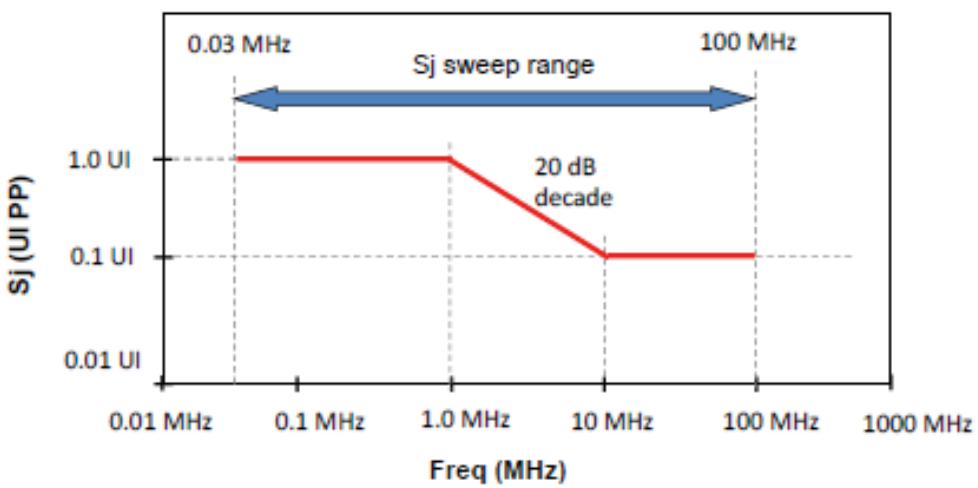
The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure. Note that the allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and Dpackage pins.

Figure 53. Test and measurement load



This figure shows the swept sinusoidal jitter mask.

Figure 54. Swept sinusoidal jitter mask



3.23.5 Serial ATA (SATA)

3.23.5.1 SATA DC electrical characteristics

This table provides the differential transmitter output DC characteristics for the SATAinterface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 79. SATA Gen 1i/1m 1.5G transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA\_TXDI\ FF}$	400.0	500.0	600.0	mVp-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA\_TXDI\ FFIM}$	85.0	100.0	115.0	Ω	DC impedance.

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Terminated by a 50Ω load.
3. DC impedance.

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 80. SATA Gen 1i/1m 1.5G receiver input DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA\_RXDI\ FF}$	240.0	500.0	600.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA\_RXS\ EIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	50.0	120.0	240.0	mV p-p	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage relative to common of either signal comprising a differential pair.
3. DC impedance.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 81. SATA Gen 2i/2m 3G transmitter DC electrical characteristics (SD_OV DD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA\_TXDI\ FF}$	400.0	-	700.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA\_TXDI\ FFIM}$	85.0	100.0	115.0	Ω	DC impedance.

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.

2. Terminated by a 50Ω load.
3. DC impedance.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 82. SATA Gen 2i/2m 3G receiver input DC electrical characteristics (SD_SV DD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA\_RXDI\ FF}$	240.0	-	750.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA\_RXS\ EIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	75.0	120.0	240.0	mV p-p	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage relative to common of either signal comprising a differential pair.
3. DC impedance.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 83. SATA Gen 3i transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA\_TXDI\ FF}$	240.0	-	900.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA\_TXDI\ FFIM}$	85.0	100.0	115.0	Ω	DC impedance.

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Terminated by a 50Ω load.
3. DC impedance.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 84. SATA Gen 3i receiver input DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA\_RXDI FF}$	240.0	-	1000.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA\_RXS EIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	75.0	120.0	200.0	mV p-p	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage relative to common of either signal comprising a differential pair.
3. DC impedance.

3.23.5.2 SATA AC timing specifications

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 85. SATA reference clock input requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn_P/ SDn_REF_CLKn_N frequency range	t_{CLK_REF}	-	100 / 125	-	MHz	1
SDn_REF_CLK z_P/ SDn_REF_CLKn_N frequency tolerance	t_{CLK_TOL}	-350.0	-	350.0	ppm	-
SDn_REF_CLKn_P/ SDn_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	2
SDn_REF_CLKn_P/ SDn_REF_CLKn_N cycle-to- cycle clock jitter (period jitter)	t_{CLK_CJ}	-	-	100.0	ps	3
SDn_REF_CLKn_P/ SDn_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50.0	-	50.0	-	3, 4, 5

Notes:
1. Caution: Only 100 MHz and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. Measurement taken from differential waveform.
3. At RefClk input.
4. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
5. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 1i/1m 1.5 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ\ 5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ\ 250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ\ 5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ\ 250UI}$	-	-	0.22	UI p-p	1

Note:
1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 1i/1m 1.5 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Total jitter, data-data 5 UI	$U_{SATA\_RXTJ\ 5UI}$	-	-	0.43	UI p-p	Measured at the receiver.
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ\ 250UI}$	-	-	0.6	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ\ 5UI}$	-	-	0.25	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ\ 250UI}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 88. Gen 2i/2m 3 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	-	-	0.37	UI p-p	1
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJ\ fB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJ\ fB/1667}$	-	-	0.35	UI p-p	1

Note:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 89. Gen 2i/2m 3 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	-	-	0.6	UI p-p	Measured at the receiver.
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJ\ fB/1667}$	-	-	0.65	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	-	-	0.42	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJ\ fB/1667}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 90. Gen 3i transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Channel speed	t_{CH_SPEED}	-	6.0	-	Gbps
Total jitter before and after compliance interconnect channel	J_T	-	-	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 91. Gen 3i receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Total jitter before and after compliance interconnect channel	J_T	-	-	0.6	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

3.23.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in 4-wire AC-coupled SGMII serial link connection example, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in SerDes transmitter and receiver reference circuits.

3.23.6.1 SGMII DC electrical characteristics

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N), as shown in the SGMII transmitter DC measurement circuit figure below.

Table 92. SGMII DC transmitter electrical characteristics (SD_OV_{DD} = 1.8V) [1,12,13]

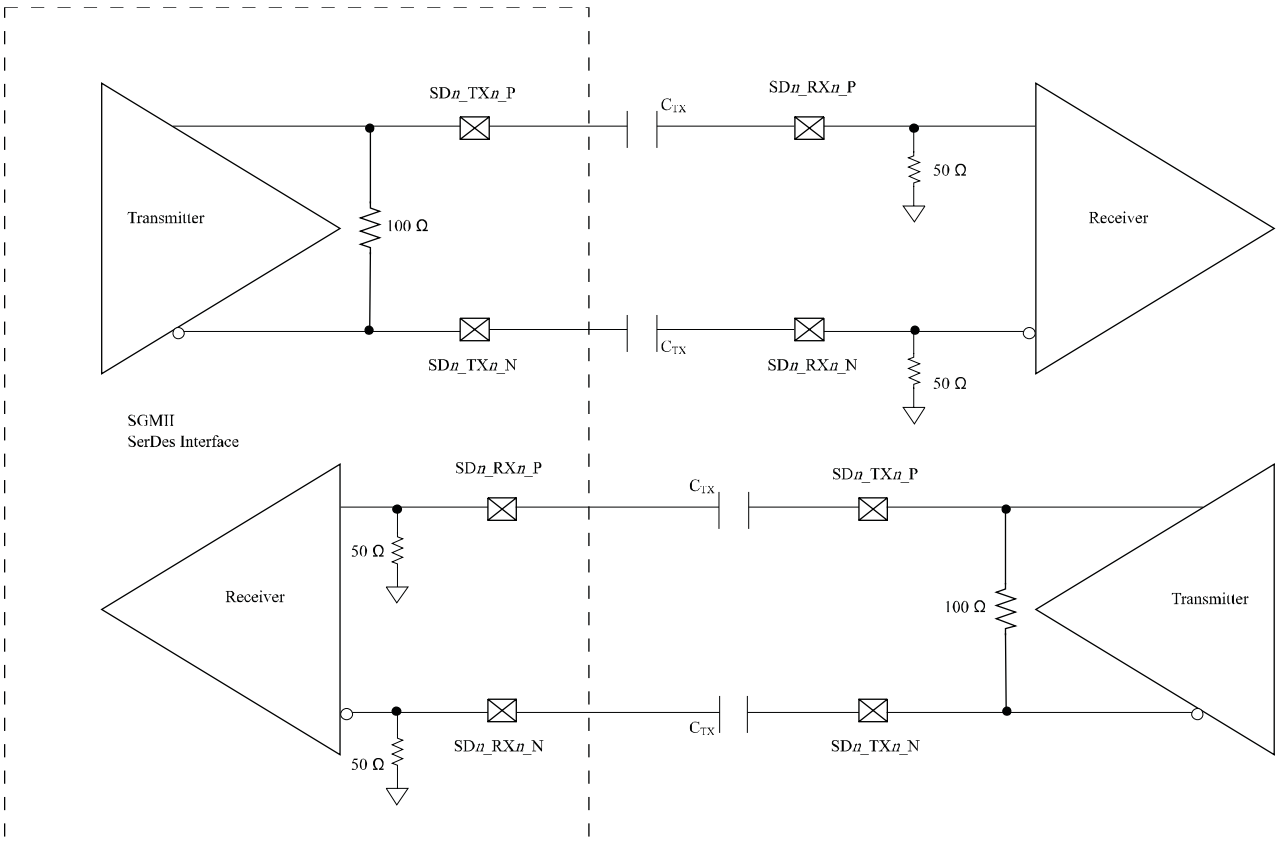
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\|V_{OD}\|_{-max}$	mV	2
Output low voltage	V_{OL}	$\|V_{OD}\|_{-min}/2$	-	-	mV	2
Output differential voltage	$\|V_{OD}\|$	320.0	500.0	725.0	mV	3, 4, 5
Output differential voltage	$\|V_{OD}\|$	293.8	459.0	665.6	mV	3, 4, 6
Output differential voltage	$\|V_{OD}\|$	266.9	417.0	604.7	mV	3, 4, 7
Output differential voltage	$\|V_{OD}\|$	240.6	376.0	545.2	mV	3, 4, 8
Output differential voltage	$\|V_{OD}\|$	213.1	333.0	482.9	mV	3, 4, 9
Output differential voltage	$\|V_{OD}\|$	186.9	292.0	423.4	mV	3, 4, 10
Output differential voltage	$\|V_{OD}\|$	160.0	250.0	362.5	mV	3, 4, 11
Output impedance (differential)	R_O	80.0	100.0	120.0	Ω	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. This does not align to DC-coupled SGMII.
3. $|V_{OD}| = |V_{SD\_TXn\_P} - V_{SD\_TXn\_N}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
4. The $|V_{OD}|$ value shown in Typ column is based on the condition of SD_OVDD-Typ, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn_TXn_P and SDn_TXn_N.
5. LNmTECR0[EQ_AMP_RED]=0b000000
6. LNmTECR0[EQ_AMP_RED]=0b000001
7. LNmTECR0[EQ_AMP_RED]=0b000011
8. LNmTECR0[EQ_AMP_RED]=0b000010
9. LNmTECR0[EQ_AMP_RED]=0b000110 (default)
10. LNmTECR0[EQ_AMP_RED]=0b000111
11. LNmTECR0[EQ_AMP_RED]=0b010000
12. See Figure 55.
13. See Figure 56.

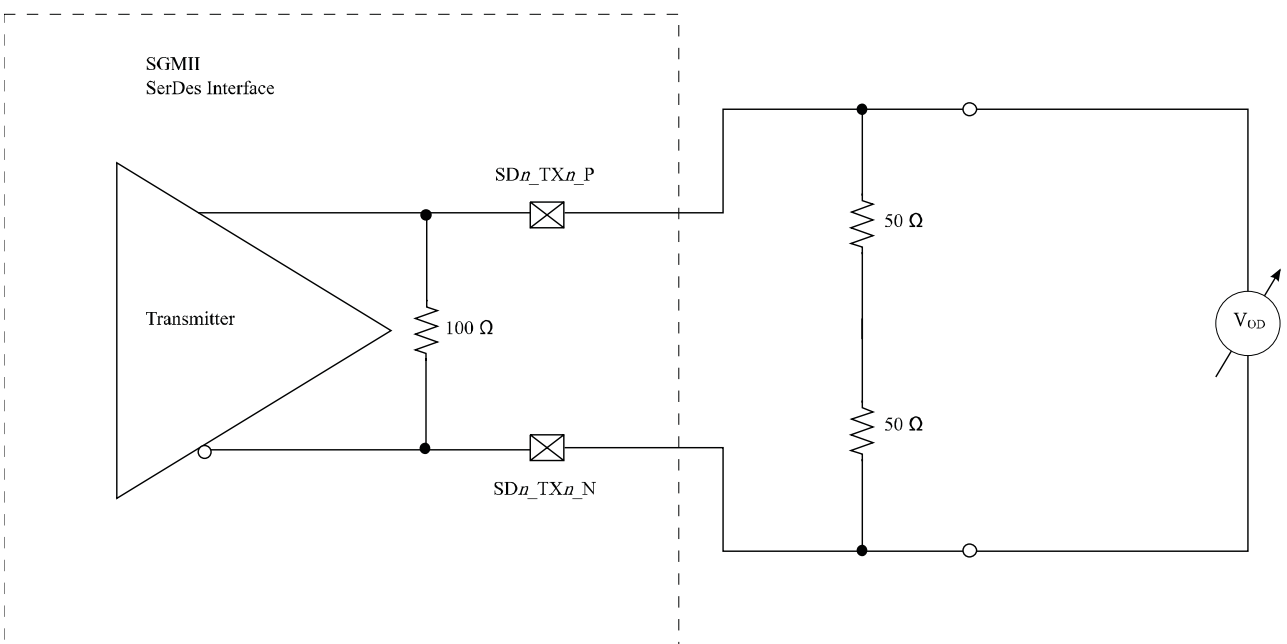
This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

Figure 55. 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

Figure 56. SGMII transmitter DC measurement circuit



This table lists the SGMII DC receiver electrical characteristics. Source synchronousclocking is not supported. Clock is recovered from the data.

Table 93 SGMII DC receiver electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Max	Unit	Notes
DC input voltage range	V_{IN}	N/A	N/A	-	2
Input differential voltage (default)	$V_{RX\_DIFFp\text{-}p}$	100.0	1200.0	mV	3, 5
Input differential voltage	$V_{RX\_DIFFp\text{-}p}$	175.0	1200.0	mV	3, 6
Loss of signal threshold (default)	V_{LOS}	30.0	100.0	mV	4, 5
Loss of signal threshold	V_{LOS}	65.0	175.0	mV	4, 6
Receiver differential input impedance	Z_{RX_DIFF}	80.0	120.0	Ω	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Input must be externally AC coupled.
3. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express.
5. LNmRGCR1[DATA_LOST_TH_SEL]=001
6. LNmRGCR1[DATA_LOST_TH_SEL]=100

3.23.6.2 SGMII AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

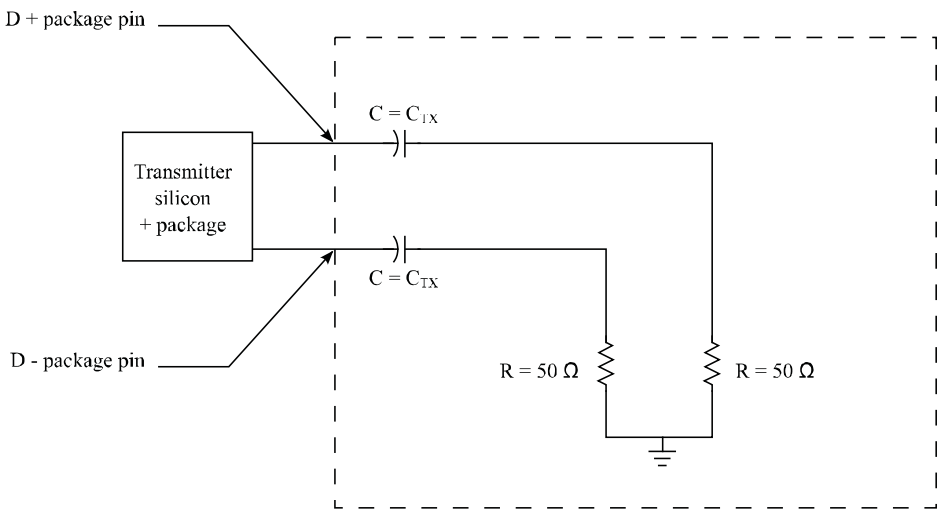
Table 94. SGMII transmitter AC timing specifications 4

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	-	-	0.17	UI p-p	-
Total jitter	J_T	-	-	0.35	UI p-p	1
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	2
AC coupling capacitor	C_{TX}	10.0	-	200.0	nF	3

Notes:
1. See Figure 58.
2. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. See Figure 57.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N) or at the receiver inputs (SDn_RXn_P and SDn_RXn_N) respectively, as shown in this figure.

Figure 57. SGMII AC test/measurement load



This table provides the SGMII receiver AC timing specifications. TheAC timing specifications do not include RefClk jitter. Source synchronous clocking is notsupported. Clock is recovered from the data.

Table 95. SGMII receiver AC timing specifications 3

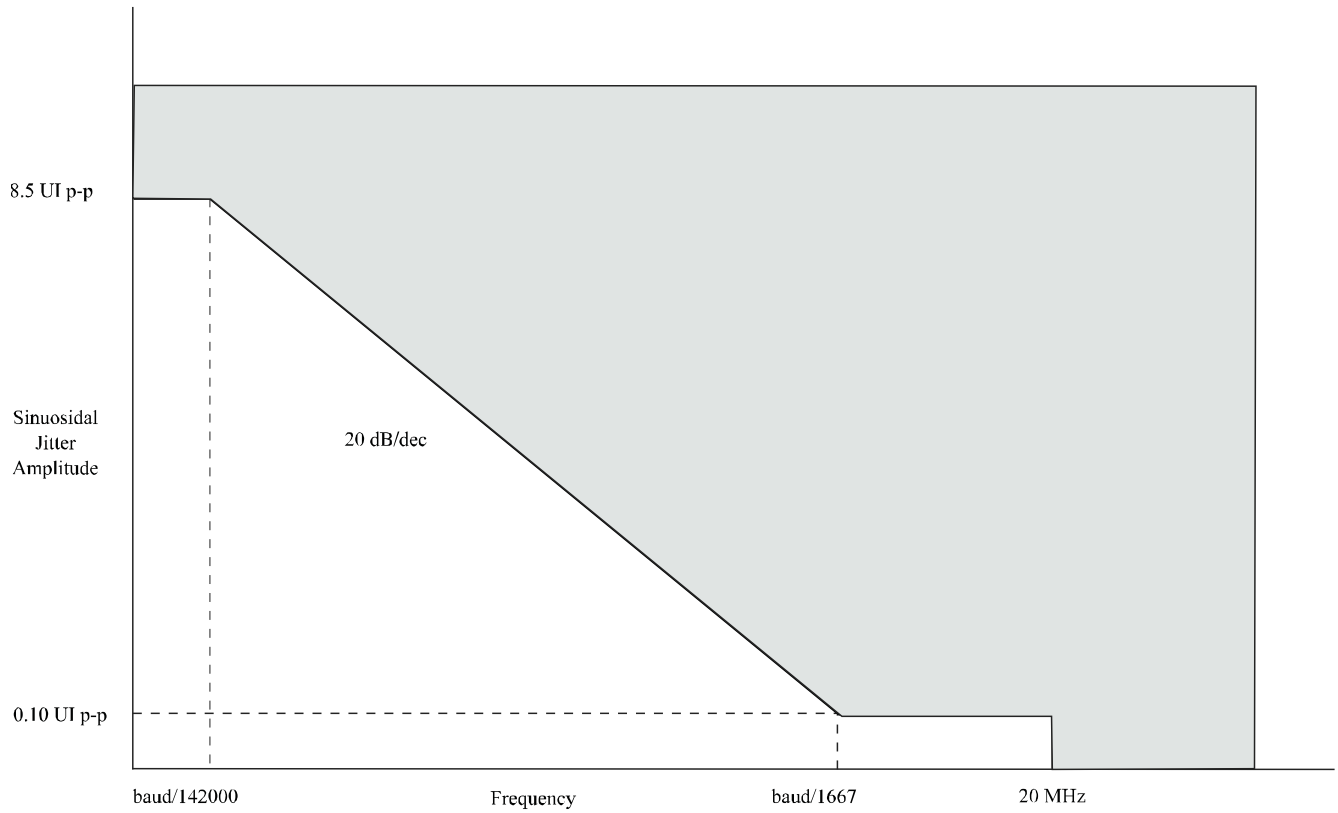
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2, 3
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	1
Bit error ratio	BER	-	-	10^{-12}	-	-

Notes:

1. Measured at receiver.
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of the Single-frequency sinusoidal jitter limits figure shown below. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. See Figure 58.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

Figure 58. Single-frequency sinusoidal jitter limits



3.23.7 XFI

3.23.7.1 XFI DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 96. XFI transmitter DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360.0	-	770.0	mV	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5d\ B}$	3.0	3.5	4.0	dB	4
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0d\ B}$	5.5	6.0	6.5	dB	6

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5d\ B}$	9.0	9.5	10.0	dB	7
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000111
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the XFI receiver DC electrical characteristics.

Table 97. XFI receiver DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	R_{RD}	80.0	100.0	120.0	Ω	-
Input differential voltage	$V_{RX-DIFF}$	110.0	-	1050.0	mV	2

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Measured at receiver.

3.23.7.2 XFI AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 98. XFI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter tolerance	T_J	-	-	0.3	UI p-p

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 99. XFI receiver AC timing specifications 3

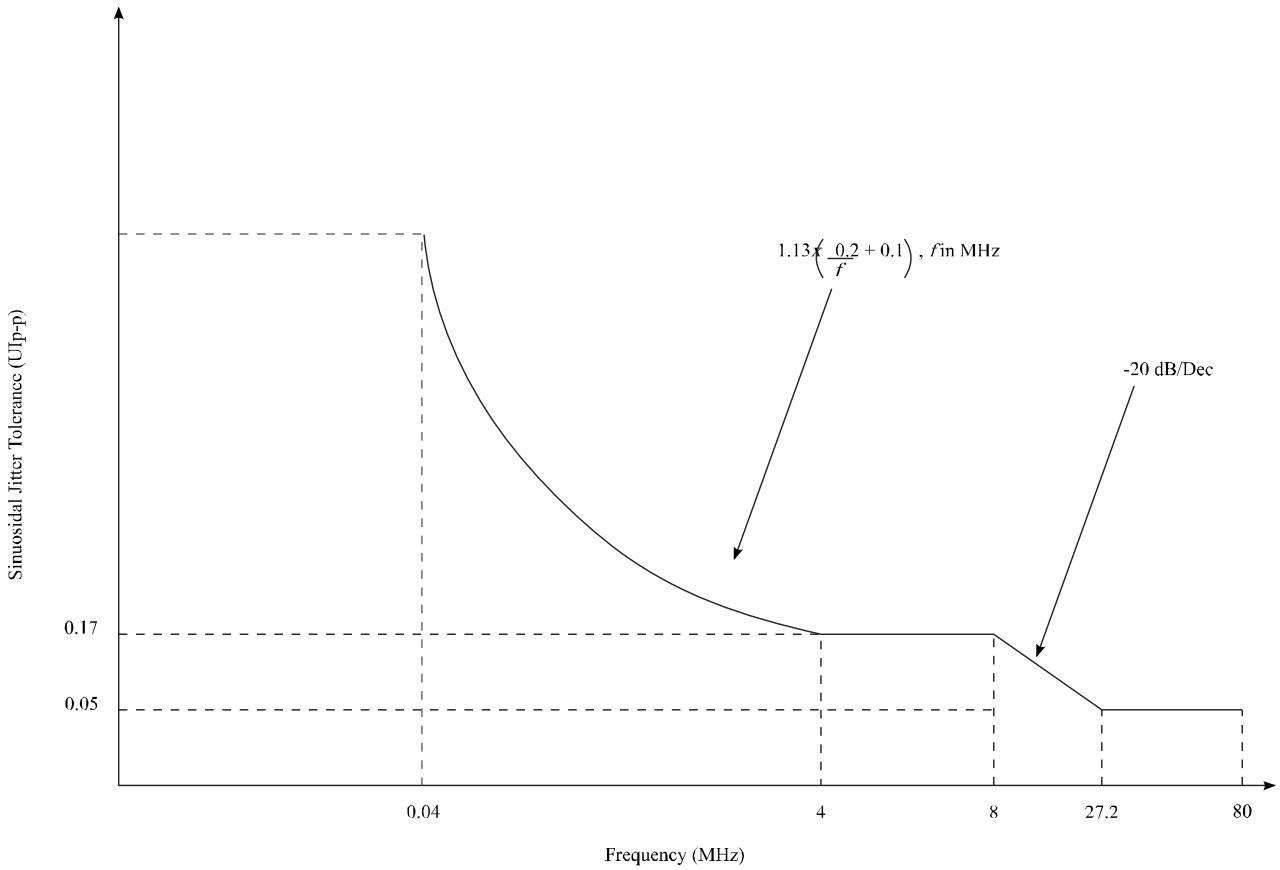
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

Notes:

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.
3. See Figure 59.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

Figure 59. XFI host receiver input sinusoidal jitter tolerance



3.23.8 SFI

This section presents the SFI+ specifications at data rate 10.3125Gb/s.

3.23.8.1 SFI DC electrical characteristics

This table defines the SFI+ transmitter DC electrical characteristics.

Table 100. SFI+ host transmitter DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	190	-	700	mV_{p-p}	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5d\ B}$	3	3.5	4	dB	4
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0d\ B}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX\text{-}DE\text{-}RATIO\text{-}9.5d\ B}$	9	9.5	10	dB	7
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000111
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the SFI+ host receiver DC electrical characteristics.

Table 101. SFI+ host receiver DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	R_{RD}	80		120	Ω	-
Input differential voltage	$V_{RX\text{-}DIFF}$	300	-	850	$mV_{p\text{-}p}$	-

Note:
1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.8.2 SFI AC timing specifications

This table defines the SFI+ host transmitter AC timing specifications.

Table 102. SFI+ host transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Data dependent jitter	DDJ	-	-	0.1	UI p-p
Data dependent pulse width shrinkage	DDPWS			0.055	UI p-p
Uncorrelated jitter	UJ			0.023	UI (RMS)
Total jitter tolerance	T_J	-	-	0.28	UI p-p

Notes:

1. Duty cycle distortion (DCD) and Pulse Width Shrinkage (DDPWS) are components of DDJ. DDJ is the range (max-min) of the timing variations.
2. The AC specifications do not include Refclk jitter.

This table defines the SFI+ host receiver AC timing specifications.

Table 103. SFI+ host receiver AC timing specifications

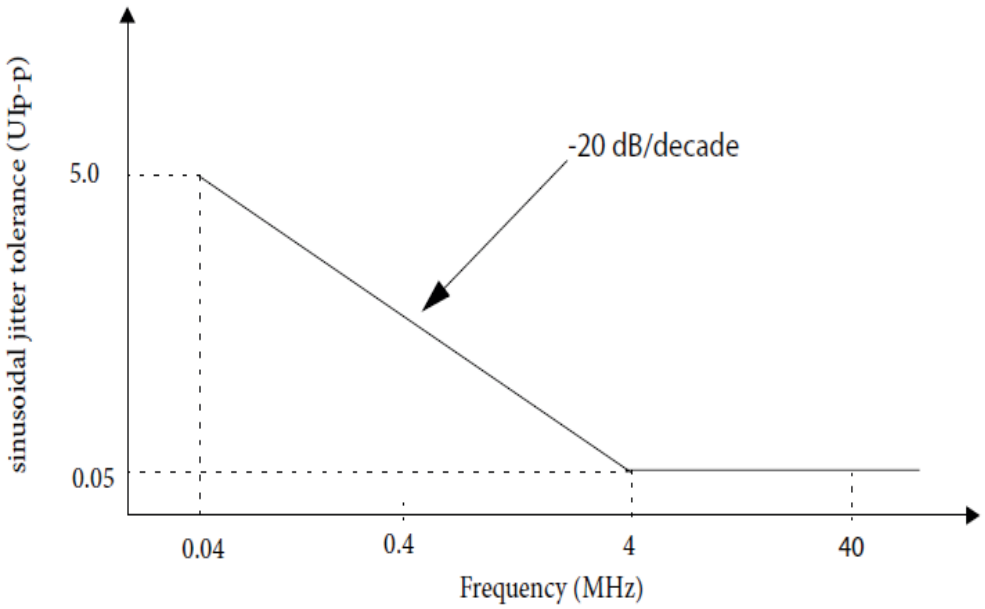
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
99% jitter	J2			0.42		1
Pulse width shrinkage jitter	DDPWS	-	-	0.3	UI p-p	2
Total jitter	T_J	-	-	0.7	UI p-p	

Notes:

1. The 99% jitter is per SFF-8431 Rev4.1 and includes sinusoidal jitter, per Figure 60.
2. In practice the test implementer may trade DDPWS with other pulse width shrinkage from the sinusoidal interferer per SFF-8431 Rev4.1.
3. The SFI total channel Link Budget when measured with Host Compliance board is 9.0 dB @5.5GHz. The channel
4. loss including connector measured with Host Compliance board @ 5.5GHz is 6.5dB. The penalty for reflections and other impairments is 2.5dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.
5. The AC specifications do not include Refclk jitter.

This figure shows the sinusoidal jitter tolerance of SFI receiver.

Figure 60. SFI+ SR and LR host receiver input datacom sinusoidal jitter tolerance



3.23.9 SFP+ direct attach copper

SFP+ direct attach copper is supported for passive copper cable compliant per SFF-8472.

3.23.9.1 SFP+ direct attach copper DC electrical characteristics

The SFP+ host supporting direct attach cables must meet transmitter output DC specifications in Table 100 at reference point B per SFF-8472. In addition, the SFP+ host transmitter must meet the specifications in the table below.

This table defines the SFP+ host transmitter output DC specifications.

Table 104. SFP+ host transmitter output DC electrical characteristics at B for Cu (SD_OVDD = 1.8V) 1

Parameters - B	Symbol	Min	Typ	Max	Unit
Voltage modulation amplitude (p-p)	VMA	300			mV
Transmitter Qsq	Qsq	63.1			
Output AC common mode voltage				12.0	mV (RMS)
Host output TWDPc	TWDPc			10.7	dBe

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. Qsq = 1/RN if the one level and zero level noises are identical. RN is relative noise per SFF-8472.
3. Host electrical output measured with LRM 14 taps FFE and 5 taps DFE Equalizer with PRBS9 for copper direct attach stressor.
4. The TWDPc is the host transmitter penalty for copper cable stressor.

The SFP+ host supporting direct attach cables must meet the receiver output DC specifications in Table 101.

3.23.9.2 SFP+ direct attach AC timing specifications

The SFP+ host supporting direct attach cables must meet the transmitter output AC specifications in Table 102 at reference point B per SFF-8472.

The SFP+ host supporting direct attach cables must meet the AC specifications in Table 103 in at reference point B per SFF-8472. In addition, the SFP+ host receiver must meet required 1×10^{-12} BER when tested with the stressed signal described per SFF-847.

3.23.10 1000Base-KX

3.23.10.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3-2015. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 105. 1000Base-KX transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800.0	-	1600.0	mV	2
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.
2. SRDSxLNmTECR0[EQ_AMP_RED]=00_0000

This table provides the 1000Base-KX receiver DC timing specifications.

Table 106. 1000Base-KX receiver DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFFp-p}$	-	1600.0	mV
Differential resistance	T_{RDIN}	80.0	120.0	Ω

Note:
1. For recommended operating conditions, see Recommended Operating Conditions

3.23.10.2 1000Base-KX AC timing specifications

This table defines the 1000Base-KX transmitter AC timing specifications.

Table 107. 1000Base-KX transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ}/T_{RJ}	-	-	0.15	UI p-p	-
Deterministic jitter tolerance	T_{DJ}	-	-	0.1	UI p-p	-
Total jitter tolerance	T_{TJ}	-	-	0.25	UI p-p	1

Note:
1. Total jitter is specified at a BER of 10^{-12}.

This table defines the 1000Base-KX receiver AC timing specifications.

Table 108. 1000Base-KX receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Total jitter tolerance	R_{TJ}	-	-	Per IEEE 802.3ap-clause 70.	UI p-p	1
Random jitter	R_{RJ}	-	-	0.15	UI p-p	2
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.1	UI p-p	1

Notes:
1. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
2. Random jitter is specified at a BER of 10^{-12}.

3.23.11 10GBase-KR

3.23.11.1 10GBase-KR clocking requirements for SDn_REF_CLKn and SDn_REF_CLKn_B

Only SerDes 1 and SerDes 2 may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks .

3.23.11.2 10GBase-KR DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 109. 10GBase-KR transmitter DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	4
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5d B}$	9.0	9.5	10.0	dB	7
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

Notes:
1. For recommended operating conditions, see Recommended Operating Conditions.

2. LNmTECR0[EQ_AMP_RED]= 000000
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 110. 10GBase-KR receiver DC electrical characteristics (SD_SV DD = 0.9V)1

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	1200.0	mV
Differential resistance	R_{RD}	80.0	120.0	Ω

Note:
1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.11.3 10GBase-KR AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 111. 10GBase-KR transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Deterministic jitter	T_DJ	-	-	0.15	UI p-p
Total jitter	T_TJ	-	-	0.3	UI p-p

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 112. 10GBase-KR receiver AC timing specifications 3

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Total jitter	T_J	-	-	1.0	UI p-p	1, 2
Random jitter	R_J	-	-	0.13	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1

Notes:
1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max, where ISI is jitter due to frequency dependent loss.
3. TX equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

3.23.12 CAUI-4, 50GAUI-2, and 25G-AUI interface

The IEEE Std 802.3-2015. 100 Gb/s Attachment Unit Interface (CAUI-4) is intended for use as a chip-to-chip or a chip-to-module interface. The four-lane version (CAUI-4) in Annex 83D and Annex 83E supports 100GbE. Each lane operates at 25.78125 GBaud. 50GAUI-2 supports 50GbE (2 lanes, each running @ 25.78125 GBaud) and 25G-AUI supports 25GbE (single lane @ 25.78125 GBaud)

3.23.12.1 CAUI-4/50GAUI-2/25G-AUI DC electrical characteristics

This table defines the CAUI-4/50GAUI-2/25G-AUI transmitter DC electrical characteristics.

Table 113. CAUI-4/50GAUI-2/25G-AUI transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential peak-to-peak output voltage	$V_{TX-DIFF}$			1200.0	mV
Differential peak-to-peak output voltage transmitter disabled	$V_{TX-DIS-\ DIFF}$	0.0	-	30.0	mV
DC common mode voltage	V_{CM}	0.0	-	1.9	V
Output waveform steady state voltage	V_f	0.4	-	0.6	V
Output waveforem linear fit pulse peak	$V_{P(k)}$	0.71 * V_f	-	-	V
Differential resistance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω

Note:

1. For recommended operating conditions, see Recommended Operating Conditions.

This table defines the CAUI-4/50GAUI-2/25G-AUI receiver DC electrical characteristics.

Table 114. CAUI-4/50GAUI-2/25G-AUI receiver DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit
Differential resistance	$Z_{RX-DIFF-DC}$	80.0	120.0	Ω

Note:

1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.12.2 CAUI-4/50GAUI-2/25G-AUI AC timing characteristics

This table defines the CAUI-4/50GAUI-2/25G-AUI transmitter AC timing specifications.

Table 115. CAUI-4/50GAUI-2/25G-AUI transmitter AC timing specifications 1, 2

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	25.78125-100 ppm	25.78125	25.78125+100 ppm	Gb/s
AC common mode output voltage RMS	V_{CM}	-	-	0.012	V
Bounded uncorrelated jitter	T_{BUJ}			0.1	UI p-p
Even-odd jitter	T_{EOJ}	-	-	0.035	UI
Total uncorrelated jitter	T_{TUJ}	-	-	0.26	UI p-p
Signal-to-noise-and-distortion ratio	SINAD	27.0	-	-	dB

Notes:
1. See Figure 61.
2. See Figure 62.

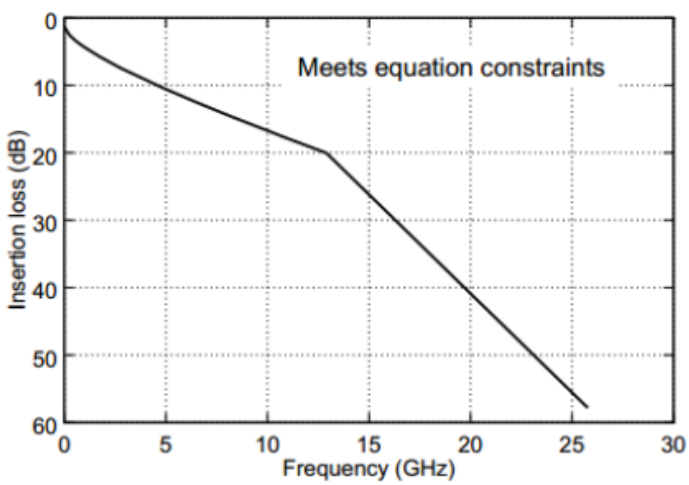
This figure shows the applied sinusoidal jitter tolerance of the CAUI-4/50GAUI-2/25G-AUI receiver.

Figure 61. CAUI-4/50GAUI-2/25G-AUI receiver applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
f < 100 kHz	Not specified
100 kHz < f ≤ 10 MHz	5 x 10^5/f
10 MHz < f < 10 LB^a	0.05

This figure provides the ISI channel loss profile.

Figure 62. CAUI-4/50GAUI-2/25G-AUI chip-to-chip channel insertion



3.23.13 USXGMII interface (USXGMII)

3.23.13.1 USXGMII DC electrical characteristics

This table defines the 10G-SXGMII transmitter DC electrical characteristics.

Table 116. 10G-SXGMII transmitter DC electrical characteristics (SD_OVDD = 1.8V) 1

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω

Note:
1. For recommended operating conditions, see Recommended Operating Conditions.

This table defines the 10G-SXGMIIreceiver DC electrical characteristics.

Table 117. 10G-SXGMII receiver DC electrical characteristics (SD_SVDD = 0.9V) 1

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	1200.0	mV
Differential resistance	R_{RD}	80.0	120.0	Ω

Note:
1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.13.2 USXGMII AC timing characteristics

This table defines the 10G-SXGMIItransmitter AC timing specifications. RefClk jitter is not included.

Table 118. 10G-SXGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ}/T_{RJ}	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.3	UI p-p

This table defines the 10G-SXGMIIreceiver AC timing specifications. RefClk jitter is not included.

Table 119. 10G-SXGMII receiver AC timing specifications 3

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Total jitter	T_J	-	-	1.0	UI p-p	1, 2
Random jitter	R_J	-	-	0.13	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1

Notes:
1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max, where ISI is jitter due to frequency dependent loss.
3. TX equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

3.23.14 XLAUI interface (XLAUI)

The XLAUI standard achieves 40 Gbps with four 10.3125 Gbps lanes.

3.23.14.1 XLAUI DC electrical characteristics

This table defines the XLAUI transmitter DC electrical characteristics. The parameters are specified at the transmitter compliance point per IEEE Std 802.3-2015.

Table 120. XLAUI transmitter DC electrical characteristics (SD_OVDD = 1.8V)1

Parameter	Symbol	Min	Typ	Max	Unit
Differential peak-to-peak output voltage	$V_{TX-DIFF}$			760.0	mV p- p
De-emphasis		4.4	-	7.0	dB
Differential resistance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω

Note:
1. For recommended operating conditions, see Recommended Operating Conditions.

This table defines the XLAUI receiver DC electrical characteristics. The parameters are specified per IEEE 802.3-2015.

Table 121. XLAUI receiver DC electrical characteristics (SD_SV_{DD} = 0.9V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential input voltage	V_{IN}	85.0		850.0	mV p- p
Differential receive input impedance	V_{IN}	80.0	100.0	120.0	Ohm

Note:

1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.14.2 XLAUI AC timing characteristics

This table defines the XLAUItransmitter AC timing specifications.The parameters are specified per IEEE 802.3-2015. The AC timing specifications do not include RefClk jitter.

Table 122. XLAUI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Deterministic jitter eye mask (far end)	J_D			0.17	UI p-p
Total jitter eye mask (far end)	J_T	-	-	0.32	UI p-p
Transmitter baud rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s

This table defines the XLAUIreceiver AC timing specifications.The parameters are specified per IEEE 802.3-2015. The AC timing specifications do not include RefClk jitter.

Table 123. XLAUI receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Input AC common-mode voltage tolerance		20.0	-	-	RMS
Deterministic jitter tolerance	J_D	0.42			UI p-p
Total jitter tolerance	J_T	0.62	-		UI p-p
Bit error ratio	BER	-	10^{-12}	-	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s

3.23.15 SerDes Recovered Clock Outputs

The RCLK[0:1] pins provide the recovered clocks from SerDes lanes running Ethernet protocols (SGMII 1G, XFI, USXGMII, CAUI-4, 50GAUI-2, 25G-AUI, and XLAUI) on SerDes 1 and SerDes 2.

3.23.15.1 SerDes 1 and 2 receive recovered clocks DC electrical characteristics

This table provides the DC electrical characteristics for the recovered clock output.

Table 124. RCLK DC electrical characteristics (OVDD = 1.8V) 1

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	2
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	2

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The symbol OVDD represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

3.23.15.2 SerDes 1 and 2 receive recovered clocks AC timing characteristics

This table provides the AC electrical characteristics of the recovered clock output.

Table 125. RCLK AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RCLK frequency	f_{RCLK}	0.0	-	161.1328125	MHz	-
RCLK pulse width	t_{RCLKPW}	40.0	50.0	60.0	%	-
LP filter < 1 MHz RCLK peak-to-peak jitter	TJ_{pk-pk}	-	-	30	ps	1
	DJ_{pk-pk}	-	-	10	ps	

Note:

1. Values listed for RCLK peak-to-peak jitter represent the jitter generation limits without any input data jitter or input PLL reference clock jitter. It is recommended that system designers use RCLK with an external jitter cleaning PLL when intending to use RCLK as a reference clock for the system. Jitter calculations for such a system should include the quoted RCLK peak-to-peak jitter, the system's SerDes PLL reference clock jitter, and the system's receiver input data jitter. Determination of both the SerDes PLL reference clock peak-to-peak jitter and the receiver peak-to-peak input data jitter should include the use of a low pass filter with a bandwidth of 1 MHz with a roll off of at least 20 dB per decade.

4 HARDWARE DESIGN CONSIDERATIONS

4.1 Clock ranges

This table provides the clocking specifications for the processor core, coherency domain, platform, memory, and DCE.

Table 126. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1800 MHz		2000 MHz		2200 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	700	1800	700	2000	700	2200	MHz	
Core frequency	175	1800	175	2000	175	2200	MHz	1
Coherency Domain frequency	1000	1300	1000	1400	1000	1500	MHz	
Platform clock frequency	500	650	500	700	500	750	MHz	1
Memory bus clock frequency	650	1300	650	1450	650	1600	MHz	1, 2
Decompression/compression acceleration engine (DCE) frequency	300	400	300	450	300	450	MHz	

Notes:

1. **Caution:** The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR4 data rate.

4.2 Platform clock requirements for Ethernet

This table shows the minimum platform clock frequency required to run Ethernet at different speeds.

Table 127. Platform clocking restrictions

Ethernet Speed	Platform clock requirement
10G	516 MHz
25G	645 MHz
40G	261 MHz
50G	350 MHz
100G	652 MHz

4.3 Power supply design

For additional details on the power supply design, see the applicable chip design checklist.

4.3.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip.

Note:

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating VDD at boot of 0.850 V. It is highly recommended to select a regulator with a Vout range of at least 0.7 V to 0.9 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

The table below lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 128. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000	default (0.850 V)
00010	0.775 V
10000	0.800 V
10010	0.825 V
10100	0.850 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 THERMAL

This table shows the thermal rating for the chip.

Table 129. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to case thermal resistance		$R_{\Theta JC}$	0.15	°C/W	1

Note:

1. Junction-to-Case thermal resistance is determined using an isothermal cold plate heat extraction through the top side of the package. Case temperature is the surface temperature at the package lid's geometric centre.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Teledyne e2v sales office.

5.2 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature by using an external temperature monitoring device (such as NXP SA56004x).

The following are the specifications of the chip's on-board temperature diodes: Operating range: 14 - 240 µA

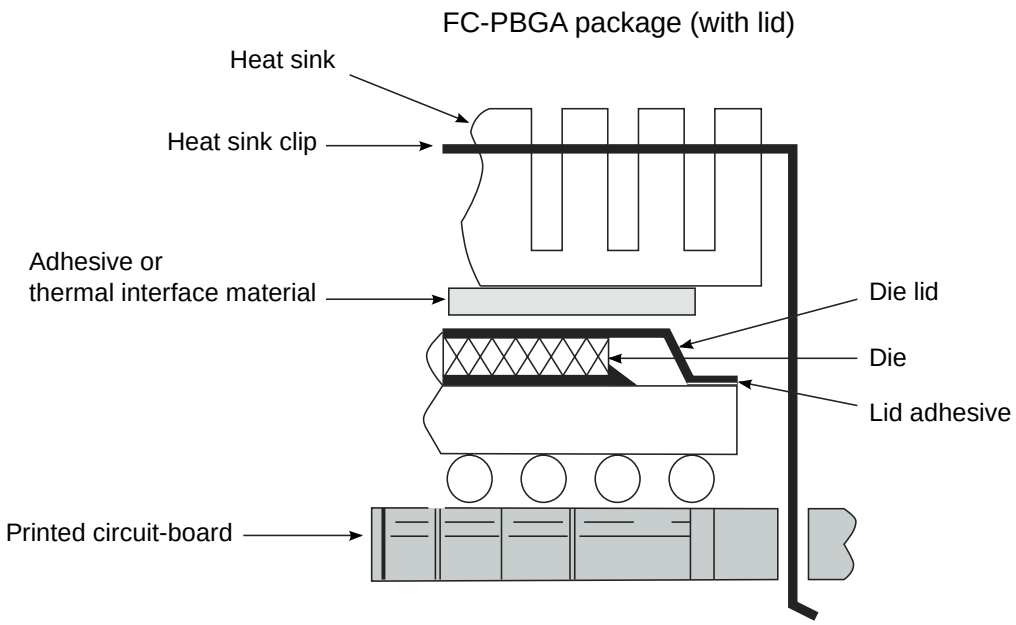
The ideality factor over temperature range 85Cº to 105Cº, n = 1.022 ± 0.003, with approximate error +/- 1.5 Cº and approximate error under +/- 3 Cº for temperature range 0 Cº to 85Cº and 105 Cº to 125Cº.

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 63. The heat sink should be attached to the printed-circuit board with the spring force centered over the lid. This spring force should not exceed 47 pounds force (209 Newton).

Figure 63. Package exploded, cross-sectional view-FC-PBGA (w/ Lid)



The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 63).

The system board designer can choose among several types of commercially available thermal interface materials.

6 PACKAGE INFORMATION

6.1 Package parameters for the FC-PBGA

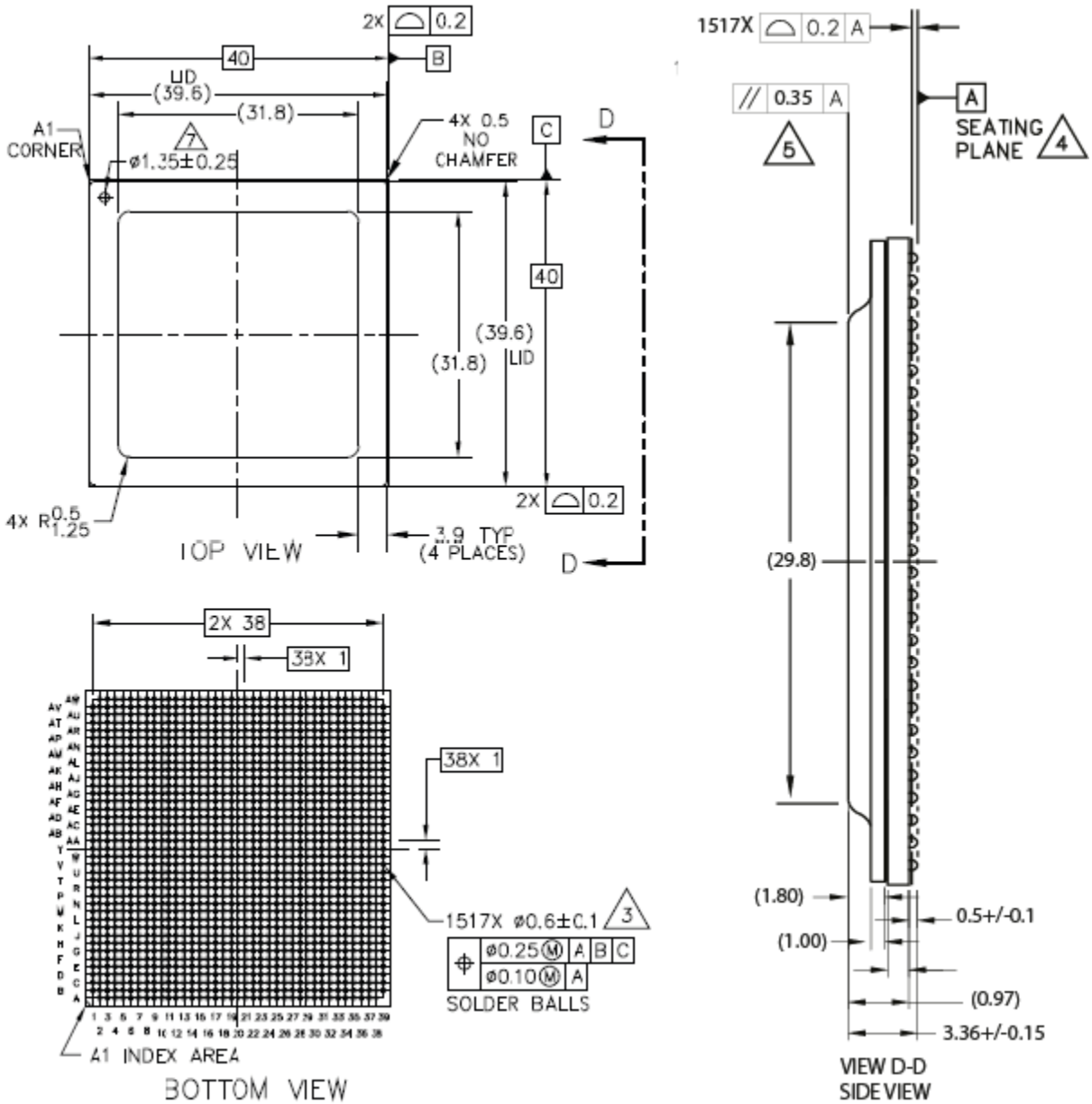
The package parameters are as provided in the following list.

- Package: #I/O 1517, 40 mm x 40 mm, lidded FCBGA
- Substrate: #3-2-3, stack up, 600µm core thickness
- Pitch: 1 mm
- Ball Diameter (typical): 0.6 mm
- Solder Balls: 96.5% Sn, 3% Ag, 0.5% Cu
- Solder Balls: 63% Sn, 37% Pb
- Module height: 3.21 mm (minimum), 3.36 mm (typical), 3.51 mm (maximum)
- Case outline number: 98ASA01023D

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Figure 64. Mechanical dimensions of the FC-PBGA



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A. Raw ball diameter is 0.6mm
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. Deleted in Rev B
9. Lid overhang on the substrate is not allowed

7 SECURITY FUSE PROCESSOR

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture featurs is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 10. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Recommended Operating Conditions.

Note:

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 ORDERING INFORMATION

Contact your local Teledyne e2v sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

This table provides the Teledyne e2v Layerscape platform part numbering nomenclature.

Table 130. Part numbering nomenclature

Family	Performance Level	Number of cores	Derivatives	Temperature range	Options	Package Type	CPU Frequency, DDR Data Rate	Revision
LX(X)[2] = 16FFC	2	08 = 8 12 = 12 16 = 16	0 = first	A = -40/105 F = -40/125 M = -55/125	C = SEC, CANFD enabled E = SEC enabled, CAN 2.0b enabled (no CAN-FD support) N = SEC disabled, CAN 2.0b enabled (no CAN-FD support)	7 = 40x40mm FC PBGA pb-free C4/C5 3 = 40x40mm FC PBGA C4 = pb-free, C5 = SnPb (63/37)	1826 = 1800 MHz, 2600 MT/s 2029 = 2000MHz, 2900 MT/s 2232 = 2200 MHz, 3200 MT/s	B = Rev 2.0

Notes:

1. For availability of the different versions, contact your local Teledyne e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a LXX part number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

9 REVISION HISTORY

This table summarizes revisions to this document.

Issue	Date	Comments
DS 60S 222625(A)	11/22	Initial revision
DS 60S 222625(B)	03/23	Added an additional line in Section 6.1.

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