PRODUCT BRIEF - Preliminary

1 MAIN FEATURES

- Quad channel 12-bit 1.6 GSps ADC.
- 1 Vpp 100Ω differential DC/AC coupled input voltage
- 100Ω Differential input AC coupled clock
- Cross-point switch enabling 1, 2 or 4 channel mode at 6.4 GSps/3.2 GSps/1.6 GSps
- 4.5/ >6GHz selectable analog input bandwidth (-3dB)
- Low Latency ESIstream serial link at 12.8 Gbps
- Power supply: 3.3V (analog), 2.5V (I/O), 1.2V (digital), optional 1.8V (SPI)
- Power consumption 6.6W (Typical)
- SPI digital interface (gain, offset, sampling delay adjust, test modes)
- 2 manufacturing calibration sets for interleaving (through IN0 input)
- ADC Gain, Offset, Sampling delay adjustment for user's interleaving calibration
- Clock and SYNC chaining
- Package: CBGA323 (HiTCE) 16x16mm pitch 0.80mm : RoHS
- Temperature range: Tc -40°C / Tj +110°C

2 PERFORMANCE

Typical performance (Ambient temperature, nominal power supply)

Performance @1.6GSPS (4 channel-mode)	**Performance @6.4GSPS (1 channel-mode)**
SFDR (Spurious Free Dynamic Range) - Fin = 100MHz : 71.0 dBFS - Fin = 740MHz : 64.7 dBFS - Fin = 1480MHz : 60.1 dBFS - Fin = 2980MHz : 56.4 dBFS - Fin = 5980MHz : 37.1 dBFS **SNR** (Signal to Noise Ratio) - Fin = 100MHz : 54.2 dBFS - Fin = 740MHz : 53.8 dBFS - Fin = 1480MHz : 52.9 dBFS - Fin = 2980MHz : 49.6 dBFS - Fin = 5980MHz : 45.5 dBFS	**SFDR** (Spurious Free Dynamic Range) - Fin = 100MHz : 54.8 dBFS - Fin = 1480MHz : 58.6 dBFS - Fin = 2230MHz : 61.9 dBFS - Fin = 2980MHz : 55.0 dBFS - Fin = 5980MHz : 37.1 dBFS **SNR** (Signal to Noise Ratio) - Fin = 100MHz : 54.1 dBFS - Fin = 1480MHz : 52.8 dBFS - Fin = 2230MHz : 50.6 dBFS - Fin = 2980MHz : 49.5 dBFS - Fin = 5980MHz : 45.5 dBFS

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ENOB (Effective Number Of Bits) - Fin = 100MHz : 8.7 bitFS - Fin = 740MHz : 8.6 bitFS - Fin = 1480MHz : 8.3 bitFS - Fin = 2980MHz : 7.8 bitFS - Fin = 5980MHz : 5.6 bitFS **NPR (Noise Power Ratio)** at -12dB Loading Factor (80% Nyquist = 600MHz) 1st Nyquist : NPR = 44.9dB 2nd Nyquist : NPR = 40.6dB 3rd Nyquist : NPR = 39.9dB	**ENOB** (Effective Number Of Bits) - Fin = 100MHz : 7.9 bitFS - Fin = 1480MHz :8.1 bitFS - Fin = 2230MHz : 7.9 bitFS - Fin = 2980MHz :7.5 bitFS - Fin = 5980MHz : 5.1 bitFS

3 APPLICATIONS

Automatic Test Equipment
High-speed Data Acquisition
Oscilloscopes
Phased-Array RADAR Receivers
Wideband Satellite Receivers
Point-to-Point Microwave Receivers
LIDAR (LIght Detection And Ranging)
Direct RF data conversion
High Energy Physics

4 DESCRIPTION

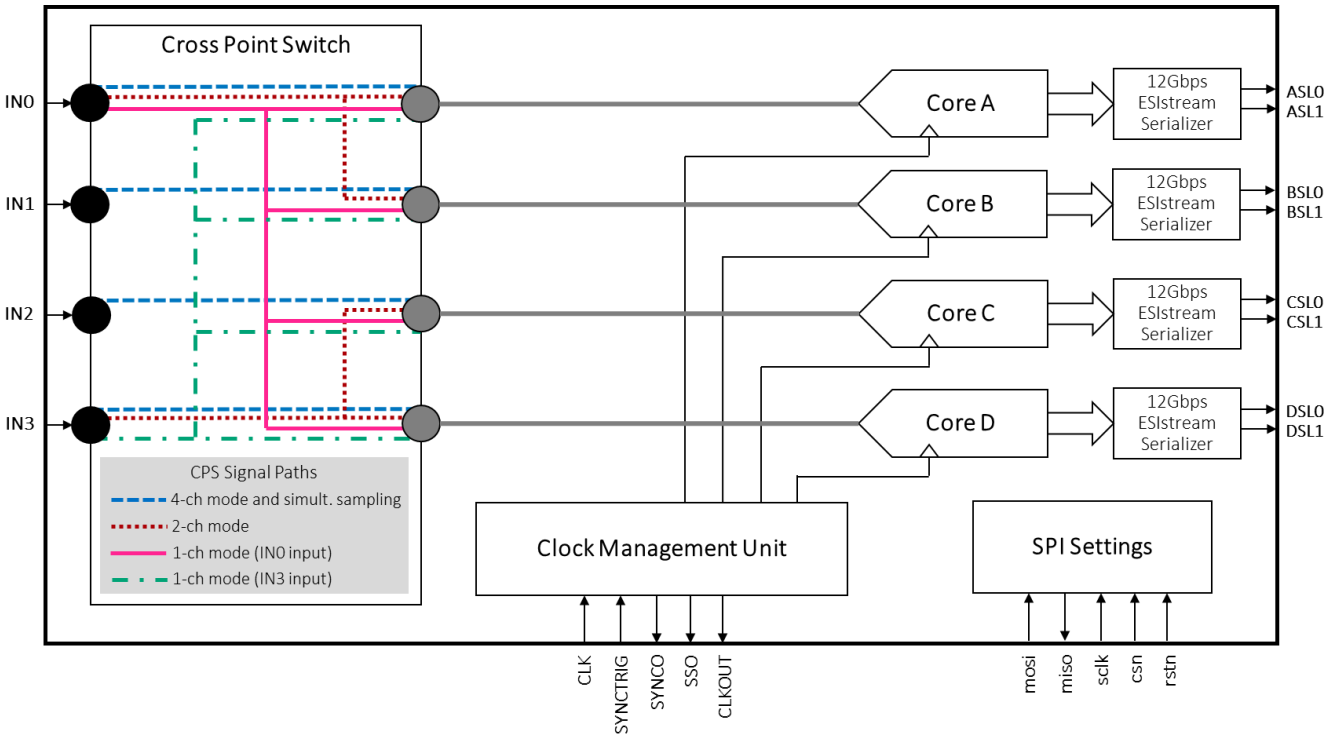

Figure 1 – Simplified block diagram

EV12AQ605 is a quad 12 bit 1.6GSps ADC featuring a built in cross-point switch (controlled thru the SPI) allowing 1, 2 or 4 channel digitizing at respectively 6.4 GSps, 3.2 GSps or 1.6 GSps sampling rate.

The four ADC cores can operate in phase or interleaved (option controlled thru the SPI). External clock must be provided at four times the individual sampling rate.

The architecture uses four high sampling rate single cores (up to 1.6GSps) without interleaving thus providing high level of spectral purity.

Data is output on a short latency serial link at up to 12.8 Gbps, using ESIstream protocol.

ADC synchronization is achieved through SYNC input pin. Multiple ADC synchronization is simplified thanks to ability of SYNC chaining through SYNCO output.

Digital CMOS inputs levels can be configured in 1.8V, 2.5V or 3.3V logic compatibility.

Functionalities controlled thru the SPI include:

- Clocking modes: 4 ADC cores sampling simultaneously, 2 ADC cores sampling simultaneously in opposition with 2 others, 4 ADC cores interleaved.
- Clocking features: enable/disable CLKOUT, SSO and SYNCO outputs (in order to save power if these features are not needed).
- Inputs selection: 4 ADC cores interleaved and driven by the same input IN0 (or IN3), 2 ADC cores driven simultaneously by IN0 and IN3, 4 ADCs core driven simultaneously by IN0, IN1, IN2 and IN3.
- Analog input bandwidth: 4.5GHz (nominal) or >6GHz (extended)
- 2 manufacturing calibration sets selection for interleaved mode (IN0). Custom interleaved mode calibration through Offset/Gain/Phase adjustment
- Swing Adjust: Output swing of both serial links and timer CML or LVDS buffers is reduced by 30% for power dissipation reduction purpose.
- Output buffer impedance adjust (trim by a range of 20%) to improve transmission
- 12.8 Gbps Serial link polarity can be inverted

5 PIN DESCRIPTION

5.1 Type / Outline

HiTCE Ceramic Ball Grid Array CBGA323

- High TCE Glass-Ceramic substrate
- Body size: 16.0x16.0 mm
- Lands Pitch: 0.80mm
- Number of balls: 323
- Conductor: cofired copper

Package interconnection

- 18x18 BGA matrix (323 balls, A1 removed)
- 0.80 mm ball pitch
- Ball type : SAC305
- MSL3 (non-hermetic)

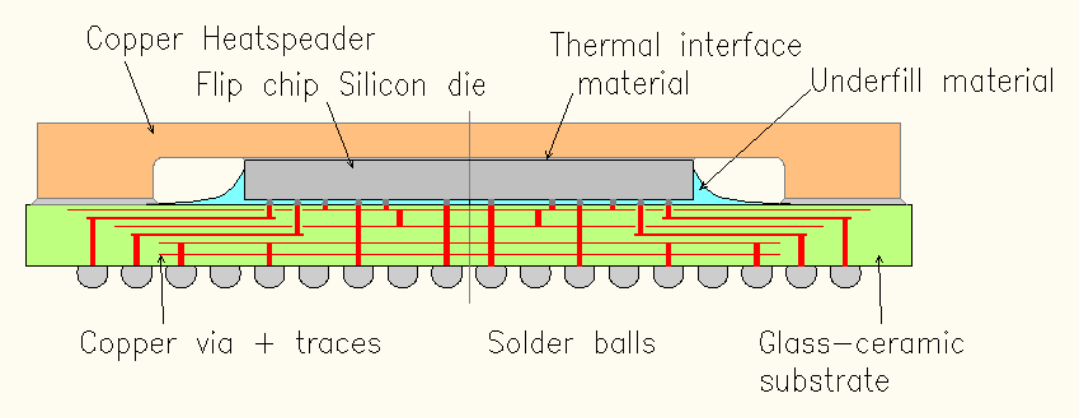

Figure 2 – Package cross-section

5.2 Pinout top-view

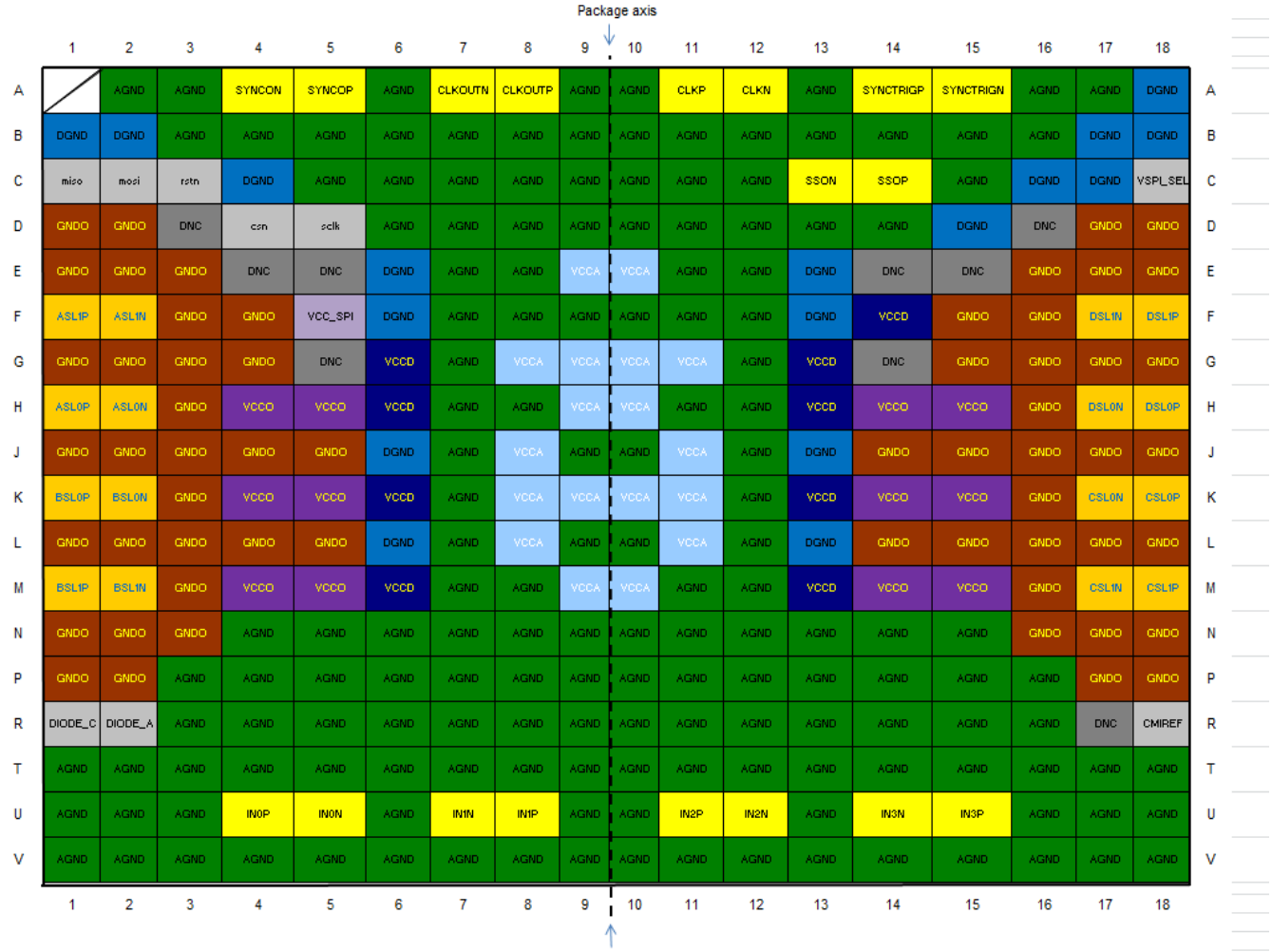

Figure 3 - Pinout

5.3 Package drawing

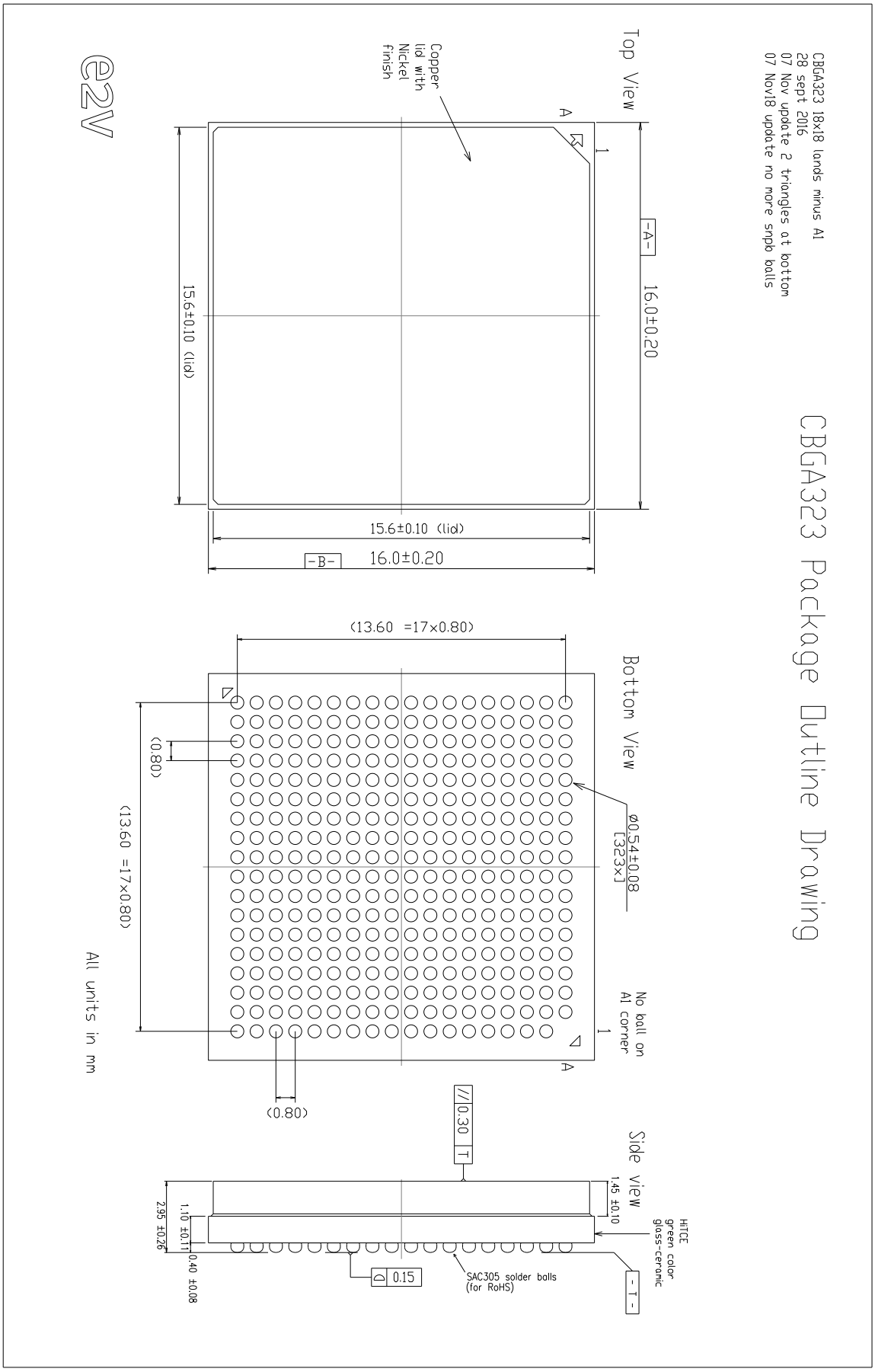

Figure 4 – Package outline for SAC305 balls

6 ORDERING INFORMATIONS

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EVP12AQ605SH	Ambient	Prototype	RoHS	Beta sampling

7 REVISION HISTORY

Issue	Date	Comments
A	19/11/2018	Creation

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