WHITE PAPER

Designing a Space qualified, edge computing board, based on a Quad ARM Cortex A72 processing module with built-in DDR4 memory

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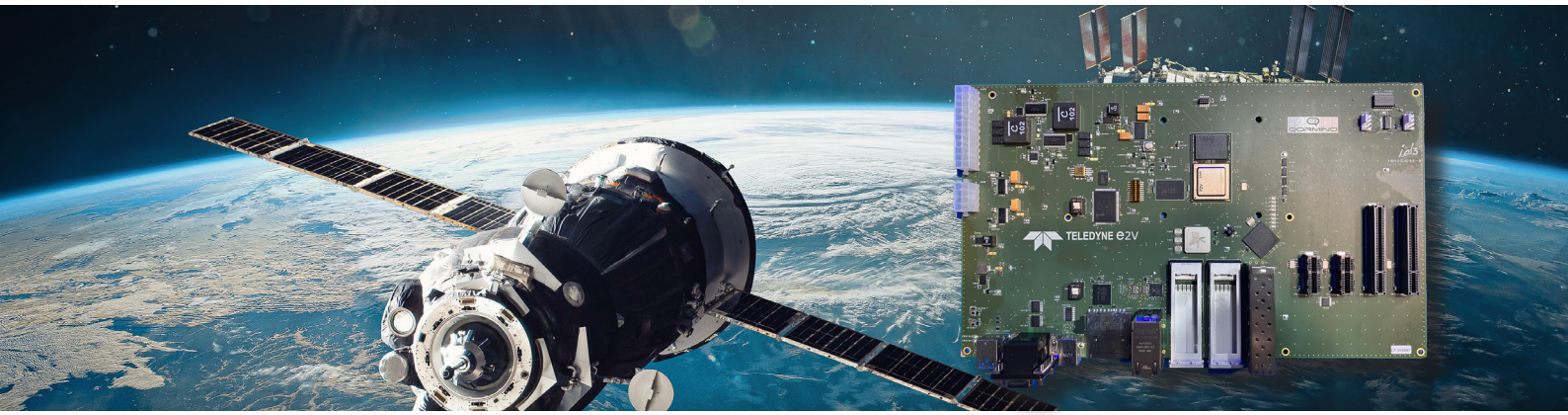
ABSTRACT

From concept to Space qualified electronic board... This paper highlights some of the key points requiring particular attention to succeed during the design process of a Space grade digital processing board: main components choice, PCB requirements, critical simulations, metrics, and milestones.... A Teledyne e2v reference design board, based on Radiation Tolerant components, provides an example for this story telling.



THE REFERENCE DESIGN, COMPANION ON THE WAY FROM IDEA TO SPACE...

Design steps usually required for the development of an electronic equipment are also applicable to Space systems (components selection, schematics, simulations, components arrangement on board, routing, DFT...) and the same design targets are pursued: Time To Market, Return On Investment, ... specification compliance, long term procurement.

Nevertheless, during this process, because of harsh conditions in a Space environment, particular attention must be paid to specific requirements such as complex cooling conditions, limited power amount, autonomous and highly reliable operation exigence, fast recovering or repowering, Radiations performance.
Teledyne e2v Space Radiation Tolerant digital processing solutions offer disruptive computing capabilities.
Latest generations are based on ARM® Cortex®-A72 and high speed DDR4, making them compliant with a broad range of Space use cases, such as, among so many others: Real-time image or video processing & compression, SatComs, Navigation, Scientific data analysis, Autonomous operations, including robotics, landing..., AI, including innovative, adaptive, frugal and efficient algorithms, Avionics space systems, Data Science, Lunar gateways, Autonomous operations, ...

This paper presents and highlights successively:

- The Purpose and architecture of an edge computing system / board
- Teledyne e2v Qormino® QLS1046-Space processing module, a combo with a Quad Core ARM Cortex A72 associated with high speed DDR4
- Teledyne e2v QLS1046-Space reference design:
  - Design strategy/process and goals
  - High speed communication interfaces
  - Supports functions as NAND and NOR FLASH memories, cadencing clocks, Supervisor...
  - Power supplies and power on sequence
  - PCB, layout and stacking

GENERAL ARCHITECTURE OF AN EDGE PROCESSING BOARD

EDGE COMPUTING ON BOARD CHALLENGES

For Space applications, constant increasing edge computing capabilities today allow to process always bigger amounts of data, delivered with always higher data rate. increasing memories sizes allow that calculation results, may eventually be compressed, then, stored on board, prior to their transmission to ground stations. Typical application examples are Earth observation, early warnings, automated docking or landing, debris avoidance, mobiles tracking, orbital or floor communication gateways. This type of architecture deals with Data streams issued from different sources such as sophisticated sensors, high speed links... All these capabilities must be implemented with the highest reliability grade due to the Space environment.

TYPICAL EDGE COMPUTING BOARD ARCHITECTURE

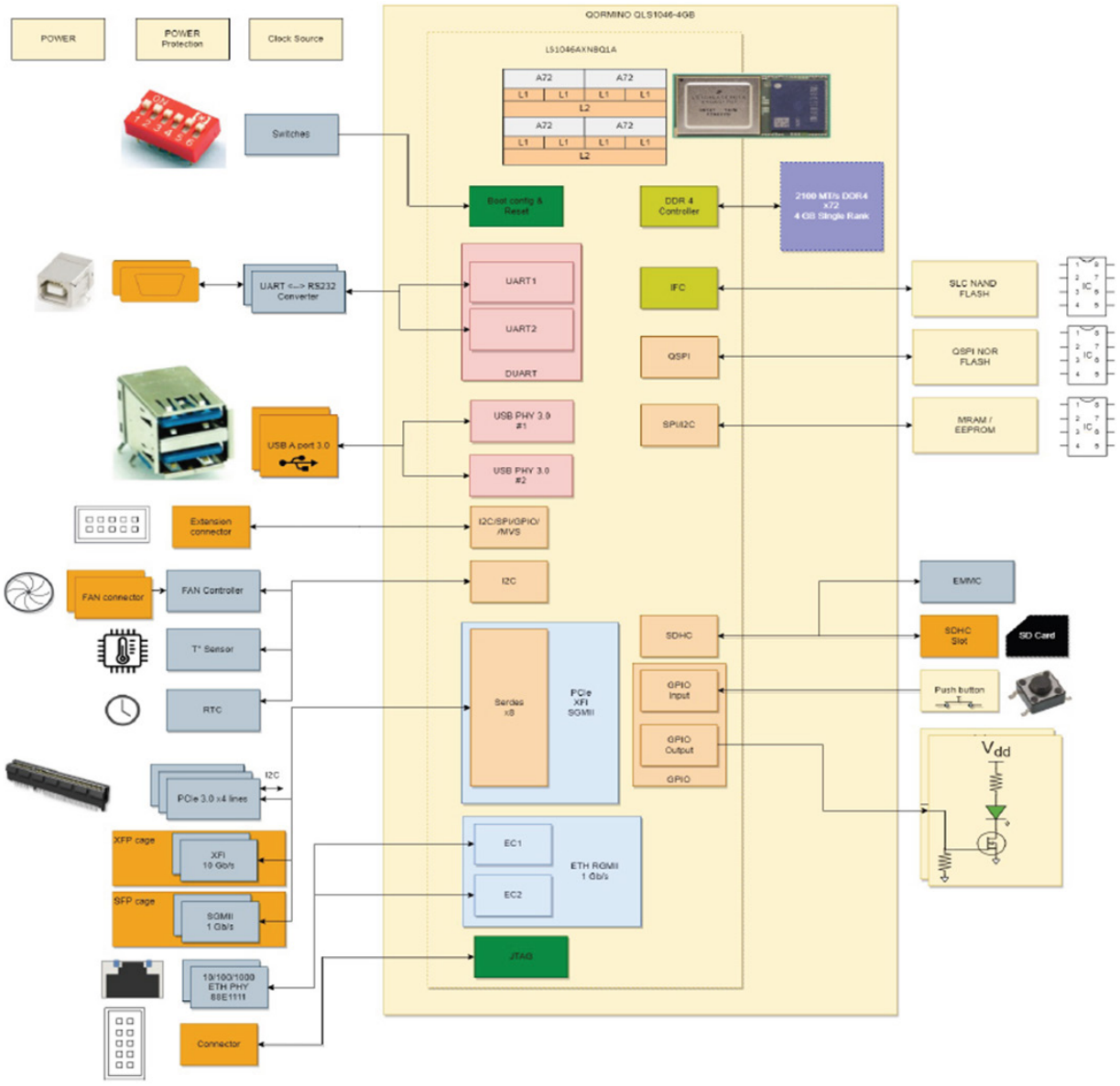


Figure 1: Evaluation board architecture

The edge computing architecture is built around the processing device, which performs calculation and data treatment. This type of feature can either be microprocessor, FPGA, ACAP, ASIC, or even a combination of several types.

Whatever it is, its performances and characteristics determine the board's size and performances.

Most of the time, this component requires a big amount of volatile (mainly DDRAM) or persistent memory (NAND and NOR FLASH, or possibly MRAM). All these key components must be qualified for radiations, complying with mission duration, conditions, and cruciality.

These devices are Radiation Tolerant and based on recent technology nodes to offer high performance. They must be paired with external high-density and high-speed volatile memory to buffer data, typically DDR, especially when image processing is involved. The architecture features several fast interfaces, supporting different protocols, to handle the incoming raw data, and to generate the outcoming processed information.

To operate the board, non-volatile memory is used to store the software application, the operating system, or the programmable logic configuration. Several clocks are also required to operate the processing device, as well as a supervisor acting in a watchdog role. Also, special power supply scheme is needed to deliver the high currents and low voltages associated to the recent technology nodes.

QLS1046-SPACE PROCESSING MODULE - DESCRIPTION

The edge computing architecture is based on a Teledyne e2v QLS1046-Space processing module. QLS1046-Space is a Space qualified, Radiation Tolerant, Compute Intensive integrated solution. In a small form factor of 44 x 26mm, it embeds a Space grade processor and Space grade DDR4 memory. The processor is a Quad ARM Cortex-A72 (LS1046) running at up to 1.8GHz and bringing 30k DMIPS / 56 GFLOPs computing capabilities, with integrated packet processing acceleration, high speed peripherals including 1/10 Gb Ethernet, PCIe® Gen3. The DDR4 memory has a 4GB density and is connected to the processor, offering rates up to 2100MT/s (130Gbps).

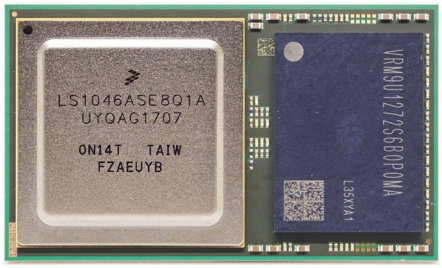


Figure 2: Qormino QLS1046-Space

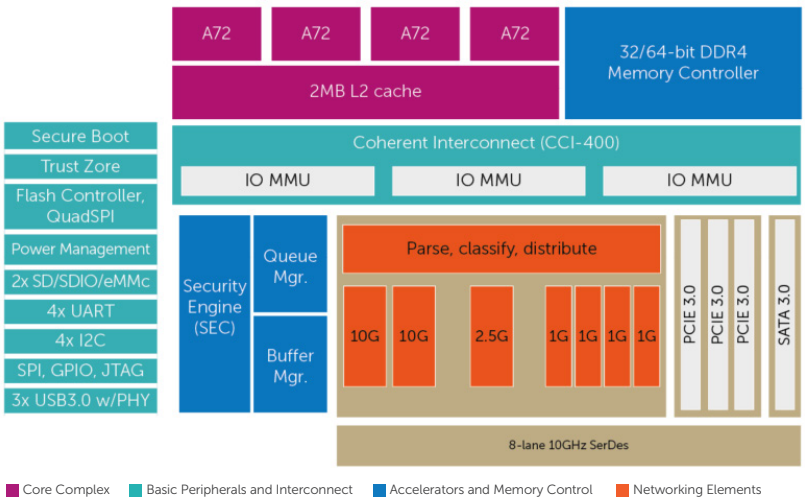


Figure 3: QLS1046-Space high level diagram

QLS1046-Space complies with NASA Level 1 (based on NASA EEE-INST-002 - Section M4 – PEMs) and ECSS Class 1 (ECSS-Q-ST-60-13C). In terms of radiation tolerance, it has a SEL LET threshold above 62.5 MeV.cm^2/mg, and can sustain a TID of 100 krad(Si) allowing it to comply to significant mission conditions. SEU and SEFI cross-sections are also available in dedicated radiation reports.

QLS1046-Space is a computing module that can be used for many applications requiring compute intensive capabilities in Space.

It especially fits with Space systems embedding AI algorithms. It already demonstrated its ability to run adapt deep learning AI algorithms parameters, for image processing on board, for example. It brings all the technical benefits of pre-processing information, reducing on-board storage capability requirement, budget, and bandwidth for the downlink to ground stations.

QLS1046-Space is particularly interesting to reduce Time To Market, risks, system size, bill of material...
It avoids dealing with complex implementation required between the processor and memory (64 data bus, 8 ECC, control signals...). : their impedance characteristics must indeed be perfectly simulated, warranted, and controlled, which can be a tricky challenge. This point requires special characteristics for the PCB stack up and will potentially result in a more expensive one, eventually just to comply with this only feature.

REFERENCE DESIGN ROADMAP & FEATURES

DESIGN METHODOLOGY

The following methodology has been followed to implement QLS1046-Space reference design. First, selecting the functional features and interfaces to be available at reference design level, to serve Space use cases, and/or development/debug functions. Second, listing critical functions such as power supplies, clocks, memories, and supervisor. Finally, mapping as much as possible the selected functions were populated with components having Space versions.

When possible, on the reference design, the equivalent industrial grade of the selected Space components was installed. If only space version of the component is available, EMs (Engineering Models) are selected. When possible, the maximum of components of the same manufacturer were chosen to facilitate procurement.

Here are the main functions of QLS1046-Space Reference Design:

- Interfaces (RGMII, SGMII, PCIe) for high-speed communications
- Non-volatile memories (NOR, NAND flash) to boot, execute the program and store data.
- Power supplies and power sequencing,
- Clocks (oscillators) for the processor and the different interfaces present on the board,
- GPIO and low-speed interfaces for various purposes,

Particular attention has been paid on Space grade status and radiation tolerance (TID, SEL). All others usual topics were checked (Sustainability, Technical Features: voltage, power consumption, interfaces, speed, size, weight...) were obviously considered. On top of the Space-compliant functions, some additional functions have been also implemented on the reference design for development purposes and ground usage: XFI (10Gb/s) Ethernet, SD card and eMMC, MRAM, serial communication (USB, UART), temperature measurement, fan controller... For Ethernet links, the module can handle several protocols, among which RGMII, SGMII, and XFI are relevant for Space applications to offer 1Gbps and 10Gbps connections. These protocols require external PHY devices to interface with the physical layer.

HIGH-SPEED COMMUNICATIONS LINKS INTERFACES

QLS1046-Space supports different types of high-speed interfaces, such as Ethernet, PCIe, SATA... On the Space reference design, Ethernet and PCIe interfaces have been implemented as commonly used in Space applications:

- For the PCIe (fig10) implementation, no specific interface component is required.

Concerning RGMII, **MICROCHIP VSC8541XMV**[1] was selected as it is largely proven for Space systems. This PHY manages Ethernet connection up to 1Gbps. It offers high level of radiation immunity (TID of 100 krad (Si) and SEL > 78 MeV.cm^2/mg). An industrial version, pin-to-pin compliant allows to realize ground design at lower cost. VQFN68 package if well proven for assembly during manufacturing process.

On the reference design board, two RGMII devices and two RJ45 connectors are used since the QLS1046-Space can manage two RGMII interfaces.

Regarding SGMII links, **MICROCHIP VSC8574XKS**[2] was selected for almost the same reasons than the RGMII PHY. It presents the same levels for radiations immunity. This PHY can manage up to four interfaces at 1Gbps. On the reference design, it is interfaced with the SerDes of the QLS1046-Space, to offer two SFP connections:

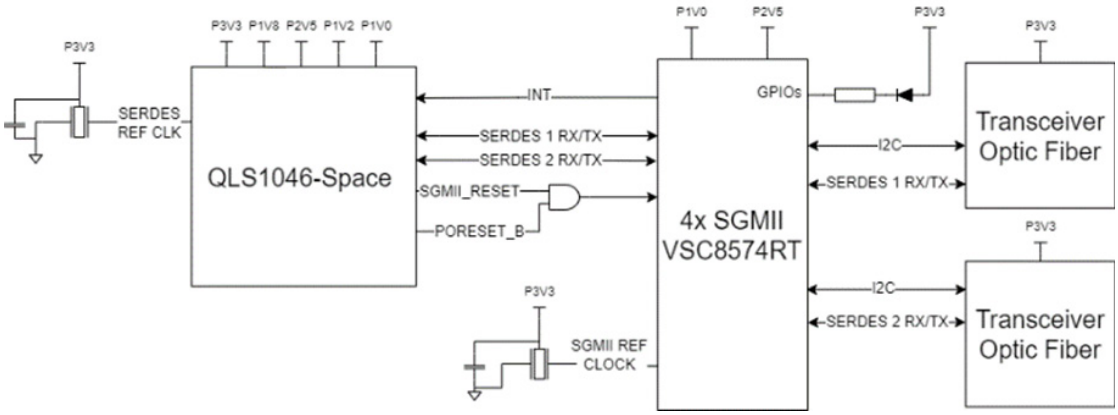


Figure 4: VSC8574RT SGMII block diagram implementation

Two XFI links are also available on the reference design to support 10Gbps data rates for development purposes and future needs. The implementation is based on a commercial grade **MICROCHIP VSC8254YMR PHY**, which is not available today as Radiation Tolerant, unlike the other PHYs.

HIGH-SPEED COMMUNICATIONS LINKS INTERFACES

Considering non-volatile memories, 3 components were implemented on the reference board. They are used for boot sequence, OS and application storing. Boot can be issued from different types of persistent memories such as SD Card / eMMC, parallel or QSPI NOR FLASH.

Space grade SD Card or eMMC are not still available.

INFINEON CYRS17B512 NOR FLASH was chosen for booting. Its compliance with QSPI interface allows to reduce the number of relevant tracks. Its size, 64MB, is enough to store the initial bootloader. It can accept 1.8V on I/Os, allowing to interface directly with the QLS1046-Space. It operates up to 133MHz, which is higher than the maximum QSPI frequency for QLS1046 (62,5MHz). It also presents a high level of radiation performance, TID of 300krad (Si) and SEL immunity higher than 60 MeV.cm^2/mg.

1. *Radiation-Tolerant Single Port Gigabit Ethernet Copper PHY with GMII/RGMII/MII/RMII Interfaces*
2. *Quad-Port 10/100/1000BASE-T PHY with Synchronous Ethernet, IEEE 1588, and QSGMII/SGMII MAC*

DDC 69F64G16 NAND FLASH was also implemented to store OS, Root Files System, application, and data. 32Gbit up to 256Gbit sizes are available. 64Gbit, 16-bit parallel interface that can be configured as 2 memories of 4GByte 8-bit parallel interface was selected. The proprietary RAD-PAK® package can afford TID of 100krad (Si) sufficient for many missions. Timings are compliant with the QLS1046-Space, and interface signals can be connected directly to the flash controller thanks to the 1.8V capability.

An MRAM from **EVERSPIN TECHNOLOGIES EM128LX** was also implemented. It supports the Expanded SPI (xSPI) standard protocol and can reach a capacity of 128 Mb. Implementing merging code and critical data (stack pointer, data registers) on the same device may be considered.

CLOCKS

For QLS1046-Space, the clock needed are mainly 100MHz, 125MHz and 156.25MHz in LVDS level. For the PHYs, the required input clock types are CMOS, LVDS and LVPECL. The QLS1046-Space main system clock is 100MHz and can be either single-ended or differential. A differential clock is used, as the DDR clock can be derived directly from it, reducing the total number of external clocks required, hence reducing the bill of material.

For the high-speed serial interfaces of the QLS1046-Space (called "SerDes" for Serializer / Deserializer), the clock requirements depend on the selected interfaces. QLS1046-Space can handle up to 8 SerDes lanes. On the reference design, the implemented interfaces are of PCIe, SGMII, and XFI types. Two SGMII and two XFI interfaces are implemented on the SerDes module 1, with Reset Configuration Word (RCW) value of 0x1133. SGMII needs a reference clock at 125MHz on PLL1, and the XFI needs a clock reference at 156.25MHz on PLL2.

SRDS_PRTCL_S1 RCW[128-143] (in hex)	D SD1_RX0_P/N SD1_TX0_P/N	C SD1_RX1_P/N SD1_TX1_P/N	B SD1_RX2_P/N SD1_TX2_P/N	A SD1_RX3_P/N SD1_TX3_P/N	PLL mapping for all lanes/ protocols	
					When PCIe operates at Gen1/2	When PCIe operates at Gen3
1333	XFI.9	SGMII.10	SGMII.5	SGMII.6	2111	not available

Figure 5: SerDes module 1 configuration

Regarding the PCIe, two configurations will be available. First option, with the Reset Configuration Word (RCW) value of 0x8888, enables one PCIe x4 interface. Second option with the configuration word value of 0x5577, enables two PCIe x1 and one PCIe x2 interfaces. PCIe can work using a 100MHz clock, hence PLL1 and PLL2 of SerDes module 2 can both be fed with a clock reference at 100MHz.

SRDS_PRTCL_S2 RCW[144-159]	A SD2_RX0_P/N SD2_RX0_P/N	B SD2_RX1_P/N SD2_RX1_P/N	C SD2_RX2_P/N SD2_RX2_P/N	D SD2_RX3_P/N SD2_RX3_P/N	PLL mapping for all lanes/ protocols	
					When PCIe operates at Gen1/2	When PCIe operates at Gen3
8888	PCIe.1 x4				2222	2222
5577	PCIe.1 x1	PCIe.2 x1	PCIe.3 x2		2222	1111

Figure 6: SerDes module 2 configuration

For this reference design, the Q-Tech Corporation QT735 series is chosen, since it fits the operation frequency requirements is also Radiations Tolerant qualified, It is available with various output levels compliant with this reference design. Its package is a generic SMT 3.2x5mm packaging, standard for a ground POC, a SnPb termination is available if required for a Space Flight Model. Considering radiation performance, these parts can sustain a TID of 50 krad (Si) typically compliant with LEO requirements. For applications requiring higher radiation performance, other series are available from Q-Tech Corporation. Some clocks with HCSL output are also required on the PCIe connectors. No Space grade clock with such output has been identified, hence, an industrial clock is used for this reference design.

SUPERVISOR

The QLS1046-Space sustains high level of radiations, but can still exhibit SEU and SEFI events, which can cause a temporary loss of functionality. Mitigation techniques allow the device to self-recover from some of these events, but rarely and in ultimate cases, an external action may be required to recover. **RENESAS ISL706** Radiation Hardened supervisor is used as watchdog on this reference design. It will reset the system if it occurs that the QLS1046-Space stops operating properly. The supervisor also manages the reset sequence upon power-up.

POWER SUPPLIES AND BUDGET

The functional architecture of this reference design is fully defined. Thus, power consumption can be estimated. Power consumption budget is presented in the following table, according to worst-case scenario, where all devices and interfaces are operating simultaneously at their maximum capabilities.

Voltage	Current	Power	Tolerance
12,0V	2,1A	25,20W	NA
5,0V	3,3A	16,50W	NA
3,3V	4,3A	14,19W	± 165 mV
2,5V	1,4A	3,50W	± 120 mV
1,8V	1,0A	1,80W	± 90 mV
1,4V	1,2A	1,62W	± 67 mV
1,2V	4,0A	4,80W	± 60 mV
1,0V	32,5A	32,50W	± 30 mV
0,6V	1,0A	0,60W	±6 mV
Total		**100,71W**	

Table 1: Power budget

The 5V supply is the main input power supply. It is used by power converters to deliver lower required voltage rails. The 5V is also directly used on USB connectors. An extra 12V supply is only required to be delivered to any PCIe devices connected to the board.

The power supplies should be able to operate with an input voltage of 5V, and they should have "enable" and "power good" signals for chaining them to realize the proper power-up sequence. On top of these requirements, efficiency is the main driver for selecting the Space grade supplies, since power consumption and heat dissipation is a challenge is Space environment. Based on these criterions, the following Texas Instruments converters were selected to achieve the power supply scheme on the reference design:

- Texas Instruments TPS7H4003-SEP, switching, up to 18A output current,
- Texas Instruments TPS7H4010-SEP, switching, up to 6A output current,
- Texas Instruments TPS7H1111-SEP, LDO, up to 1.5A output current,
- Texas Instruments TPS7H3302-SEP, DDR4 termination regulator.

Plastic package were retained, because of their easiness for assembly. They are certified for a defined Radiation Tolerance level, TID of 20 krad (Si), and SEL immunity of 43 MeV.cm^2/mg. When facing an application requiring higher radiation performance, or higher quality level, there exist ceramic flatpack versions offering a TID of 100krad (Si) and SEL immunity of 75 MeV.cm^2/mg. An example of implementation of one of the switching regulators is shown on Fig. 7:

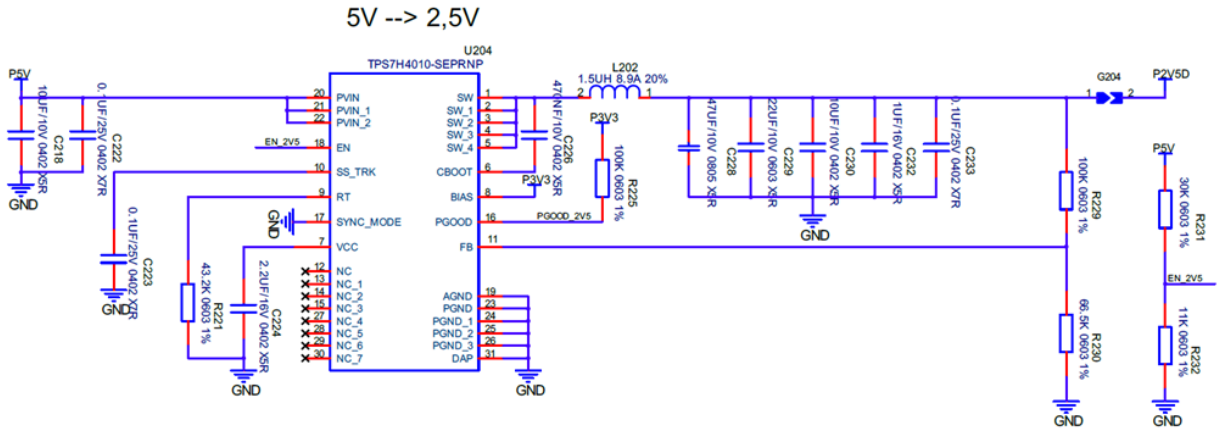


Figure 7: 2.5V supply schematics

The QLS1046-Space requires a specific power-up sequence. For this purpose, the "enable" and "power good" signals of the different converters are used. Fig. 8 illustrates the complete power supply scheme of the reference design board with the way the regulators are chained to achieve the proper sequence.

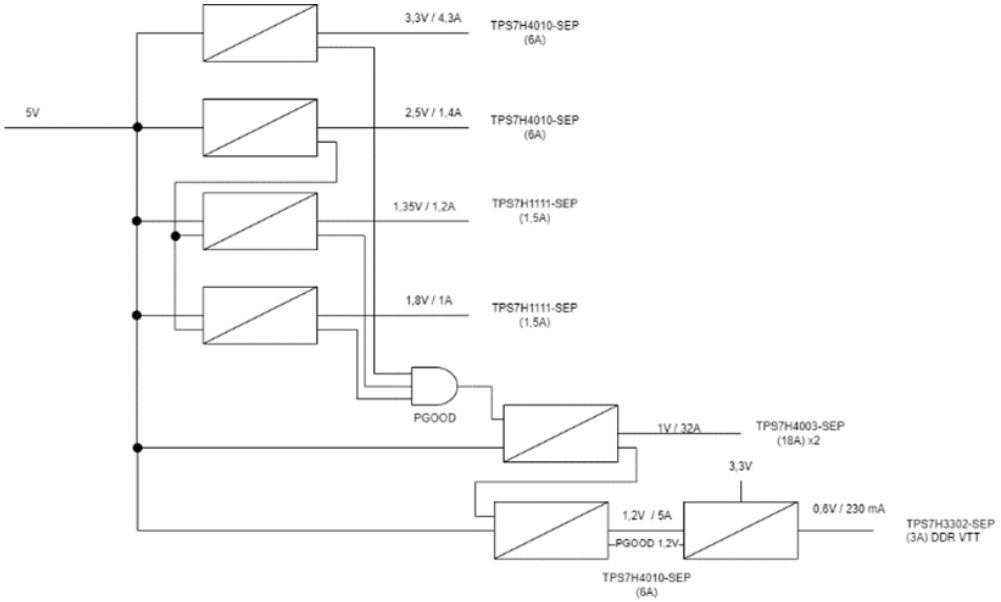


Figure 8: Complete power supply scheme

LAYOUT, PCB, STACKUP

After the full schematics of the board was achieved, classical layout development flow was performed:

- placement of components (thermal, cross talking, decoupling; tracks sizing, isolation groups sort...)
- routing
- ground planes tracing

Particular attention was paid to critical high speed communication links (RGMII, SGMII, and XFI), in terms of impedance, isolation, cross talking, decoupling, filtering.

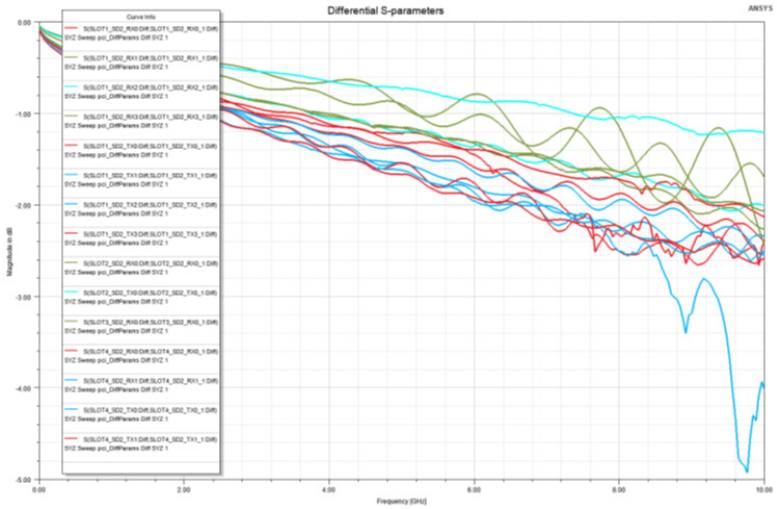
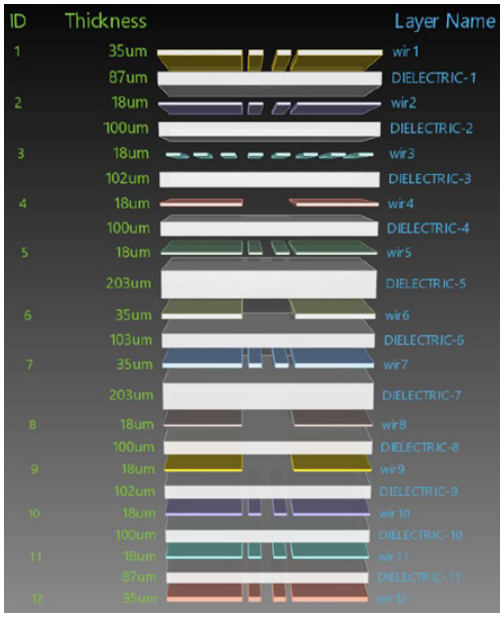


Figure 9: S-parameters model in transmission for the PCIe interface

For the power supplies, a particular attention was put on the core voltage (1V). Filtering, ability to constantly deliver high currents was particularly studied. Power integrity was checked. Power dissipation of the QLS1046 was studied. Cooling of the processor for ground usage is based on a heatsink and a small fan. Obviously, cooling in Space is more challenging, and is detailed in Teledyne e2v Application Note AN 60S 223092.

At the end, the main PCB characteristics are the following ones:



Nb of layers	12 layers
Copper thickness (external layer)	35 µm
Copper thickness (internal layer)	17 µm and 35 µm on power
Board thickness	1,6 mm
Material	MEG6
BGA	Yes min pitch 0,8mm
SMT	Yes min pitch 0,4mm
Through hole	Yes
Pressfit	No
Component's place	Top and bottom (passives only)
Via	Buried/one eyed vias
Finition	Snpb
Metallization	ENIG
PCB Color	Green
Serigraphy color	White

Figure 11: PCB characteristics

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TELEDYNE E2V SUPPORTS YOU...

The Reference Design Kit is an important part of Teledyne e2v global offer, and it has been developed to help customers achieve and success on their qualified Edge computing designs for Space.
Teledyne e2v offer includes, among all others:

- Portfolio of Radiation Tolerant standalone components and processing modules.
- Long term legacy and experience for real Space requirements, proven with success on mythical Space missions.
- Space radiations characterization know-how:
  - Detailed radiations test reports (TID, SEE)
  - Mitigation and design advise, for both hardware and software
- Database of RAD hardened or RAD Tolerant components
- Warranted long term procurement and PCN consequences management.
- Reactive technical and business support, upstream and downstream, from a project point of view
- Long-lastingand stron Partnerships with major components manufacturers
- Flexibility to propose and deliver components with reliability grade fitting with the mission, in term of criticality and budget

The reference design kit comes with a global design package, which is made available to designers:

- Schematics
- PCB design, CAO files
- BOM with space qualified part numbers
- Linux BSP (QLS1046 is compliant with certifiable RTOS such as PikeOS and VxWorks for instance)

All this offerhelps to significantly reduce “Time To Mission” . It also strongly mitigates the project risks as adapting a pre-validated architecture. all these elements are available upon request from Teledyne.

TELEDYNE e2v Semiconductors

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