WHITE PAPER

Rugged, Proven DDR4 Memory Portfolio Supports All Space Orbits.

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TELEDYNE | e2v Semiconductors

EXECUTIVE SUMMARY

Satellite payloads continue to evolve to support ultra-high-resolution imaging, live video streaming, synthetic aperture radar (SAR), SATCOM capabilities, device-to-device (D2D) communication, and space situational awareness (SSA).Moreover, future satellites will increasingly run **AI directly on-orbit**, using advanced, radiation-tolerant compute to analyze data, adapt missions, and manage themselves in real time. A shift that turns spacecraft into **autonomous, reconfigurable intelligence nodes** that deliver faster insights, reduce reliance on ground control, and unlock entirely new mission profiles.

The volume of data generated in orbit shows no signs of slowing, placing ever increasing emphasis on a core component, namely space-grade memory. Consider that one minute of SAR data typically requires 70 Gb of storage. For this reason, operators want to process more of this data in space to avoid overwhelming downlink capacity and to enable autonomous decision-making.

As you will discover, Teledyne e2v responded in 2021 by pioneering the first radiation-tolerant DDR4 SDRAM memory for space, and it remains the market leader with a scalable, pin-compatible portfolio now spanning 4 GB, 8 GB, and recently 16 GB capacities.

Readers will discover the environmental and technical challenges of space-grade SDRAM, and how Teledyne e2v's modern DDR4 portfolio unlocks a new era of performance, flexibility, and reliability for high-throughput satellite (HTS) payloads, and also for next-generation applications such as on-board AI processing, autonomous navigation, and advanced edge computing across deep-space missions and low-Earth orbit constellations.

This white paper is split into six sections:

1. Introduction
2. **Evolution of DDR memory** and the **benefits of DDR4**
3. **Space level qualification needs** and the implication for operators of payloads in various earth orbits
4. **Technical benefits and innovations of Teledyne e2v's** scalable memory offering
5. A word on **space applications** and the inherent **value advantage of DDR4**.
6. Conclusions

1. INTRODUCTION: THE NEWSPACE DATA EXPLOSION

The space industry is shifting from traditional, single-satellite missions to constellations, real-time services, and AI-enabled edge autonomy. Space today is big business, and operators seek new revenue by delivering value-added applications such as:

- Ultra high-resolution imagery
- Real-time analytics and AI inference on-orbit
- Extended acquisition windows and longer dwell times
- Software-defined payloads and reconfigurable satellites

Industry forecasts reflect this trend and estimate that:

- The global satellite data services market, valued at $6 billion[1] in 2020, is projected to reach $45 billion by 2030, indicating a 22% compound annual growth rate (CAGR) over the decade
- EO and geospatial data services revenue is forecast to hit around $15 billion by 2030, with some regions (Europe, APAC) growing >20% CAGR from 2024–2030, driven by AI-enabled analytics, hyperspectral and high-revisit constellations, and edge/onboard processing.

[1]Source: Allied Market Research, "Satellite Data Services Market Statistics 2021-2030", 2023

We already see records being broken for high throughput satellites (HTS) as publicly claimed by ViaSats's ViaSat 3 Americas platform. Launched in May 2023, it was designed to deliver 1 Tbps throughput. Payload processing chains, ADC/DAC front-ends, FPGAs, microprocessors, GPUs can now generate and process massive data streams. But without sufficient high-speed, high-density, radiation-tolerant memory, these capabilities cannot be realized.

In modern satellite designs, memory is thus, no longer, a supporting component, rather it is the gatekeeper of mission capability.

Why Memory Has Become the Bottleneck

Space-grade FPGAs offer high logic gate density and multi-gigabit I/O, but typically only have **tens of megabits** of internal memory on hand. Space-grade CPUs provide even less. To buffer, store, and process data in real time, designers rely on considerable amounts of off-chip SDRAM. However, legacy memory solutions present multiple limitations:

- **Limited bandwidth**
  - DDR3 and older generations cannot keep pace with GHz-rate data or real-time AI inference workloads.
- **Insufficient capacity**
  - 2 Gb to 8 Gb densities are common in DDR3-based solutions — far below modern mission requirements.
- **Large physical size**
  - Memory density matters since greater capacity without increasing on orbit mass, complexity whilst limiting power demand.
  - In addition, multiple discrete device packages consume board area and complicate routing (impedance management) and thermal design in a world where every cubic centimeter matters.
- **High power consumption**
  - Older technologies demand higher voltage supply wasting power in refresh and I/O operations.
- **Qualification gaps**
  - COTS memory cannot survive radiation or meet mission-lifetime expectations without substantial mitigation. It requires shielding, redundancy, ECC, derating, or screening, since missions cannot tolerate soft data errors on orbit. These extra steps inevitably increase cost, risk, and delivery lead time.

In short: existing memory options (e.g DDR3) have held back payload innovation.

The Challenges of Space-Grade Memory Design

Developing memory for space is a uniquely complex challenge because of the balance of performance, density, size, power, reliability, and radiation tolerance needed. Designers must contend with:

- **Radiation Effects**
  - SEU, SEFI, SEL, and cumulative ionizing radiation (TID) degradation differs across **LEO, MEO, and GEO,** meaning memory solutions must be **orbit-specific**
- **Thermal Extremes & Cycling**
  - From -55 °C to +125 °C, across thousands of cycles over mission life
- **SWaP Constraints**
  - Especially in small satellites and high-integration modules
- **Qualification Requirements**
  - Different missions (LEO/MEO/GEO) demand different qualification levels since qualification is a risk-management methodology and not a mere checkbox activity.

[2]Source: ABI Research, Aug 2025; World Economic Forum & Deloitte, May 2024; Reuters coverage of sovereign EO constellation build-outs (2024–2025).

- **Longevity & Supply Chain**
  - Space programs often require components with **10–15-year availability** and be supplied with comprehensive documentation, test data, and heritage. Managing such demand requires a fundamentally different mindset than one focused on commercial applications; a world where the specialists at Teledyne e2v thrive.

These factors help explain why few suppliers operate successfully in this domain and why Teledyne e2v's experience and heritage matter.

2. 25 YEARS OF DDR EVOLUTION

Over the past quarter century, DDR memory has evolved from the early 200 MHz modules of DDR1 to the multi-gigahertz transfer speeds of DDR5. Each generation has pushed bandwidth, efficiency, and power management forward to meet the soaring data demands of advanced processors, AI accelerators, and graphics systems.

Generation	Typical Data Rate (MT/s)	Theoretical Bandwidth per 64-bit Channel (GB/s)	JEDEC Status	Notes
DDR1	200-400	1.6-3.2	Finalized (DDR SDRAM)	Introduced 2000, 2.5 V signaling
DDR2	400-800	3.2-6.4	Finalized (DDR2 SDRAM)	Lower voltage, improved prefetch
DDR3	800-1866	6.4-14.9	Finalized (DDR3 SDRAM)	Wider adoption, 1.5 V typical
DDR4	1600-3200	12.8-25.6	Finalized (DDR4 SDRAM)	Introduced bank groups, 1.2 V
DDR5	3200-8000	25.6-70.4	Finalized (DDR5 SDRAM)	Introduced dual 32-bit subchannels, 1.1 V

Innovations marking the transition from DDR3 to DDR4

DDR4 introduces several hardware enhancements designed to reduce power consumption. The I/O voltage (VDDQ) has been lowered from 1.35 V in DDR3 to 1.2 V, while an additional 2.5 V supply (Vpp) activates the internal word line more efficiently, cutting power use by around 10%. The data bus interface has transitioned from push-pull series-stub terminated logic (SSTL) to pseudo-open-drain (POD) signaling, which consumes power only when transmitting logic "0." Terminating to VDDQ instead of half that voltage allows designers to fine-tune signal amplitude in situ. DDR4 also implements Data Bus Inversion (DBI), which minimizes the number of bits driven low, further reducing switching activity, noise, and improving signal integrity.

Overall DDR4 Power Advantage

Together, these innovations—including the lower VDDQ, the external Vpp supply, POD signaling, VDDQ termination, and smaller row activation currents deliver significantly lower power consumption than DDR3 SDRAM. At equivalent data rates, DDR4 achieves up to 30% higher power efficiency. This gain can be leveraged to increase performance or reduce heat dissipation at comparable speeds. Power-prediction spreadsheets and ICEPAK/ECXML thermal models are also available from Teledyne e2v.

Other DDR4 enhancements

• **Increased Bank Groups for Higher Bandwidth**
DDR4 doubles the number of internal banks to 16, organized into four bank groups. This architecture allows multiple memory operations to proceed in parallel, reducing access conflicts and boosting effective throughput at higher frequencies. The result is significantly improved performance scalability compared to DDR3.

• **Improved Signal Integrity and Reliability**
DDR4 introduces several mechanisms to maintain data accuracy at higher speeds, including cyclic redundancy check (CRC) on data transfers, parity on command/address signals, and Data Bus Inversion (DBI) to reduce simultaneous switching noise. Together, these features enhance robustness and ensure reliable operation even under tighter DDR4 timing margins.

Teledyne e2v: Pioneering a New Generation of Space Memory

Teledyne e2v was first to deliver space-grade DDR4 SDRAM and remains the only supplier with a scalable, space-optimized portfolio — featuring its own dedicated LEO qualification flow, fully developed in-house.
• Compact 4 GB, 8 GB, and 16 GB densities; all package-, pin- and footprint-compatible
• Radiation-tolerant, space-qualified, and already trusted in flight worldwide
• Tailored options for LEO, MEO, GEO
• Multiple qualification levels offered (NASA 1, 2, 3; ECSS Class 1; Teledyne e2v specific X1 flow)
• Supported by Teledyne e2v's deep test, characterization, and qualification expertise
• Industry-leading miniaturization and packaging

This family presents much more than an incremental upgrade. It is a fundamental step-change in how memory can be designed into space systems.

Teledyne e2v's DDR4 Family: A Scalable Memory Platform for Space

The Teledyne e2v DDR4 family includes 4, 8 and 16 GB. Engineering models of the latter having been market released in August 2025, and first FM shipped in Q4 2025. This capacity progression aligns directly with the evolution of satellite capabilities: as payloads become more sophisticated and data-hungry, memory density must advance. Teledyne e2v has structured its roadmap to grow in lockstep with mission complexity, a key client message: evolution driven by real-world satellite demands.

Pin- and footprint-compatibility across all densities

With common mechanical dimensions and electrical interfacing across the portfolio brings significant design benefits of scalability, this means:
• Design the board once
• Qualify it once
• Scale memory capacity without redesigning
• Reuse firmware and memory controller logic
• Avoid new layout, new routing, new thermal modelling
• Reduce cost, risk, and time to market dramatically

In an industry where a board re-spin can cost millions and delay missions by months, this is a major commercial differentiator.

[3]Source: X1 is a LEO space qualification level supplied exclusively by Teledyne e2v.

3. ORBIT-TAILORED DEVICE FLEXIBILITY

Different Earth orbits impose different radiation and longevity design challenges:

- **LEO (Low Earth Orbit):** higher particle flux, shorter mission life and cost-sensitivity
- **MEO (Medium Earth Orbit):** overall, the most challenging zone for electronics since it includes the Van Allen radiation belt and is subjected to lengthy thermal cycles
- **GEO (Geostationary Orbit):** long missions (10–15 years), demands high TID exposure capable components and maximum robustness

Orbit	Orbital height - Radiation impact	Thermal Cycling	Debris Risk	Longevity	Latency
LEO	160-2000 km - Moderate	High	High	Short	Low
MEO	2000-35786 km - High	Moderate	Low	Medium	Medium
GEO	> 35786 km - High	Low	Very Low	Very Long	High

Each orbit presents a unique set of challenges for electronics, primarily driven by the radiation, and thermal environment, along with mission duration. Designing electronics for space requires careful consideration to balance risk factors driving the qualification demands of the market.

4. KEY INNOVATIONS AND TECHNICAL ADVANTAGES

Teledyne e2v's DDR4 memory is a proven **radiation-tolerant architecture.** Teledyne e2v has extensively characterized and validated the device against radiation. Moreover, robust space flows ensure device robustness in Space. These devices are built using a multi-chip package.

Each DDR4 module integrates multiple memory dies and access management combined with error correction control (ECC) logic in a single package. For instance, the original 4 GB version comprises four 1 GB DDR4 dies, and a dedicated error correction coding (ECC). All variants use a 72-bit data interface providing native ECC support comprising 64-bits data and 8-bits ECC.

This MCP approach delivers the highest **volumetric density in the smallest footprint.**
Moreover, physically short interconnect paths lead to better signal integrity through easier and consistent impedance matching.

High Throughput Performance

Teledyne e2v's DDR4 design supports a data rate of up to 2400 MT/s I/O speed resulting in a data rate of:
- ~19.2 GBps effective bandwidth with ECC
- ~21.6 GBps without ECC

This represents a 62% bandwidth increase over DDR3 solutions commonly used today.

Radiation tolerance

Unlike COTS DDR4, Teledyne e2v devices are proven radiation-tolerant devices. Typical radiation performance includes:

- **TID:** 100krad,
- **SEL:** Tested up to 60 MeV
- **SEU/SEFI:** data up to 60MeV

These figures demonstrate resilience to both cumulative and single-event effects across LEO, MEO, and GEO environments.

Built-in Error Mitigations

- Single Error Correction, Double Error Detection (SECDED) ECC corrects most bit flips automatically
- Internal architecture isolates memory banks to limit error propagation
- Robust power delivery support reduces latch-up risk
- Programmable timing and refresh options optimize behavior in radiation events

Qualification Options

Depending on mission profile, parts can be supplied with:

- NASA Levels 1, 2 & 3
- ECSS Class 1 (European standards)
- Teledyne e2v X1 (developed for LEO)
- Custom screening and lot-by-lot reports are also available

This mission-specific qualification flexibility is a key advantage. It allows system builders to find just the right qualification level and manage mission risk.

DDR4 memory data integrity aspects

The onboard ECC logic enables:

- Single Error Correction, Double Error Detection (SECDED)
- Automatic mitigation of radiation-induced bit flips
- Significantly reduced soft-error rates than COTS options

At a system level, DDR4 offers improved reliability, availability and serviceability (RAS). Integrated real-time, CRC error detection of the data bus during write operations is available along with parity checking of the command and address buses. Unlike forerunner DDR3 memories, DDR4 can be configured to block commands upon detection of parity errors.

As a true DDR4 design, the device uses an 8n prefetch architecture, allowing internal data to be accessed at 1/8 the external data rate. This provides high throughput without recourse to elevated internal clock speeds.
Bank interleaving enables parallel access to different memory banks, reducing latency and improving sustained bandwidth, critical for continuous data streaming from sensors or for real-time AI workloads.

Miniaturization

The MCP packaged memory has been carefully designed to ensure all I/O command and address lines are dynamically terminated to reduce signal integrity challenges. Short signal paths help minimize parasitic anomalies easing the interface to the memory controller system.

All density options are offered in the same compact organic PGBA package:
- 15 mm × 20 mm × 1.92 mm
- 391 balls, 0.8 mm pitch
- Available as leaded

5. SPACE APPLICATIONS FOR DDR4

In modern Earth-observation, communications and on-orbit analytics payloads, DDR4 memory is becoming a key enabler of high-throughput on-board processing. For example, the satellite industry recognizes that ultra-high-resolution imaging, live video streaming, and in-orbit AI/edge compute all demand much greater memory bandwidth and capacity than previous generations.

As one industry article[4] observes, "DDR4 will allow the satellite industry to offer higher-throughput on-board processing and increased acquisition times" — which enables longer contiguous data capture and more aggressive buffering in-orbit. Because DDR4 supports higher transfer rates and densities, spacecraft payload designers can ingest more raw data from sensors (e.g., hyperspectral, synthetic aperture radar) and perform real-time or near-real-time processing rather than simply storing and down-linking everything (see figure 1).

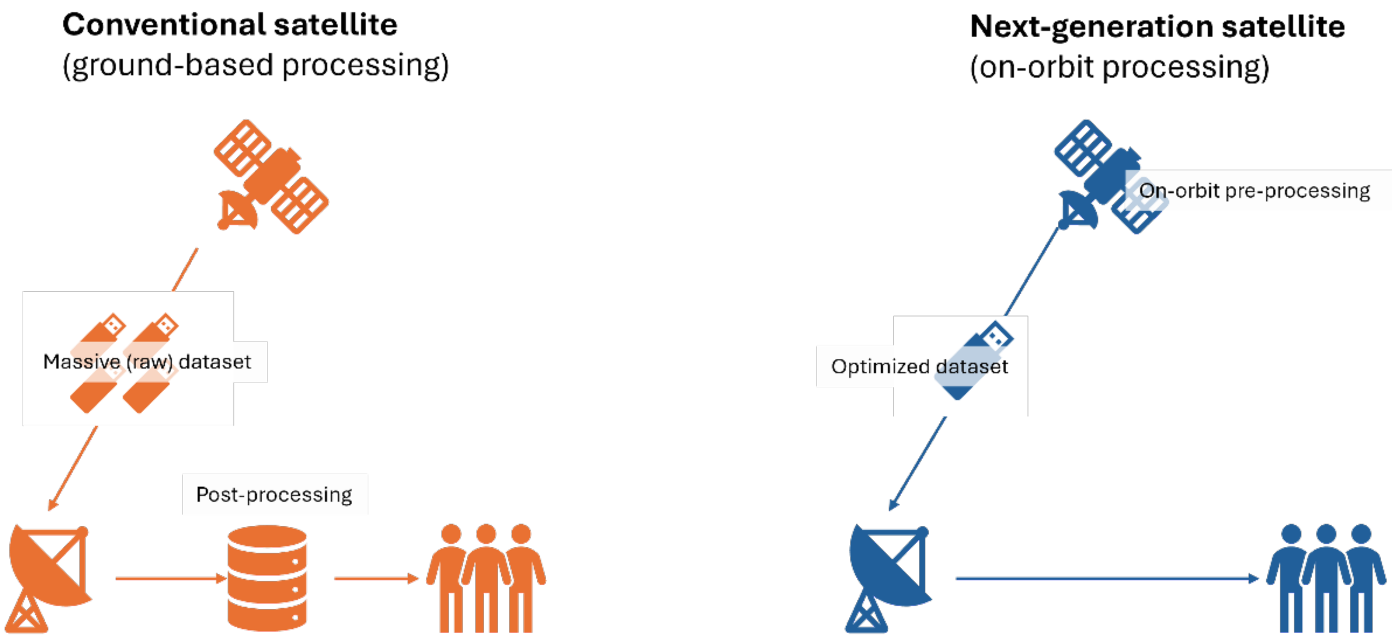

Figure 1 On-orbit processing aided by fast DDR4 memory makes better use of downlink capacity

[4]*Source: Dr. R. Bedi, of Spacechips "DDR4 will enable new applications in the satellite industry" EDNAsia, 2020*

6. CONCLUSION

For modern space systems, memory is mission critical. If the memory channel caps system throughput, your payload leaves performance and revenue on the table. Teledyne e2v's space-qualified DDR4 changes that equation with genuine headroom (bandwidth), scalability without redesign (4/8/16 GB today), orbit-specific qualification, and a compact, power-efficient form factor with native ECC.

If you're architecting HTSs, SAR, video, AI/ML, or software-defined payloads and you need a single, proven footprint that scales across missions, this DDR4 family is the practical way to unlock performance now and preserve future flexibility options.

Teledyne e2v supports its products with extensive documentation, design-in tools, and highly skilled application engineers. You can find further details and contact options via: https://semiconductors.teledyne-e2v.com/

In short:
Teledyne e2v's DDR4 memory doesn't just make existing designs faster, it enables entirely new classes of space systems.

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