WHITE PAPER

Non-Uniform Sampling for High-Bandwidth ADCs: Reducing Data Throughput Without Sacrificing Fidelity

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This article highlights a non-uniform sampling (NUS) experimental demonstrator for RF microwave reception based on a zero-IF design. It uses a Teledyne EV10AS940 direct conversion ADC. The demonstrator will enable NUS performance evaluation in spectrally crowded RF microwave environments across multiple Nyquist zones. The study focuses on evaluating compressive sampling and data volume reduction techniques to reduce overall system complexity and the resulting power consumption.

The demonstrator aims at extracting signal power across the entire analog bandwidth (>30 GHz) of the target data converter. Sampling at rates up to 12.8 giga samples/second (12.8 Gsps) leads to output data rates of several hundred giga-bits per second; a huge real-time processing challenge. Much of the focus therefore is on establishing suitable hardware and data compression techniques in support of the study's basic objective.

This study shows that NUS can be successfully deployed to detect and demodulate crowded multi-carrier DVB-S2 signal streams in direct conversion contexts.

NUS HISTORY AND ADVANCEMENTS

Though not as well known to many communication engineers and signal processing students today as his predecessors C. Shannon and H. Nyquist, it was in his 1967 paper that Henry Landau defined the concept of «occupied bandwidth» - the total portion of the frequency spectrum that signal energy occupies. Thus, launching a unification to sampling theory that accounts for both practical system limitations as well as allowing a route to new high performance radio architectures.

What is non-uniform sampling (NUS)?

Non-uniform or compressed sampling is a method used in signal processing where data points are collected at irregular or varying time intervals. This approach can be useful when sensors or systems cannot sample at fixed rates, or when focusing resources on specific parts of a signal. Non-uniform sampling still allows accurate signal reconstruction if the average sampling rate meets the Nyquist condition, though NUS reconstruction algorithms are more complex.

Landau's key theoretical result, a twist on Nyquist-Shannon, was that the average sampling rate need only be at least twice the total occupied signal bandwidth for perfect reconstruction. In effect:

- If a signal occupies several (n) disjoint spectral bands summing to a bandwidth nB, the required average sampling rate is ≥ 2nB.
- This result assumes prior spectrum knowledge where bands are «occupied» with viable signal energy, a reasonable assumption for most RF systems today
- •The result generalizes the Nyquist-Shannon sampling theorem to include non-uniform sampling as well as signals with non-contiguous spectral support.

This foundational concept, though elusive in traditional texts, is starting to see greater levels of research focus as the communications, Radar and military industries work to deliver ever smarter solutions.

NUS IN ACTION

Non-uniform or compressed sampling eases sampling system design by removing the need for a sample clock to always be double the signal bandwidth, for signal recovery. The NUS simulated waveform below (figure 1) shows the effect of random NUS sampling of the blue input signal. The lower yellow trace is the sample output with samples randomly removed demonstrating a compression ratio (CR) of 1, 2 and 4.

How Landau changed sampling theory back in 1967

In his 1967 paper, Henry Landau defined the concept of «occupied bandwidth». That is the total portion of the frequency spectrum that a signal occupies. This observation assumes it is known, which parts of the spectrum contain signal energy. Occupied bandwidth differs from the mere maximum frequency component of the signal in that it only counts the span of frequency bands where the signal has non-negligible energy. This hints that with sparse signal density; lower performance converters might achieve more than is possible under standard Nyquist criteria.

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An early practical paper[1] on implementing NUS was produced by researchers at Rostock University in 2003. The paper focused on the importance of sampling driver (SD) design. Their key research conclusions can be summarized as follows:

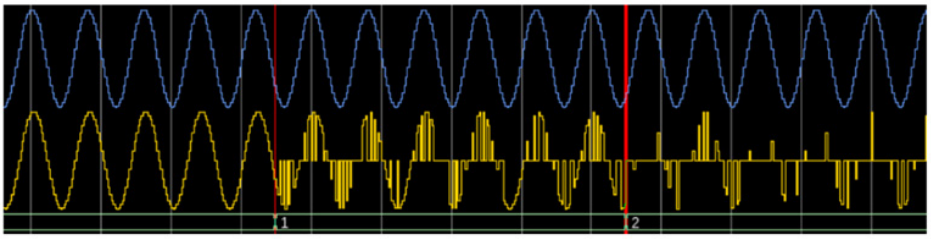

Figure 1 - Simulation of the NUS sampler. The input signal (blue); the yellow waveform shows the output with randomly removed samples for a compression (CR) of 1, 2, and 4.

- Equivalent Bandwidth (EB) Enhancement: Deliberate non-uniform sampling dramatically increases the equivalent sampling rate (by 40 x) and thus the effective processing bandwidth of digital systems. With a mean sampling rate of 80 MHz, a prototype achieved an EB of 1.6 GHz; forty times that of a uniform sampled system.
- Sample Driver Architecture: They detailed an efficient synchronous sample driver, built around a pseudo-random number generator (PRNG) and a digital controllable delay line.
- Phase Shifting and Random Number Correlation: To address the issue of consecutive samples occurring too close together (i.e. within the recovery time of the ADC), the team offered sample clock phase shifting and probabilistic approaches for the pseudo-random sampling as solutions to further explore.

Drawing from early experiments, learnings show that with careful sample driver design, including statistical control over sampling pulses, enables EB expansion. But clearly, there is a complexity penalty, requiring thoughtful engineering to match ADC hardware constraints with NUS sample clock and reconstruction algorithm design.

NUS STUDY OBJECTIVES

Today, with ever faster data converters there is an alternative design constraint under the magnifying glass. That is assisting with managing the massive data output. Interfacing and processing are critical pain points leading efforts directed at data compression. This is the lens through which this study is to be judged.

A practical, advanced RF demonstrator demands the ability to evaluate basic receiver functions. And so, the proposed system provides an RF detection and receiver capability. The source signal energy was defined to be DVB-S2 coded carriers. Three use cases are under evaluation (figure 2):

1. Detection of a DVB-S2 signal at different power levels only affected by the receive electronics' thermal noise
2. Several DVB-S2 carriers (with different power levels) located in the Nyquist band and affected by the electronics' thermal noise. Only one carrier needs demodulating
3. A DVB-S2 signal interfered with by a noise pattern (NP) occurring within the Nyquist zone of interest

EV10AS940 features

- Sample rate up to 12.8 Gsps
- 10-bit resolution with a > 30 GHz bandwidth reaching Ka-band
- 2.5 W power consumption
- Integrated digital down converter and numerical controlled oscillators facilitate data compression and advanced signal hopping
- Low-latency, license free ESIstream serial output data protocol with DC balance and embedded encoding

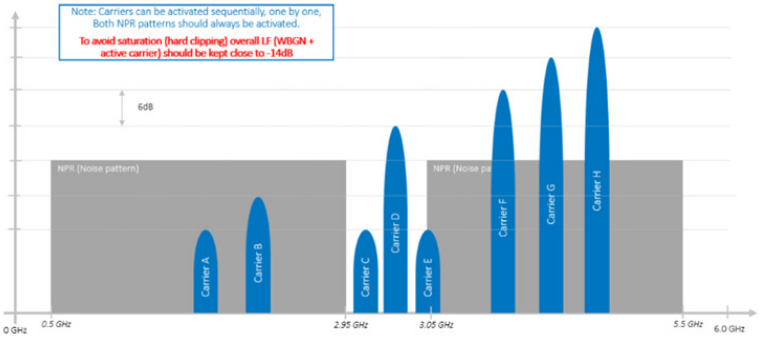

Figure 2 - Experimental demonstrator use case detail.

1. System Increases Dynamic Range of Digital Receivers | 2021-04-11 | Microwave Journal

A NOVEL FRONT-END ADC POWERS THE NUS DEMONSTRATOR – THE EV10AS940

The EV10AS940 is a 10-bit Ka-band capable, single channel analog-to-digital converter (ADC) with a sampling rate up to 12.8 GSps, and 2.5 W power consumption. The ADC features an analog bandwidth of > 30 GHz. Moreover, it embeds digital processing features including digital down conversion (DDC) and frequency hopping (FH) capabilities with multiple digital channels accessible thanks to the integration of five numerically controlled oscillators (NCOs).

On the data output side, eleven high-speed serial lanes are supplied which operate at 12.8 GHz. The device uses Teledyne e2v's license-free 62/64b ESIstream protocol for data transmission. Data can be sent in either 10-bit real mode or via the on-board decimation module allowing decimation factors from 2-1024 (or 4-2048 for I/Q encoding).

EXPERIMENTAL SDR AND TEST BENCH SYSTEM USING ZYNC ZCU111

The demonstrator comprised three key functional blocks. The front-end features the above fast conversion 10-bit data converter delivered on an FPGA mezzanine card (FMC+). The FMC+ is easily plugged in to a commercial FPGA evaluation system, in this case the ZCU111. This FPGA development system targets RF applications and features an RF system-on-chip combining both FPGA functions and a powerful ARM CPU.

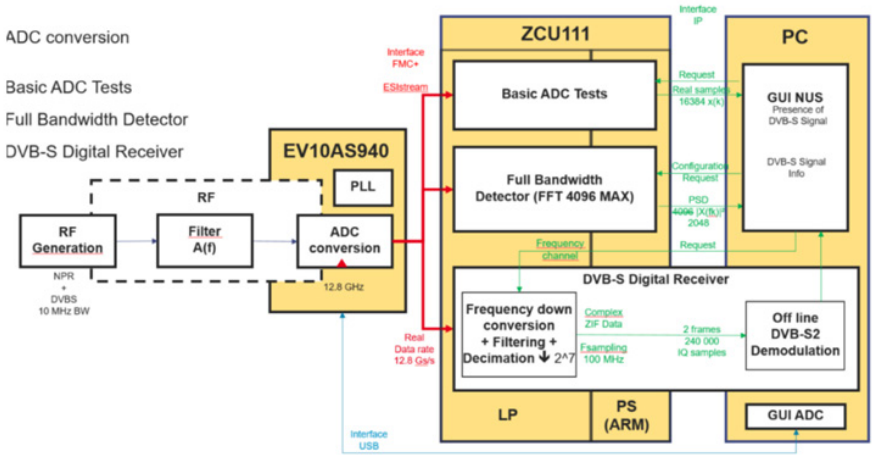

Figure 3 - NUS demonstrator system block diagram.

Three key hardware cores were developed on the ZCU111 in this study as shown in the diagram (figure 3) and include:

- Basic ADC set-up tests and calibration
- The full bandwidth DVB-S2 detector
- The DVB-S2 receiver – in this case, note that the processing board is only providing frequency down conversion, filtering and decimation. The full demodulation chain relies on a local PC for offline demodulation.

The final aspect of the demonstrator is a local PC used to control the ADC and the demonstrator, perform DVB-S2 demodulation and to display results in a graphical user interface (GUI).

To simplify hardware design of the DVB-S2 receiver, several constraints were implemented:

- Signal bandwidth is fixed at 10 MHz
- DVB-S2 generation and ADC to share the same 10 MHz reference clock
- The DVB-S2 center frequency is defined by the operator (e.g., from an NUS detector)
- The DVB-S2 generator always transmits the same DVB-S2 frame, simplifying bit error rate (BER) estimation.

TEST ENVIRONMENT SET-UP

The RF signal for the demonstrator is generated by combining two instruments with a 3 dB combiner (figure 4). These are:

- A Rohde & Schwarz SMBV (vector signal generator) for the DVB-S2 signal
- An Arbitrary Waveform Generator (AWG) for the noise power signal

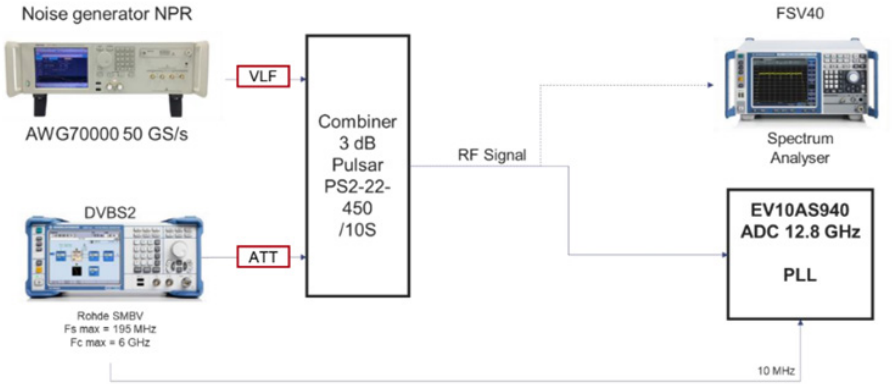

Figure 4 - NUS demonstrator RF test set up.

This setup allows flexible adjustments: the DVB-S2 signal's power and frequency can be changed without affecting the noise signal. The combined RF output can also be sent to a spectrum analyser.

As the DVB-S2 and noise signal are independently sourced, they both lose 3dB across the passive combiner. A VLF filter rejects 12.5 GHz spurious signals from the arbitrary wave generator. An attenuator (ATT) applied to the DVB-S2 branch allows output power level setting relative to the noise signal. The combiner isolation is around 20 dB. A 10 MHz, 0 dBm reference clock from the DVB-S2 source is provided to the ADC FMC+.

IMPLEMENTATION - ESTABLISHING SYSTEM LEVEL PARAMETERS

The RF detector

The detector was conceived to deliver a time domain signal power estimation after a 10 MHz channelization had occurred. The measured power is then to be compared with the noise level estimate to decide if there is useful signal energy in a target channel. Channelization is performed using an FFT. Prior to the FFT a windowing function is applied to the data signal to help reduce the influence of signal side lobes in the detected result. After the complex FFT, multiple FFT results are accumulated to help reduce signal variance over time and achieve more robust signal detection defined through probabilistic system parameter setting.

As the objective of the demonstrator is to evaluate NUS, a time gap between FFT windows was added corresponding to an effective data compression ratio (CR). The achieved CR is impacted by the resource utilization of the ZCU111 processing board and is also a variable of the compute frequency. A minimum for the compression ratio can be calculated as follows:

- The input stream of ADC samples has a frequency fADC = 12.8 GHz
- The compute frequency for the system was decided to be fPROC = 250 MHz
- The number of parallel FFT pipelines was set at P = 16

The above two performance factors were selected empirically based on experience and apparent FPGA resource availability. From these factors, a minimum CR is calculable as follows:

CRmin = 1/P x fADC/Fproc producing a minimum value of 3.2. This was rounded to 3.3 to account for delays in the FPGA

Detection throughput rate, i.e. the rate at which the detection algorithm can react comprises a fixed and variable element. The fixed element is the recovery time comprising the FFT size divided by the processing frequency aggregated with the time needed to read the FFT accumulators (adjacent table 1).

FFT size	$t_{recovery}$ (µs)
512	3.072
1024	6.144
2048	12.288
4096	24.576

Table 1 - Detection recovery time for various FFT sizes.

The variable term is the total time window used for sampling. Three detection time windows were defined for the experiment, namely 10 microseconds, 1 millisecond and 100 milliseconds. From this, A (the number of complete FFT accumulations) was measured for four different FFT sizes, see table 2 below.

Allowed detection time	FFT-512		FFT-1024		FFT-2048		FFT-4096	
	A	t_{signal} (µs)	A	t_{signal} (µs)	A	t_{signal} (µs)	A	t_{signal} (µs)
10 µs	52	2.08	14	1.12	-	-	-	-
1 ms	7552	302	3764	301	1870	299	923	295
100 ms	757552	30302	378764	30301	189370	30299	94673	30295

Table 2 - Maximum FFT accumulations allowed for various detection times and FFT sizes. CR is set to 3.3.

Clearly, the brief 10-microsecond window only allows for limited FFT sizes (up to 1024). However, for the 1 and 100 ms windows, the recovery time is insignificant for all FFT sizes.

User control features designed into the detector module comprise:

- The compression ratio – from CR = 3.3 upwards
- The applied windowing function – six functions are supported
- FFT size - the size of the FFT changes the spectral resolution. If the ADC converts the input signal at 12.8 GHz, a FFT size of 4096 implies a RBW (Resolution Bandwidth) of 3.125 MHz. Thus, FFT size selects the frequency channel.
- The number of FFT accumulations (i.e. the detection rate)
- The detection threshold

Note that the FFT size selected influences the windowing function shown below. The length of the window must be equal to the FFT size. The width of the primary lobe increases (figure 5 'a'). Shown here are Hann windows for 512, 1024, 2048 and 4096 FFTs. With the Hann window function applied with 4096 sample the RBW increases from 3.125 MHz to around 10 MHz (see fig. 5 'b') representing our designed channel width.

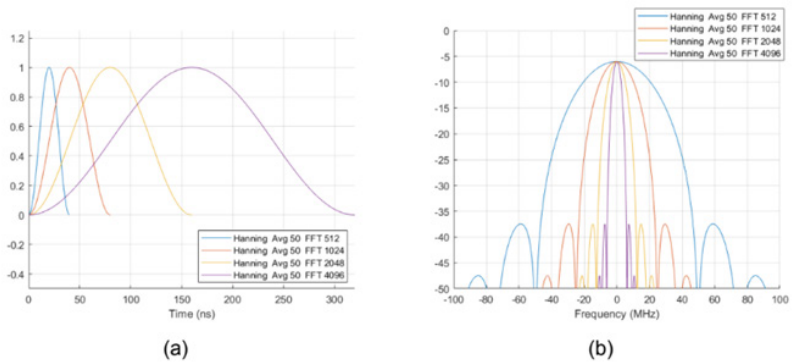

Figure 5 - Effect of FFT size on Hann windowing function.

Preliminary demonstrator results (detector)

A series of tests of the detector were performed for different SNR scenarios with the objective of defining a minimum detection duration (figure 6), yielding a bad detection and false alarm probabilities (Pmd and Pfa) below desired levels, namely:

- Pmd < 10-2 and Pfa < 10-6

For each of the five scenarios, optimization work using configuration variables was performed to determine the minimum time to achieve detection compliant to the probabilistic variables (Pmd and Pfa). Experimental results were compiled and compared to earlier theoretical assumptions are as follows:

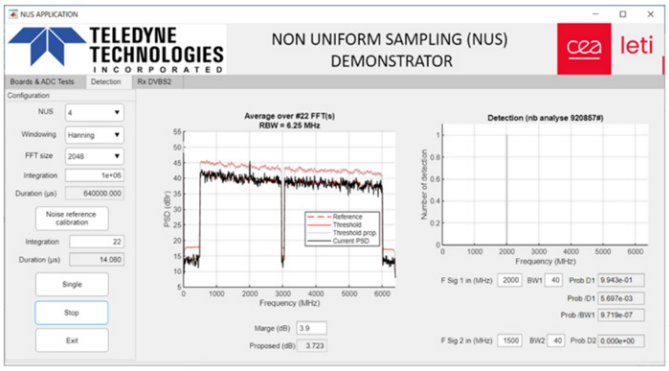

Figure 6 - Confirmed DVBS2 signal detection @2 GHz, SNR = 12 dB (FFT size 2048).

SNR	Theoretical [D122]	Preliminary Practical			
(dB)	Time period (µs)	Time period (µs)	FFT integration	FFT size	Margin (dB)
18	1.6	1.92	3	2048	8.04
12	3.2	3.84	6	2048	6.50
6	12.8	14.08	22	2048	3.90
0	104	117.76	92	4096	2.00
-6	820	1280.00	1000	4096	0.66

Table 3 - Theoretical and measured detection duration comparison.

These results closely correlate with the theoretical assumptions (table 3). They yield a detection time degradation of less than 20 % except for the most challenging scenario of -6 dB SNR. Note that at elevated SNRs, smaller FFTs are recommended, reducing the time window. At 12.8 GHz, a 4096 FFT window is equal to 0.32 µs while the 2048 FFT window is only 0.16 µs.

Preliminary demonstrator results (receiver)

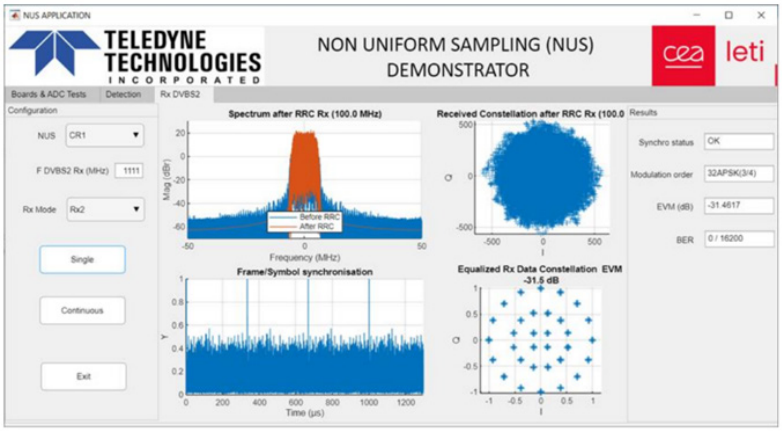

Figure 7 - DVB-S2 signal identification and demodulation @ 1111 MHz without noise pattern.

A first version of the receiver design has been developed with initial results gathered. The chart below provides confirmation of basic operation (figure 7). This shows signal reception without any additive noise pattern and with all data samples currently preserved (CR = 1). Frame synchronization is correct, and the constellation is almost perfect. Estimated error vector magnitude (EVM) is lower than -30 dB and the BER is zero over a full DVB-S2 frame.

CONCLUSIONS

This preliminary report highlights some of the benefits of NUS applied to broadband direct sampling applications; those being a route to compressed sampling, reduced data flow along with potential power savings. The development of an FPGA-based real-time processing system is detailed; one capable of detecting RF signal energy and providing zero-IF based digital down conversion and DVB-S2 demodulation.

Effective NUS-based signal detection was evaluated and confirmed for five different SNR scenarios. This work has already helped to highlight some of the system design trade-offs necessary to successfully deploy NUS in future systems. For example, it was shown that a minimum compression ratio (CR) of 3.3 was achievable with the selected hardware. The research continues with the hope to return to the topic and uncover receiver performance characteristics and share experimental results using different NUS compression ratios over the coming months.

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