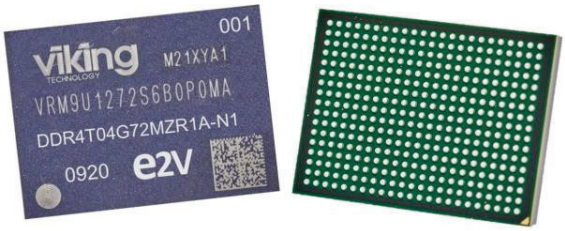
4GB / 8GB Radiation Tolerant DDR4 Memory

Datasheet DS 60S 219460 (G)



Product Summary

The 4GB / 8GB Radiation Tolerant DDR4 Memory Multi-Chip Package (MCP) is a Ultra High Density Memory Solution, targeting Space Embedded Systems & Applications.

Such MCP products achieve significantly higher memory performance and density per cubic inch than using several discrete memories.

Top level Features

- Density: 4GB / 8GB
- Bus width: 72 bits (64 bits data + 8 bits ECC)
- Speed: Up to 2400 MT/s
- Module size: 15 mm x 20 mm x 1.92 mm
- Solder Spheres: Count 391
- Pitch: 0.8 mm
- Mass: 1.2g +/- 0.1g

Space Key Features

- **Space Qualification**:
  - Up to NASA Level 1 (based on NASA EEE-INST-002 - Section M4 – PEMs)
  - Up to ECSS Class 1 (ECSS-Q-ST-60-13C)

- **Low outgassing**
  - Compliant with ASTM 595 and ESCC-Q-ST-70-02

- **Radiation Tolerance (for NASA and ECSS Flight Models):**

	Revision A	Revision B
SEL LET Threshold	> 60.88 MeV.cm²/mg	> 62.5 MeV.cm²/mg
SEU evaluated from LET 2.6 MeV.cm²/mg & Upset cross-section @ 60.88 MeV.cm²/mg	8.73E-12 cm²/bit	Under characterization
SEFI evaluated from LET 2.6 MeV.cm²/mg & SEFI cross-section @ 60.88 MeV.cm²/mg	4.17E-4 cm²/device	Under characterization
TID tolerance	100 krad(Si)	100 krad(Si)
Protons	Data available up to 190MeV	Data will be available up to 190MeV

Revision History

Date	Revision	Description
09/2024	G	Table 32 & 33 Speed bins update and table 34 timing update, TBD replaced by values, 1.3.2 Design guide: explanations reduced to essential, other recommendations moved to the User Guide document “DDR4T0xG72_General_User_Guide”, Added paragraphe « 4.2 Weight », All 1866MHz characteristics removed (not applicable), All reference to TDQS_c and TDQS_t removed (not applicable).
06/2024	F2	Chapter 1.5 / DDR4 SPEED BINs and Timing Summary: DDR4-1866 Speen Bin deleted Table 1 / DDR4 Design Guide: Additional information (± 5mils) added in Trace Lenghts Table 5 / Addressing: Die Organization information removed (Export Controlled information) Table 5 / Corrections in BG Address lines & Row Address for 4GB Rev B: 512Mx72 Chapter 7.2 / Thermal considerations: Junction to case information added Chapter 7.2 / Thermal considerations: Combination of chapters 7.2.1 & 7.2.2 on Thermal conditions Table 27 / DRAM Component Operating Temperature Range : Some details added on Tc and Tj
01/2024	F1	Update “4GB” and “8GB” to “revision A” and “revision B” Add Rev B in Ordering information Outgassing information confirmed on both revisions
07/2023	F	Change radiation tolerance sentence Add X1 reference in Ordering information Add note column on table 6 ball description Add 7.5 DDR4 power consumption
05/2023	E1	“Proprietary and Confidential” removed
03/2022	E	Update with 8GB information and ordering Information
04/2021	D	Add Capacitors note Add Outgassing feature Preliminary” removed Add Mass Add Differential Clock Termination scheme Add DDR4P and Grade notes in “Ordering Information” Add new references in “orderable parts” SEU LET sensitivity Theshold changed to 2.6 MeV
09/2020	C	Temperature compensated refresh only operates on -40 to 105°C temperature range Update of mechanical outline and orderable parts list/table Add termination resistor value Correction of ball size from 0.5 to 0.4 mm
06/2020	B	Update of « Ordering Information » Add ball’s information; Add orderable parts Change TID target to 100krad Add die configuration and notes Add Mass for RoHS parts Change PadOut picture Add Parity pin
03/2020	A	Initial Baseline Release

Ordering Information

Product Name	Radiation Performance	DDR Size[3]	Bus width	Temperature Range[3]	Package Type[3]	Speed (MT/s)	Rev[1]	Grade[4][5]
DDR4[2]	T: Rad Tol	04G: 4 GByte 08G: 8 GByte	72: 72 bits	M: -55/125C A: -40/105C	ZR: PBGA Stacked Wire Bond (Leaded SnPb) ZS: PBGA Stacked Wire Bond (Leadfree RoHS)	1: 2133 2: 2400	A B	EM: Engineering Models EQM: Engineering Qualification Models -N1: Nasa Level 1 -N2: Nasa Level 2 -N3: Nasa Level 3 -E1: ECSS Class 1 -E2: ECSS Class 2 -E3: ECSS Class 3 -X1: Specific screening flow

Notes:

(1) Revision A parts is configured for x16 and Revision B parts is configured for x8.
(2) "DDR4**P**" prototypes are functional devices dedicated to particular uses. Please contact Teledyne e2v sales office to know more about it
(3) For availability of the different versions, contact Teledyne e2v sales office.
(4) To know more about grades please refer to NE60S220869 on our website (ne-60s-220869-b0.pdf (teledyneimaging.com)
(5) To know more about these following specifications and their screening flows, please contact us:

	Rev A	Rev B
NASA Space Grade Specification	SP 31S 219973	SP 31S 222554
ECSS Class 3 Space Grade Specification	SP 31S 221735	SP 31S 224319
X1 Specific Screening Flow Space Grade Specification	-	SP 31S 222691

Orderable Parts

	Revision A	Revision B
EM	**DDR4T04G72AZS1AEM**: 4GB [-40/105°C] Leaded SnPb 2133MT/s	**DDR4T08G72AZR1BEM:** 8GB [-40/105°C] Leaded SnPb 2133MT/s
		DDR4T08G72AZR2BEM: 8GB [-40/105°C] Leaded SnPb 2400MT/s
	DDR4T04G72AZS2AEM: 4GB [-40/105°C] Leaded SnPb 2400MT/s	**DDR4T04G72AZR1BEM**: 4GB [-40/105°C] Leaded SnPb 2133MT/s
		DDR4T04G72AZR2BEM: 4GB [-40/105°C] Leaded SnPb 2400MT/s
Spatial flow	**DDR4T04G72AZR1AYYY[1]:** 4GB [-40/105°C] Leaded SnPb 2133MT/s	**DDR4T08G72AZR1BYYY[1]**: 8GB [-40/105°C] Leaded SnPb 2133MT/s
		DDR4T08G72AZR2BYYY[1]: 8GB [-40/105°C] Leaded SnPb 2400MT/s
	DDR4T04G72AZR2AYYY[1]: 4GB [-40/105°C] Leaded SnPb 2400MT/s	**DDR4T08G72MZR1BXXX[2]**:8GB [-55/125°C] Leaded SnPb 2133MT/s
		DDR4T08G72MZR2BXXX[2]: 8GB [-55/125°C] Leaded SnPb 2400MT/s
	DDR4T04G72MZR1AXXX[2]: 4GB [-55/125°C] Leaded SnPb 2133MT/s	**DDR4T04G72AZR1BYYY[1]**: 4GB [-40/105°C] Leaded SnPb 2133MT/s
		DDR4T04G72AZR2BYYY[1]: 4GB [-40/105°C] Leaded SnPb 2400MT/s
	DDR4T04G72MZR2AXXX[2]: 4GB [-55/125°C] Leaded SnPb 2400MT/s	**DDR4T04G72MZR1BXXX[2]**: 4GB [-55/125°C] Leaded SnPb 2133MT/s
		DDR4T04G72MZR2BXXX[2]: 4GB [-55/125°C] Leaded SnPb 2400MT/s

Notes:

(1)"YYY" should be replaced by Grades: EQM, -N1, -N2, -N3, -E3, -X1
(2) "XXX" should be replaced by Grades: EQM, -N1, -N2, -N3

Table of Contents

1 Introduction

The 4GB / 8GB Radiation Tolerant DDR4 Memory Multi-Chip Package (MCP) is a Ultra High Density Memory Solution, targeting Space Systems & Applications.

Such MCP products achieve significantly higher memory performance and density per cubic inch than using multiple discrete memories.

1.1 Features

- JEDEC Standard Power Supply
  - VDD = 1.2V ± 5% (VDDQ is internally connected to VDD)
  - External VPP = 2.5 Volt +10%, -5%
- 391 ball MCP
- 1.2V Pseudo-open drain I/O (POD12) DQ lines
- Internally generated VrefDQ
- 72 bit data path : 64+8 bit for ECC implementation
- Programmable CAS Latency: 13,15,16,17,19
- Programmable CAS Write Latency (CWL)
- Programmable Additive Latency (Posted CAS)
- Per DRAM addressability is supported
- Data Bus Inversion support for x8 and x16 devices
- Command/Address (CA) Parity
- On-chip CA Parity detection for the CA bus
- Databus write cyclic redundancy check (CRC)
- Output Driver Calibration
- Reduced interconnect routing
- Reduced trace lengths due to the highly integrated, impedance matched packaging
- Thermally enhanced packaging technology allows silicon integration without performance degradation due to power dissipation (heat)
- Selectable Fixed burst chop of 4 (BC4) and burst length of 8 (BL8) on-the-fly (OTF) via the mode register set (MRS)
- 8n prefetch with:
  - Rev A: 2 bank groups: 8 banks (2 bank groups x 4 banks per bank group)
  - Rev B: 4 bank groups: 16 banks (4 bank groups x 4 banks per bank group)
- Separate activation, read, write, refresh operations for each bank group
- 7 mode registers
- Dynamic On-Die-Termination (ODT) and ODT Park for improved signal integrity
- Self Refresh, Self Refresh abort and several Power Down Modes
- DLL-off mode for power savings
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern
- Asynchronous Reset

- Bidirectional Differentially Buffered Data Strobes
- SnPb and RoHS compliant package available

Notes:

(1) Refer to 'table 2' and 'table 5' for more details on the differences between the various memory versions
(2) ECC uses only the lower byte of the x16 die, the upper byte is not connected

1.2 Benefits

- Very small footprint: saves board space versus implementation with discrete components
- Very high memory capacity per cubic inch
- Very high memory bandwidth per cubic inch
- Rugged: soldered-down PBGA
- Superior signal integrity
- 0.8 mm pitch: leadfree and leaded ball options
- Suitability for use in High-Rel and Space applications requiring Mil-Temp range, small form factor, non-hermetic operation.

1.3 Design Considerations

1.3.1 Data Sheet Information

- This product and/or its specifications are subject to change without notice.
- The latest data sheet document should be retrieved from Teledyne e2v, prior to your design consideration.

1.3.2 Design Guide

DDR4 MCP is designed following JEDEC79-4D. Design rules examples can be found in JEDEC standard JESD21C "DDR4 UDIMM Design specification".

Teledyne dedicated user guide "DDR4T0xG72_General_User_Guide" is available on request.

Table 1: DDR4 Design Guide

Item	Description	Implementation Suggestion
Placement	DDR4 Interface between MCP & Host / Memory Controller	The MCP should be placed as close as possible to the processor/memory controller, with direct / straight interconnect between them.
Command address Rtt Termination	Termination for DDR4 address/command/control signals	No external termination required; all termination resistors are implemented in MCP package. The nominal value of the termination resistors is 69.8 Ω.
Differential Clock Termination	Clock Termination for DDR differential clock input signal	No external termination required; all termination resistors are implemented in MCP package.
RESET_n	Reset Signal	Requires external pull-up to VDD (typically 1K - 4.7KΩ).
ALERT_n	Alert signal	No external termination required (internally pulled-up to VDD with a 51Ω resistor).
Decoupling	High Speed Decoupling	The MCP incorporates some decoupling capacitors. For recommended external decoupling scheme please refer to the general user guide.
Bulk Decoupling	Low speed / low frequency	For recommended external decoupling scheme please refer to the general user guide.

Item	Description	Implementation Suggestion
Thermal	Thermal management	Customer should perform thermal simulation of device in application to determine appropriate thermal mitigation techniques required to ensure device case temperature maximum is not exceeded. Typical thermal mitigation techniques that may be required include heat sinks and/or PCB design enhancements such as thermal vias, heavier power and ground planes, etc.
Trace impedance	Impedance	Follow general user guide and JEDEC standard 21C DDR4 UDIMM Design specification.
Trace Lengths	Data Byte Lanes	Follow general user guide and JEDEC standard 21C DDR4 UDIMM Design specification.
Trace Lengths	Address & Command	Follow general user guide and JEDEC standard 21C DDR4 UDIMM Design specification.
Calibration	ZQ resistor for drive strength calibration	Nine individuals pull down 240Ω +/- 1% resistors are required, one per each ZQ pin (ZQ0…8).
BG1 - 8GB capacity support	Future migration to support 8GB capacity	BG1 is not used in Rev A memory design, however it is recommended to connect it to host memory controller for future compatibility with rev B memories.
Signal Integrity Simulation	End to End Simulation of all I/O signals	It is recommended to perform a signal integrity simulation on final layout design.
Simulation Model	MCP Package, Die Models	Simulation models are available on request.
Power consumption	Power calculation spreadsheet	Power calculation spreadsheet is available on request.
Thermal Simulation Model	MCP thermal model	Thermal simulation models are available on request.

Table 2: Migration from Rev A to Rev B

Signal	Implementation
BG1	To support future migration to Rev B part, this signal should be connected to the Host / Memory Controller. All other signals are applicable for both capacities. BG1 signal is not used in Rev A parts.
ZQ0 thru ZQ8	Calibration Reference - To support migration to Rev B part, connect all 9 ZQx signals to GND via 240Ω 1% Resistor and install them. ZQ1, ZQ3, ZQ5, ZQ7 signals are not used in Rev A parts.

1.4 Mapping of MCP signals to JEDEC DDR4 288pin UDIMM & DDR4 260 pin SO-DIMM signals.

For mapping of MCP signals to JEDEC DDR4 288pin UDIMM & DDR4 260 pin SO-DIMM signals, see 9 Appendix

1.5 DDR4 SPEED BINs and Timing Summary

Table 3: DDR4 SPEED BIN Nomenclature

Speed	Clock
DDR4-2133	1066 MHz
DDR4-2400	1200 MHz

Table 4: DDR4 Timing Summary

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR4-2133	0.93	15	14.06	14.06	33	47.05	15-15-15
DDR4-2400	0.83	17	14.16	14.16	32	46.16	17-17-17

Note:
(1) CL = CAS Latency, tRCD = Activate –to-Command Time, tRP = Precharge Time. Refer to Speed Bin tables for details.

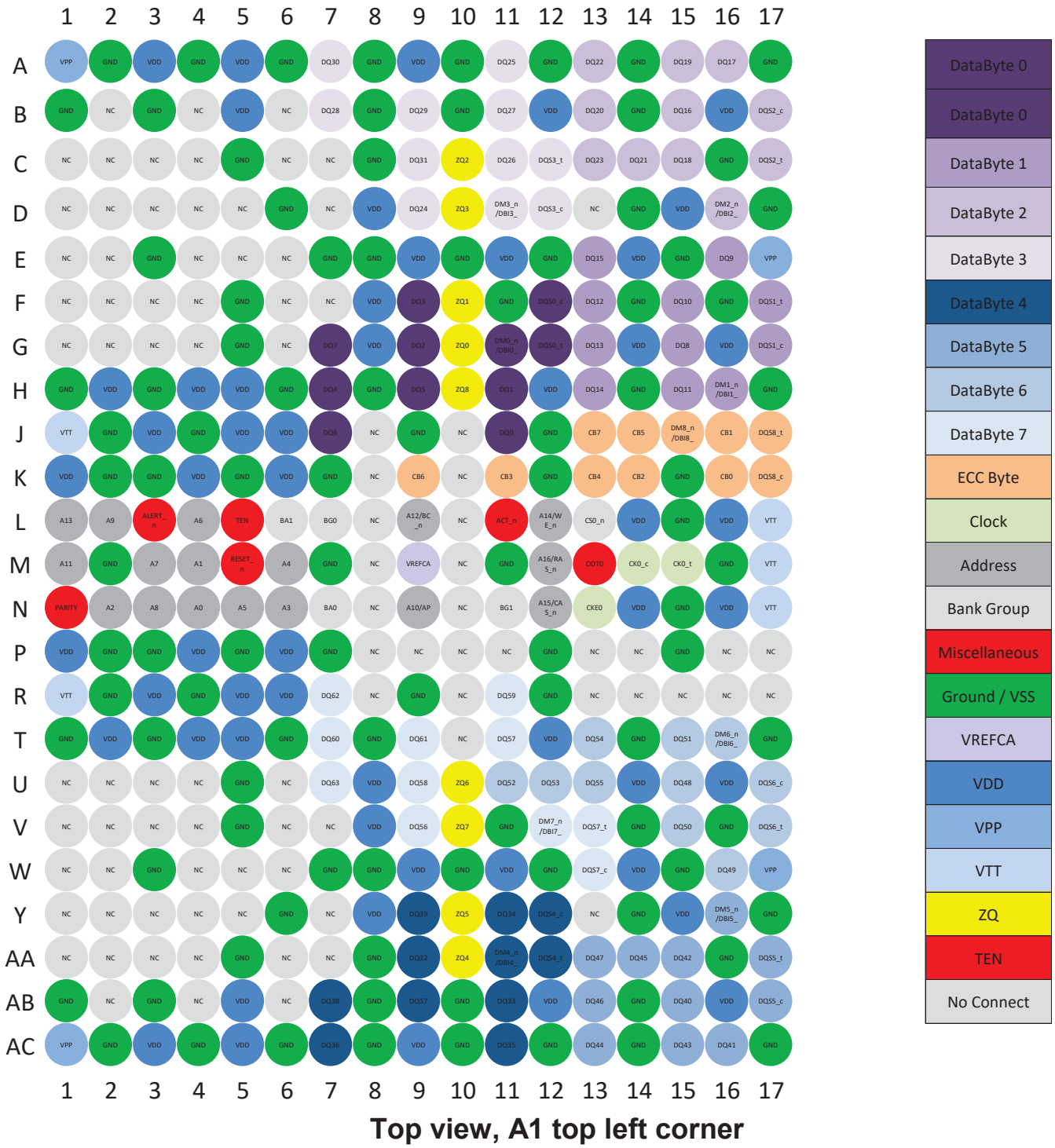
1.6 Addressing

Table 5: Addressing

		4GB Rev A: 512Mx72	4GB Rev B: 1024Mx72	8GB Rev B: 1024Mx72
Bank Address	# of Bank Groups	2	2	4
	BG Address	BG0 (BG1 is internally not connected)	BG0 (BG1 is not used)	BG0, BG1
	Bank Address in a BG	BA0 to BA1	BA0 to BA1	BA0 to BA1
Bank Count per Group		4	4	4
Row Address		64K (A0 to A15)	64K (A0 to A15)	64K (A0 to A15)
Column Address		1K (A0 to A9)	1K (A0 to A9)	1K (A0 to A9)
MCP Rank Address		CS0_n	CS0_n	CS0_n
Page size		2K	1K	1K

2 DDR4 MCP Ball Assignments

2.1 MCP Data Byte Ball Assignments (Rev A/ Rev B)



Top view, A1 top left corner

3 Ball Description

- Number of solder balls: 391
- Ball diameter: 0.4 mm
- Pitch: 0.80 mm
- Solder balls for leaded option: 63%Sn, 37%Pb
- Solder balls for Lead-free RoHS option: 96.5%Sn, 3%Ag, 0.5%Cu

Table 6: Ball Description

Symbol	Type	Function	Note
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.	
CKE0	Input	Clock Enable: CKE0 HIGH activates, and CKE0 Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE0 Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE0 is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE0, are disabled during power-down. Input buffers, excluding CKE0, are disabled during Self-Refresh.	1
CS0_n	Input	Chip Select: All commands are masked when CS0_n is registered HIGH. CS0_n provides for external Rank selection on systems with multiple Ranks. CS0_n is considered part of the command code.	1
ODT0	Input	On Die Termination: ODT0 (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT0 is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n, NU. For x16 configuration ODT0 is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT0 ball will be ignored if MR1 is programmed to disable RTT_NOM.	1
PARITY	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17;0], A10/AP, A12/BC_n, BA[1;0] and BG[1;0] with C0, C1 and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density and configuration specific should be treated internally as 0s by the DRAM pariy logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.	1
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS0_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.	1
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS0_n) define the command being entered. Those balls have multi-function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command balls for Read, Write and other command defined in command truth table.	1
DM_n/DBI_n, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.	
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. **Rev A (x16)** Has only BG0 (BG1 is internally not connected).	1

Symbol	Type	Function	Note
		Rev B (x8) If used in 8GB, BG0 and BG1 must be connected to the Host / Memory Controller. If used in 4GB BG1 can be connected to the Host / Memory Controller, or it can also be connected to the ground (should not be left floating).	
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.	1
A0-A13, A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is not used, left open or connected to ground.	1
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.	
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.	
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.	
DQ<63:00>	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0toDQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.	
CB<7:0>	Input / Output	Check Bit Input/ Output: Bi-directional ECC portion of data bus for x72 configurations	
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.	
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. This signal is internally pulled-up to VDD with a 51Ω resistor. No external resistor is required.	
TEN	Input	Boundary Scan Mode Enable: Required on x16 devices and optional input on x8 with densities equal to or greater than 8Gb. HIGH in this ball will enable boundary scan operation along with other balls. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.	
NC		No Connect: No internal electrical connection is present.	
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V	
GND	Supply	Ground	
VTT	Supply	Power Supply: 0.6 V +/- 3%	

Symbol	Type	Function	Note
Vpp	Supply	DRAM Activation Power Supply: 2.5V (2.375V min, 2.75 max)	
VREFCA	Supply	Reference voltage for CA	
ZQ	Supply	Reference Ball for ZQ calibration	

Note:

(1) No external termination required on the following balls: CK_t, CK_n, BG0-BG1, BA0-BA1, A0-A17, ACT_n, RAS_n,/A16, CAS_n/A15, WE_n/A14, PARITY, CS_n, CKE, ODT, ALERT_n.

4 MECHANICAL OUTLINE - PACKAGE DETAILS

4.1 Dimensions

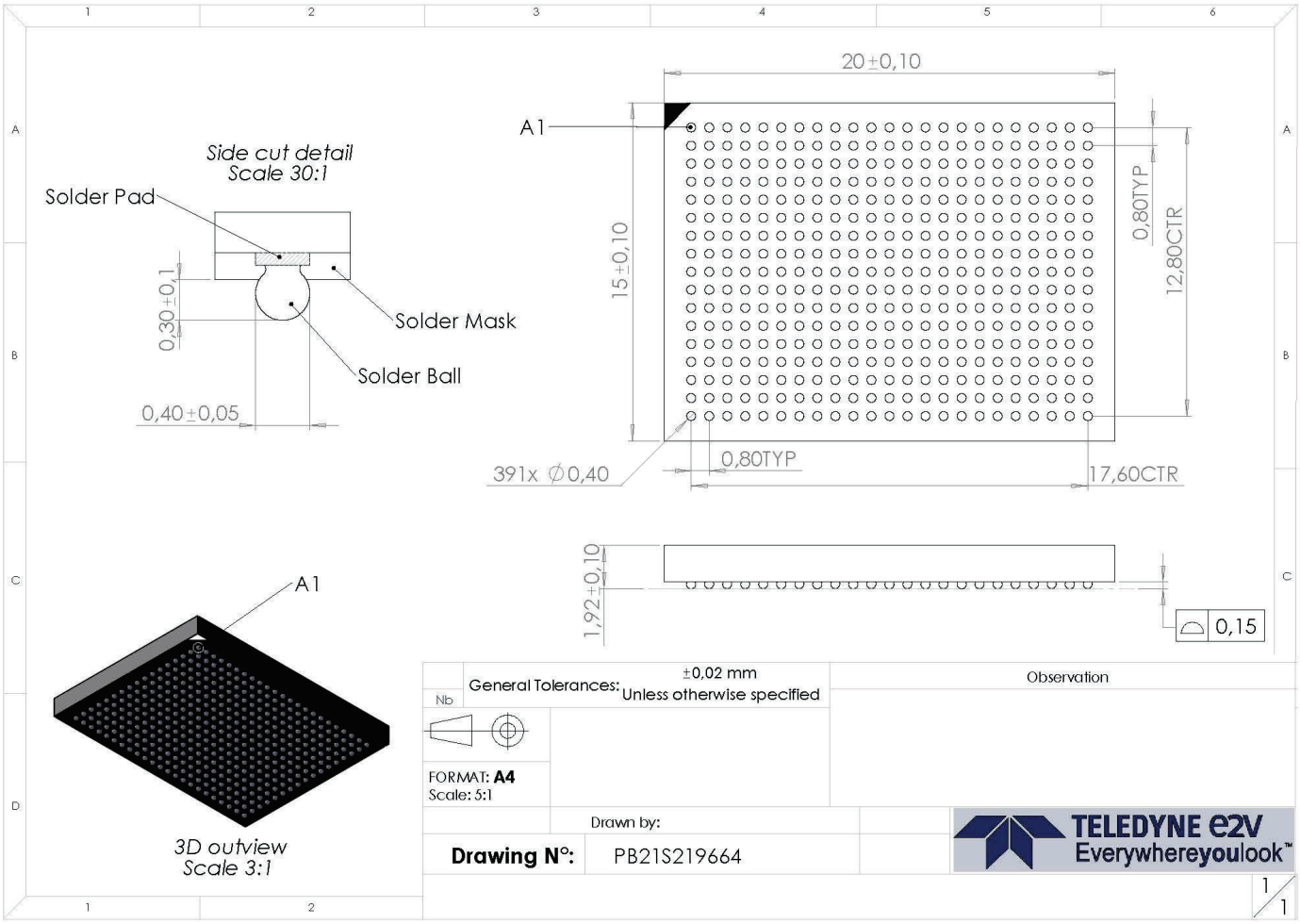


Figure 1: Mechanical Outline - Package Details

4.2 Weight

The weight is:

- Rev A parts: 1.18 grams
- Rev B parts: 1.27 grams

5 DDR4 MODE REGISTERS

5.1 Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MR*n*) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The MRS command cycle time, tMRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the tMRD Timing figure. Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don’t apply tMRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode,
- Per-DRAM addressability,
- Maximum power saving mode,
- CS to command/address latency,
- CA parity latency mode,
- VREFDQ training value,
- VREFDQ training mode,
- VREFDQ training range.

Some mode register settings may not be supported because they are not required by certain speed bins.

5.1.1 tMRD Timing Diagram

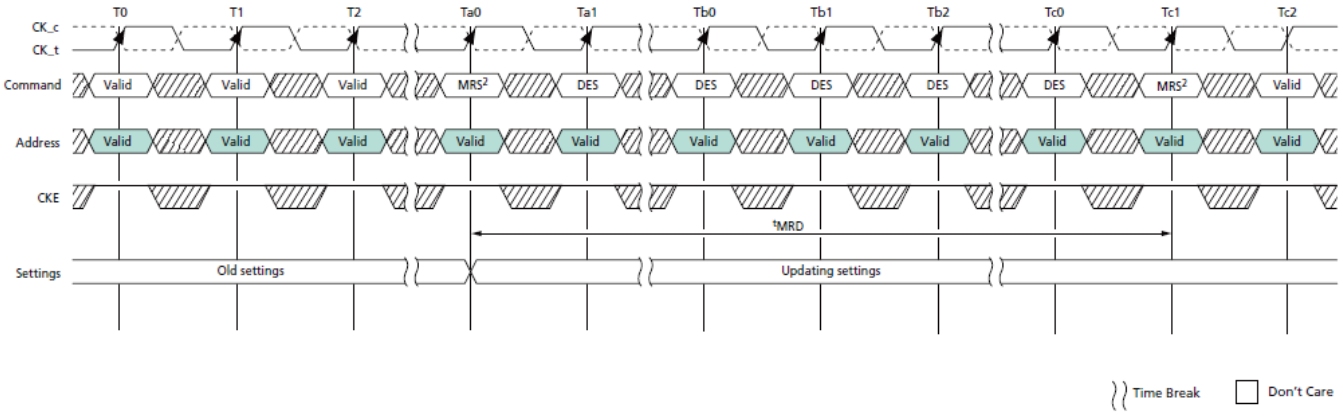


Figure 2: tMRD Timing

Notes:

(1) This timing diagram depicts CA parity mode “disabled” case.
(2) tMRD applies to all MRS commands with the following exceptions:
   a. Gear-down mode
   b. CA parity mode
   c. CAL mode
   d. Per-DRAM addressability mode
   e. VREFDQ training value, VREFDQ training mode, and VREFDQ training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET. tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the tMOD Timing figure.

5.1.2 tMOD Timing Diagram

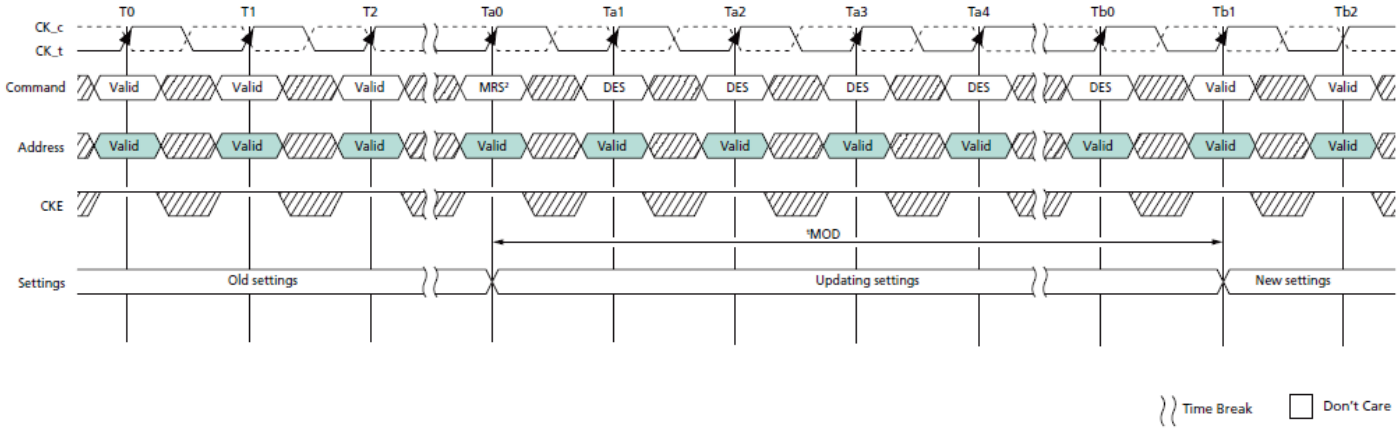


Figure 3: tMOD Timing

Notes:

(1) This timing diagram depicts CA parity mode “disabled” case.
(2) tMOD applies to all MRS commands with the following exceptions:
   a. DLL enable, Gear-down mode
   b. VREFDQ training value, internal VREF training monitor, VREFDQ training mode, and VREFDQ training range

c. Maximum power savings mode, Per-DRAM addressability mode, and CA parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the RTT(NOM) feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered HIGH after tMOD has expired. If the RTT(NOM) feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes. In some mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

5.2 MODE REGISTER 0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 7: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:
(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 8: MR0 Register Definition

Mode Register 0	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved

Mode Register 0	Description
13,11:9	**WR (WRITE recovery)/RTP (READ-to-PRECHARGE)** 0000 = 10 / 5 clocks1 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks1 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks1 0101 = 20 /10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks1 1000 = 26 / 13 clocks1 1001 through 1111 = Reserved
8	**DLL reset** 0 = No 1 = Yes
7	**Test mode (TM) – Manufacturer use only** 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	**CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out** 00000 = 9 clocks(1) 00001 = 10 clocks 00010 = 11 clocks(1) 00011 = 12 clocks 00100 = 13 clocks(1) 00101 = 14 clocks 00110 = 15 clocks(1) 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks(1) 01101 = 17 clocks(1) 01110 = 19 clocks(1) 01111 = 21 clocks(1) 10000 = 25 clocks (3DS use only) 10001 = 26 clocks 10010 = 27 clocks (3DS use only) 10011 = 28 clocks 10100 = 29 clocks(1) 10101 = 30 clocks 10110 = 31 clocks(1) 10111 = 32 clocks
3	**Burst type (BT) – Data burst ordering within a READ or WRITE burst access** 0 = Nibble sequential 1 = Interleave
1:0	**Burst length (BL) – Data burst size associated with each read or write access** 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

Note:
(1) Not allowed when 1/4 rate gear-down mode is enabled.

5.2.1 Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 9: Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

Notes:

(1) Applies to the entire table: 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
(2) When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for tWR and tWTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
(3) T = Output driver for data and strobes are in High-Z.
V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X = “Don’t Care.”

5.2.2 CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

5.2.3 Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No perations or functionality is specified if MR0[7] = 1.

5.2.4 Write Recovery(WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing t_{WR} (in ns) by tCK (in ns) and rounding up to the next integer: WR (MIN) cycles = roundup (t_{WR} [ns]/tCK[ns]). The WR value must be programmed to be equal to or larger than t_{WR} (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; t_{WR} values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data. Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer: RTP (MIN) cycles = roundup (tRTP[ns]/tCK[ns]). The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

5.2.5 DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, tDLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example,).

5.3 MODE REGISTER 1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 10: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 11: MR1 Register Definition

Mode Register 1	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5

Mode Register 1	Description
	110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) 1 = Disabled (both ODI and RTT)
11	Not used
10:8	**Nominal ODT (RTT(NOM) – Data bus termination setting (Zq=240 Ω)** 000 = RTT(NOM) disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ/1 (240 Ω) 101 = RZQ/5 (48 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)
7	**Write leveling (WL) – Write leveling mode** 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
13, 6, 5	**RFU** 000 = Default, must be programmed to 0 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 11 10 = CL - 2 11 = Reserved
2, 1	**Output driver impedance (ODI) – Output driver impedance setting (Zq=240 Ω)** 00 = RZQ/7 (34 Ω) 01 = RZQ/5 (48 Ω) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 Ω) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

5.3.1 DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for

synchronization to occur may result in a violation of the tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when RTT(WR) is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode. The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set RTT(WR), MR2[10:9] = 00.

5.3.2 Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

5.3.3 ODT RTT(NOM) Values

The device can provide three different termination values: RTT(Static), RTT(NOM), and RTT(WR). The nominal termination value, RTT(NOM), is programmed in MR1. A separate value, RTT(WR), may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITE operations. The RTT(WR) value can be applied during WRITE commands even when RTT(NOM) is disabled. A third RTT value, RTT(Static), is programmed in MR5. RTT(Static) provides a termination value when the ODT signal is LOW.

5.3.4 Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 12: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note:
(1) AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

5.3.5 Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

5.3.6 Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring MCP power. For normal operation, set MR1[12] to 0.

5.4 MODE REGISTER 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 13: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:
(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 14: MR2 Register Definition

Mode Register 2	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**TRR mode** 0 = Disabled 1 = Enabled
12	**WRITE data bus CRC** 0 = Disabled 1 = Enabled
11:9	**Dynamic ODT (RTT(WR)) – Data bus termination setting during WRITE (Zq=240 Ω)** 000 = RTT(WR) disabled (WRITE does not affect RTT value) 001 = RZQ/2 (120 Ω) 010 = RZQ/1 (240 Ω) 011 = High-Z 100 = RZQ/3 (80 Ω) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (TC: 0°C–85°C) 01 = Manual mode - Reduced operating temperature range (TC: 0°C–45°C) 10 = Manual mode - Extended operating temperature range (TC: 0°C–95°C) 11 = ASR mode - Automatically switching among all modes

Mode Register 2	Description
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1tCK WRITE preamble** 000 = 9 (DDR4-1600)(1) 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600)(1) 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933/3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933/3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2tCK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933/3200/2666) 111 = 20 (DDR4-2933/3200)
8, 2	**TRR mode - BGn control** 00 = BG0 01 = BG1 10 = BG2 11 = BG3
1:0	**TRR mode - BAn control** 00 = BA0 01 = BA1 10 = BA2 11 = BA3

Note:
(1) Not allowed when 1/4 rate gear-down mode is enabled.

5.4.1 CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

5.4.2 Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

5.4.3 Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT (RTT(WR)) settings in MR2[11:9]. In write leveling mode, only RTT(NOM) is available.

5.4.4 Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

5.4.5 Target Row Refresh Mode

For the device, rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (tMAW) before the adjacent rows need to be refreshed regardless of how the activates are distributed over tMAW. The row receiving the excessive activates is the target row (TR*n*); the two adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TR*n*, either the device must receive (roundup of tMAW / tREFI) REFRESH commands (REF) before another row activate is issued, or it needs to be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TR*n* that encountered the MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the activates from two target rows on a victim row should not exceed the MAC value as well. When the temperature controlled refresh (TCR) mode is enabled, tMAW should be adjusted depending on the TCR range as shown in the following table. Using TRR mode is not required, and in some cases has been rendered inoperable, as the device automatically performs TRR Mode in the background.

5.5 MODE REGISTER 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 15: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:
(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 16: MR3 Register Definition

Mode Register 3	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU

Mode Register 3	Description
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:11	**Multipurpose register (MPR) – Read format** 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	**WRITE CMD latency when CRC/DM enabled** 00 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400) 10 = 6CK (DDR4-2666/2933/3200) 11 = Reserved
8:6	**Fine granularity refresh mode 000 = Normal mode (fixed 1x)** 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	**Temperature sensor status** 0 = Disabled 1 = Enabled
4	**Per-DRAM addressability** 0 = Normal operation (disabled) 1 = Enable
3	**Gear-down mode – Ratio of internal clock to external data rate** 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	**Multipurpose register (MPR) access** 0 = Normal operation 1 = Data flow from MPR
1:0	**MPR page select** 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

5.5.1 Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MRn registers,
- WRITE and READ system patterns used for data bus calibration,
- Readout of the error frame when the command address parity feature is enabled.

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled,

any subsequent RD or RDA commands will be redirected to a specific mode register. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

5.5.2 WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled.

5.5.3 Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

5.5.4 Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

5.5.5 Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

5.5.6 Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

5.6 MODE REGISTER 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 17: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 18: MR4 Register Definition

Mode Register 4	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**Post Package Repair (PPR mode)** 0 = Disabled 1 = Enabled
12	**WRITE preamble setting** 0 = 1tCK toggle1 1 = 2tCK toggle
11	**READ preamble setting** 0 = 1tCK toggle1 1 = 2tCK toggle (When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.)
10	**READ preamble training** 0 = Disabled 1 = Enabled
9	**Self refresh abort mode** 0 = Disabled 1 = Enabled
8:6	**CMD (CAL) address latency** 000 = 0 clocks (disabled) 001 =3 clocks1 010 = 4 clocks 011 = 5 clocks1 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	**Soft Post Package Repair (sPPR mode)** 0 = Disabled 1 = Enabled
4	**Internal VREF monitor** 0 = Disabled 1 = Enabled
3	**Temperature controlled refresh mode** 0 = Disabled 1 = Enabled

Mode Register 4	Description
2	**Temperature controlled refresh range** 0 = Normal temperature mode 1 = Extended temperature mode
1	**Maximum power savings mode** 0 = Normal operation 1 = Enabled
0	**RFU** 0 = Must be programmed to 0 1 = Reserved

Note:
(1) Not allowed when 1/4 rate gear-down mode is enabled.

5.6.1 Post Package Repair Mode

The post package repair (PPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether PPR mode is available (A7 = 1) or not available (A7 = 0). PPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is irrevocable so great care should be exercised when using.

5.6.2 Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is revocable by either doing a reset or power-down.

5.6.3 WRITE Preamble

Programmable WRITE preamble, t_{WPRE}, can be set to 1tCK or 2tCK via the MR4 register. The 1tCK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

5.6.4 READ Preamble

Programmable READ preamble tRPRE can be set to 1tCK or 2tCK via the MR4 register. Both the 1tCK and 2tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

5.6.5 READ Preamble Training

Programmable READ preamble training can be set to 1tCK or 2tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

5.6.6 Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

5.6.7 Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCK(ns)/tCAL(ns)].

5.6.8 Internal VREF Monitor

The device generates its own internal VREFDQ. This mode may be enabled during VREFDQ training, and when enabled, VREF,time-short and VREF,time-long need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

5.6.9 Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

5.7 MODE REGISTER 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 19: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 20: MR5 Register Definition

Mode Register 5	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved

Mode Register 5	Description
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled 1 = Enabled
10	**Data mask (DM)** 0 = Disabled 1 = Enabled
9	**CA parity persistent error mode** 0 = Disabled 1 = Enabled
8:6	**Parked ODT value (RTT(Park))** **(Zq=240 Ω)** 000 = RTT(Park) disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ/1 (240 Ω) 101 = RZQ/5 (48 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)
5	**ODT input buffer for power-down** 0 = Buffer enabled 1 = Buffer disabled
4	**CA parity error status** 0 = Clear 1 = Error
3	**CRC error status** 0 = Clear 1 = Error
2:0	**CA parity latency mode** 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400)(1) 011 = 6 clocks (DDR4-2666) 100 = 8 clocks (DDR4-2933/3200) 101 = Reserved 110 = Reserved 111 = Reserved

Note:
(1) Not allowed when 1/4 rate gear-down mode is enabled.

5.7.1 Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device. The DBI function shares a common pin with the DM. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

5.7.2 Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device. The DM function shares a common pin with the DBI function. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled.

5.7.3 CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

5.7.4 ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide RTT(NOM) termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

5.7.5 CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

5.7.6 CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

5.7.7 CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16 , CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

5.8 MODE REGISTER 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 21: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

(1) RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 22: MR6 Register Definition

Mode Register 6	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**NA on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
12:10	**tCCD_L** 000 = 4 clocks (≤1333 Mb/s) 001 = 5 clocks (>1333 Mb/s and ≤1866 Mb/s) 010 = 6 clocks (>1866 Mb/s and ≤2400 Mb/s) 011 = 7 clocks (>2400 Mb/s and ≤2666 Mb/s) 100 = 8 clocks (>2666 Mb/s and ≤3200 Mb/s) 101 = Reserved 110 = Reserved 111 = Reserved
13, 9, 8	**RFU** 000 = Default, must be programmed to 000 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
7	**VREF Calibration Enable** 0 = Disable 1 = Enable
6	**VREF Calibration Range** 0 = Range 1 1 = Range 2
5:0	**VREF Calibration Value** See the VREFDQ Range and Levels table in the VREFDQ Calibration section

5.8.1 t_{CCD_L} Programming

The device controller must program the correct t_{CCD_L} value. t_{CCD_L} will be programmed according to the value defined per operating frequency in the AC parameter table. Although JEDEC specifies the larger of 5nCK or Xns, Micron's DRAM supports the larger of 4nCK or Xns.

5.8.2 VREFDQ Calibration Enable

VREFDQ calibration is where the device internally generates its own VREFDQ to be used by the DQ input receivers. The VREFDQ value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and

calibrating the internal VREFDQ level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ calibration must be used whenever values are being written to the MR6[6:0] register.

5.8.3 VREFDQ Calibration Range

The device defines two VREFDQ calibration ranges: Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDD while Range 2 supports VREFDQ between 45% and 77% of VDD, as seen in VREFDQ Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

5.8.4 VREFDQ Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ, as seen in VREFDQ Range and Levels table in the VREFDQ Calibration section.

6 DQ Internal Vref Specifications

6.1 VREFDQ Calibration and Training

The VREFDQ level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via VREFDQ calibration mode. If PDA or PPR modes are used prior to VREFDQ calibration, VREFDQ should initially be set at the midpoint between the VDD,max, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for VREFDQ calibration to determine the best internal VREFDQ level. The VREFDQ calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of VDD) or Range 2 (45% to 77.5% of VDD), and an MRS protocol using MR6[5:0] to adjust the VREFDQ level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is disabled. The DRAM controller will likely use a series of writes and reads in conjunction with VREFDQ adjustments to obtain the best VREFDQ, which in turn optimizes the data eye. The internal VREFDQ specification parameters are voltage range, step size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for DDR4 SDRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

6.1.1 VREFDQ Voltage Range

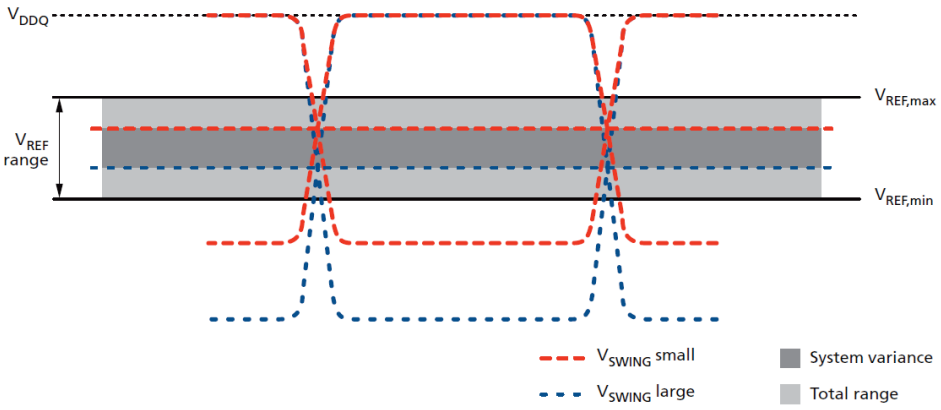


Figure 4: VREFDQ Voltage Range

6.1.2 VREFDQ Range and Levels

Table 23: VREFDQ Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 011 to 11 1111 = Reserved		

6.1.3 VREFDQ Step Size

The VREF step size is defined as the step size between adjacent steps. VREF step size ranges from 0.5% VDD to 0.8% VDD. However, for a given design, the device has one value for VREF step size that falls within the range. The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n. The VREF set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX VREF value endpoints for a specified range. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

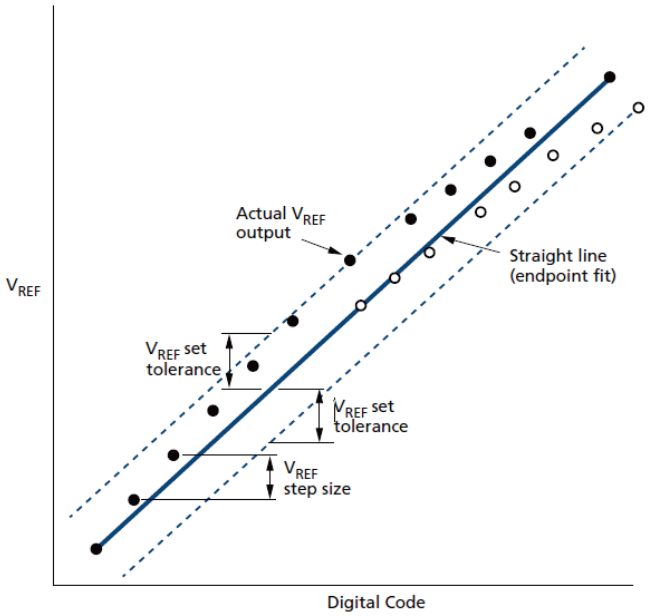


Figure 5: Example of VREF Set Tolerance and Step Size

Note:

(1) Maximum case shown.

6.1.4 VREFDQ Increment and Decrement Timing

The VREF increment/decrement step times are defined by VREF,time. VREF,time is defined from t0 to t1, where t1 is referenced to the VREF voltage at the final DC level within the VREF valid tolerance (VREF,val_tol). The VREF valid level is defined by VREF,val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment.

Note:

(1) t0 is referenced to the MRS command clock
(2) t1 is referenced to VREF,tol

6.1.4.1 VREFDQ Timing Diagram for VREF,time Parameter

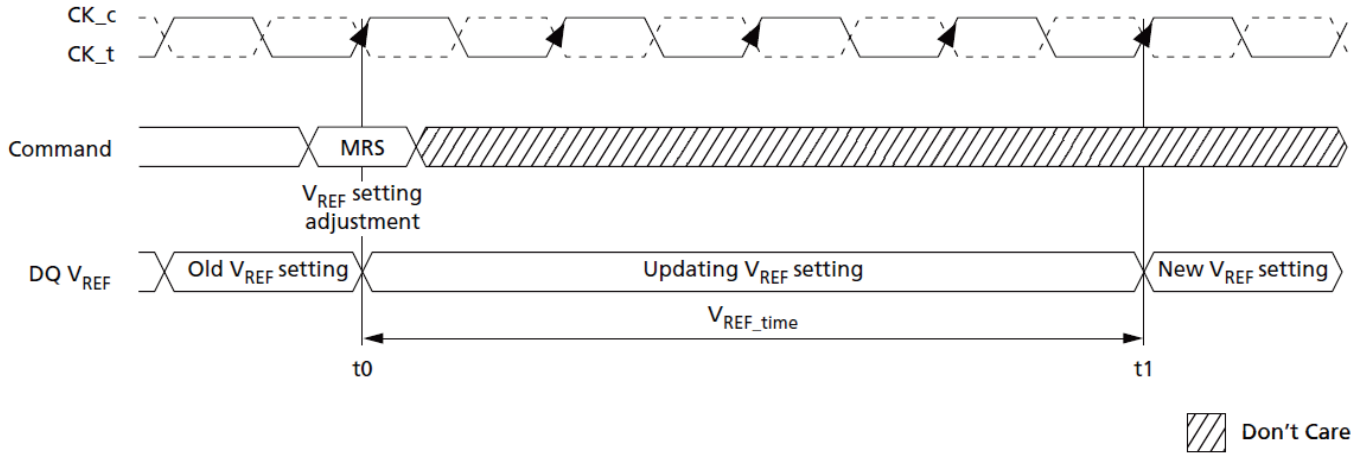


Figure 6: VREFDQ Timing Diagram for VREF,time Parameter

VREFDQ calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables VREFDQ calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After VREFDQ calibration mode has been entered, VREFDQ calibration mode legal commands may be issued once tVREFDQE has been satisfied. Legal commands for VREFDQ calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set VREFDQ values, and MRS to exit VREFDQ calibration mode. Also, after VREFDQ calibration mode has been entered, “dummy” WRITE commands are allowed prior to adjusting the VREFDQ value the first time VREFDQ calibration is performed after initialization. Setting VREFDQ values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired VREFDQ values. If MR6[7] is set to 0, MR6[6:0] are not written. VREF,time-short or VREF,time-long must be satisfied after each MR6 command to set VREFDQ value before the internal VREFDQ value is valid. If PDA mode is used in conjunction with VREFDQ calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only VREFDQ calibration mode legal commands noted above that may be used are the MRS commands: MRS to set VREFDQ values and MRS to exit VREFDQ calibration mode.

The last MR6[6:0] setting written to MR6 prior to exiting VREFDQ calibration mode is the range and value used for the internal VREFDQ setting. REFDQ calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit VREFDQ calibration mode has been issued, DES must be issued until tVREFDQX has been satisfied where any legal command may then be issued. VREFDQ setting should be updated if the die temperature changes too much from the calibration temperature.

The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 1:

- MR6[7:6]10 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).
- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]10 [5:0]VVVVVV.
- "VVVVVV" are desired settings for VREFDQ.
- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]10 [5:0]VVVVVV(1) where VVVVVV(1) = desired value for VREFDQ.

- MR6[7]0 [6:0]XXXXXXX to exit VREFDQ calibration mode.

The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 2:

- MR6[7:6]11 [5:0]XXXXXXX.
- Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).

- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]11[5:0]VVVVVV.
- "VVVVVV" are desired settings for VREFDQ.
- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]11 [5:0]VVVVVV(1) where VVVVVV(1) = desired value for VREFDQ.
  - MR6[7:6]11 [5:0]XXXXXXX to exit VREFDQ calibration mode.

Note:

(1) Range may only be set or changed when entering VREFDQ calibration mode; changing range while in or exiting VREFDQ calibration mode is illegal.

6.1.4.2 VREFDQ Training Mode Entry and Exit Timing Diagram

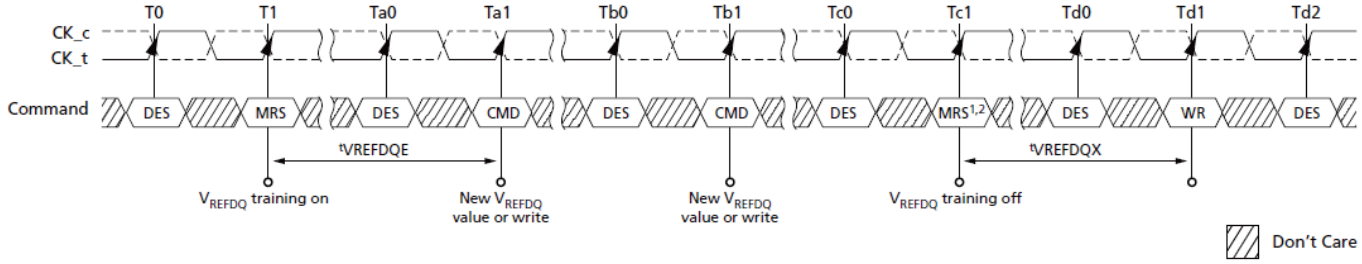


Figure 7: VREFDQ Trainning Mode Entry and Exit Timing Diagram

Notes:

(1) New VREFDQ values are not allowed with an MRS command during calibration mode entry.
(2) Depending on the step size of the latest programmed VREF value, VREF must be satisfied before disabling VREFDQ training mode.

6.1.4.3 VREF Step: Single Step Size Increment Case

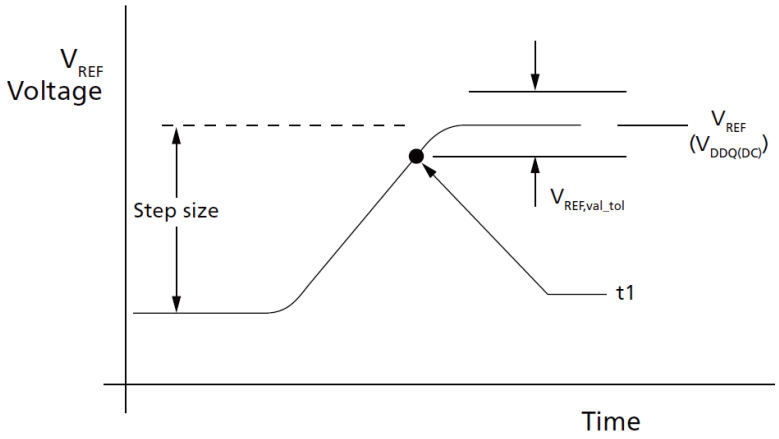


Figure 8: VREF Step: Single Step Size Increment Case

6.1.4.4 VREF Step: Single Step Size Decrement Case

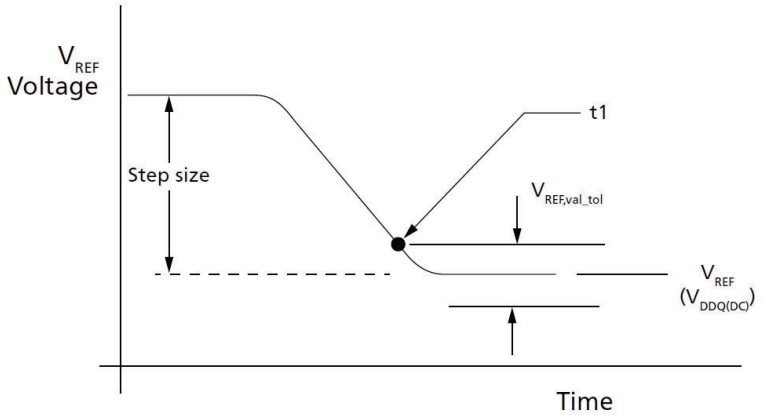


Figure 9: VREF Step:Single Step Size Decrement Case

6.1.4.5 VREF Full Step: From VREF,min to VREF,maxCase

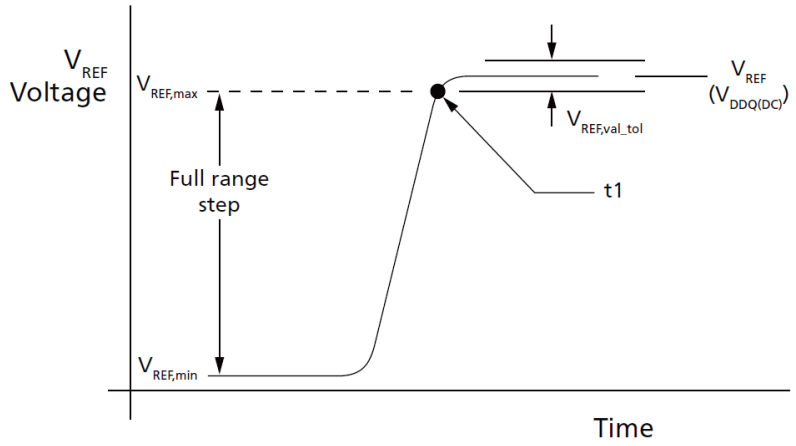


Figure 10: VREF Full Step: From VREF,min to VREF,max Case

6.1.4.6 VREF Full Step: From VREF,max to VREF,minCase

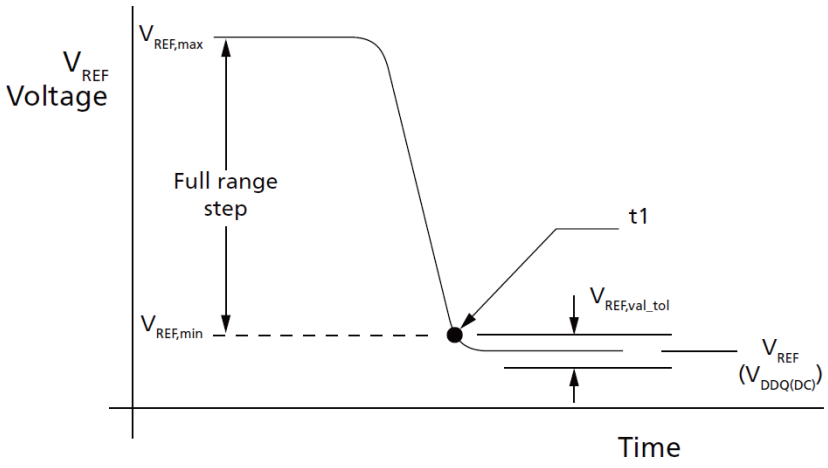


Figure 11:VREF Full Step: From VREF,max to VREF,min Case

6.1.5 VREFDQ Target Settings

The VREFDQ initial settings are largely dependents on the ODT termination settings. The table below shows all the possible initial settings available for VREFDQ training; it is unlikely the lower ODT settings would be used in most cases.

Table 24: VREFDQ Settings (VDD = 1.2V)

RON (Ω)	ODT (Ω)	Vx – VIN LOW (mV)	VREFDQ (mV)	VREFDQ (%VDD)
34	34	600	900	75%
	40	550	875	73%
	48	500	850	71%
	60	435	815	68%
	80	360	780	65%
	120	265	732	61%
	240	150	675	56%
48	34	700	950	79%
	40	655	925	77%
	48	600	900	75%
	60	535	865	72%
	80	450	825	69%
	120	345	770	64%
	240	200	700	58%

6.1.5.1 VREFDQ Equivalent Circuit

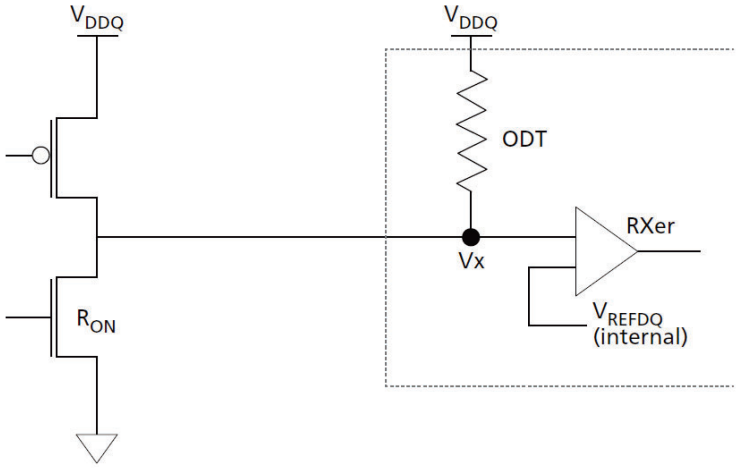


Figure 12: VREFDQ Equivalent Circuit

7 DC OPERATING CONDITIONS AND CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Table 25: Absolute maximum ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on any ball relative to GND	Vin, Vout	-0.4 to 1.5	V	1,
Voltage on VDD supply relative to GND	VDD	-0.4 to 1.5	V	1,3
Voltage on VPP supply relative to GND	VPP	-0.4 to 3.0	V	4
Storage temperature	Tstg	-55 to +150	°C	1,2

Notes:

(1) Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
(2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, refer to JESD51- 2 standard.
(3) VDD must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDD, When VDD are less than 500 mV; VREF may be equal to or less than 300 mV
(4) VPP must be equal or greater than VDD at all times
(5) Refer to JEDEC JC451 specification

7.2 Thermal considerations

7.2.1 MCP Component Operating Temperature Range

Table 26: DRAM Component Operating Temperature Range

Symbol	Temperature grade	Operating Temperature Tc / Tj	Units	Note
Toper	Normal Operating Temperature Range	T_c = 0 / T_j = 85	°C	1,2
	Extended Temperature Range	T_c = 0 / T_j = 85 and T_c = 0 / T_j = 95	°C	1,3
MCP operating temperature	Automotive A	T_c = -40 / T_j = 105	°C	
MCP operating temperature	Military M	T_c = -55 / T_j = 125	°C	

Notes:

(1) Operating Temperature TOPER is the case surface temperature on the center / top side of the MCP. For measurement conditions, refer to the JEDEC document JESD51-2.
(2) The Normal Temperature Range specifies the temperatures where all MCP specifications will be supported. During operation, the MCP case temperature must be maintained under all operating conditions.
(3) Some applications require operation of the MCP in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range.
b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range. Junction to case: Rjc = 3.7°C/W

7.2.2 tREFI by Temperature

Table 27: tREFI by Temperature

Parameter	Symbol		8Gb	Units
Average periodic refresh interval	tREFI	0°C ≤ Tcase ≤ 85°C (self/auto refresh)	7.8	µs
		85°C ≤ Tcase ≤ 95°C (see note 1)	3.9	µs
		95°C ≤ Tcase ≤ 105°C (manual refresh)	1.95	µs
		105°C ≤ Tcase ≤ 125°C (manual refresh)	0.4876	µs

Notes:

(1) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range.

(2) 8192 cycle refresh is

a. 64ms between 0 to 85°C
b. 32ms between 85 to 95°C
c. 16ms between 95 to 105°C
d. 4ms between 105 to 125°C

7.3 DC OPERATING VOLTAGE

Table 28: DC operating voltage (pod12)

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
VDD	Supply Voltage VDD: PC4:1.2V±5%,	1.14	1.2	1.26	V	1,2,3
VPP	2.5V +10%, -5%	2.375	2.5	2.75	V	3

Notes:

(1) JESD8-24 specifies Vref to be 70% of VDD.

(2) DC bandwidth is limited to 20MHz.,

(3) PODI2 1.2V Pseudo Open Drain Interface has a VDD value of 1.2V but the reference voltage allows PODI2 to be used with other VDD values. POD12 signals have pull-up-only parallel input termination and have an asymmetric output drive impedance. For example, if the output drivers were using a 60 Ω pull-up drive impedance then the pull-down drivers would be expected to produce a 40 Ω pull-down drive impedance. PODI2 does not explicitly call for series termination resistors, so it is suitable for point-to-point as well as multi-drop stub environments which may require some additional termination.

7.4 DDR4 power consumption

The DDR4 power consumption during normal operation strongly depends on the usage profile (transfer speed, write and read duty cycles, …). For this reason, it is not possible to provide power key figures fitting all applications. Teledyne e2v provides a power consumption estimation spreadsheet that should be used to estimate the power drawn by the DDR4 on D1_VDD and D1_VPP supplies. This power calculation tool is available upon request.

The maximum D1_VDD current consumed by the DDR4 memory during the initialization is provided in the following table:

Table 29 : Power consumption

Symbol	DDR4-2100	Unit
Iddinit: DDR4 initialization current on D1_VDD(1)	1600	mA
Ippinit: DDR4 initialization current on D1_Vpp(2)	N/S(2)	mA

Notes :

(1) Current during initialization of the DDR4 done by the LS1046A DDR4 controller during the boot of Qormino (ex: initialization under U-Boot). Maximum duration: 1s

(2) The initialization current on D1_VPP is not specified. It is lower or equal than the current drawn in normal operation, which can be estimated with the power consumption estimation spreadsheet.

D1_VTT corresponds to the termination voltage for the Address/Control/Command signals of the DDR4 (to which the integrated termination resistors are connected). The current on this supply can be either positive or negative, meaning that the voltage regulation must have sink and source capability. The maximum current on D1_VTT is reached when all Address/Control/Command signals are in the same state, and it is given in the next table.

VREFCA is not a supply, and it is used as a voltage reference. Its maximum leakage current is also provided in the table.

Table 30: Maximum leakage current

Supply	Maximum	Unit
D1_VTT	±223	mA
VREFCA 4GB Rev A	±10	µA
VREFCA 4GB / 8GB Rev B	±18	µA

Power supply sizing depends on the memory DDR4 controller. Teledyne e2v can't specify a value and users need to pay attention to this. Some typical power sizing examples are provided in the following table:

Table 31 Typical operating current on VDD depending on memory and DDR4 controller

Memory controller	DDR4	Power supply sizing
LS1046	4GB (Rev A)	1.2 A
	4/8GB (Rev B)	1.6 A
T1040	4GB (Rev A)	1.7 A
	4/8GB (Rev B)	1.9 A

8 AC OPERATING CONDITIONS AND CHARACTERISTICS

8.1 Speed Bins by Speed Grade

Table 32: DDR4-2133 Speed Bins and Operating Conditions

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	Min	Max		
Internal read command to first data			^{t}AA	14.06 (13.50)	19	ns	5
Internal read command to first data with read DBI enabled			^{t}AA_DBI	^{t}AA(min) + 3nCK	^{t}AA(max) + 3nCK	ns	
ACT to internal read or write delay time			^{t}RCD	14.06 (13.50)	-	ns	5
PRE command period			^{t}RP	14.06 (13.50)	-	ns	5
ACT to PRE command period			^{t}RAS	33	9 x ^{t}REFI	ns	
ACT to ACT or REF command period			^{t}RC	47.06 (46.50)	-	ns	5
	Normal	Read DBI					
CWL=9	CL=9	CL=11	^{t}CK(AVG)	Reserved		ns	1,2,3,4,6
	CL=10	CL=12		1.5	1.9		
CWL=9,11	CL=11	CL=13	^{t}CK(AVG)	Reserved		ns	1,2,3,4,5
	CL=12	CL=14		1.25	<1.5		
CWL=10,12	CL=13	CL=15	^{t}CK(AVG)	Reserved		ns	1,2,3,4,5
	CL=14	CL=16		1.071	<1.25		
CWL=11,14	CL=15	CL=18	^{t}CK(AVG)	Reserved		ns	1,2,3,4
	CL=16	CL=19		0.937	<1.071		
Supported CL Settings				10,12,14,16		nCK	7
Supported CL Settings with read DBI				12,14,16,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

Table 33: DDR4-2400 Speed Bins and Operating Conditions

Speed Bin			DDR4-2400		Unit	NOTE
CL-nRCD-nRP			17-17-17			
Parameter		Symbol	Min	Max		
Internal read command to first data		^tAA	14.16 (13.75)	19	ns	5
Internal read command to first data with read DBI enabled		^tAA_DBI	^tAA(min) + 3nCK	^tAA(max) + 3nCK	ns	
ACT to internal read or write delay time		^tRCD	14.16 (13.75)	-	ns	5
PRE command period		^tRP	14.16 (13.75)	-	ns	5
ACT to PRE command period		^tRAS	32	9 x ^tREFI	ns	
ACT to ACT or REF command period		^tRC	46.16 (45.75)	-	ns	5
	Normal	Read DBI				
CWL=9	CL=9	CL=11	$^tCK(AVG)$	Reserved	ns	1,2,3,4,6
	CL=10	CL=12		1.5	1.9	
CWL=9,11	CL=11	CL=13	$^tCK(AVG)$	1.25	<1.5	ns	1,2,3,4,5
	CL=12	CL=14					
CWL=10,12	CL=13	CL=15	$^tCK(AVG)$	1.071	<1.25	ns	1,2,3,4,5
	CL=14	CL=16					
CWL=11,14	CL=15	CL=18	$^tCK(AVG)$	0.937	<1.071	ns	1,2,3,4
	CL=16	CL=19					
CWL=12,16	CL=16	CL=19	$^tCK(AVG)$	Reserved	ns	1,2,3,4
	CL=17	CL=20		0.833	<0.937		
	CL=18	CL=21					
Supported CL Settings			10-18		nCK	7
Supported CL Settings with read DBI			12-16,18-21		nCK	
Supported CWL Settings			9-12,14,16		nCK	

Table 34: Timing Parameters for Speed Grades 2133 to 2400

Speed			DDR4-2133		DDR4-2400		Units	Note
Parameter		Symbol	MIN	MAX	MIN	MAX		
Clock Timing								
Clock period average (DLL off mode)		^{t}CK(DLL_OFF)	8	20	8	20	ns	
Average Clock Period		^{t}CK(avg,DLL_ON)	0.937	1.9	0.833	1.9	ns	3,13
Average high pulse width		^{t}CH(avg)	0.48	0.52	0.48	0.52	^{t}CK(avg)	
Average low pulse width		^{t}CL(avg)	0.48	0.52	0.48	0.52	^{t}CK(avg)	
Clock period jitter	Total	^{t}JITper_tot	-47	47	-42	42	ps	17,18
	Deterministic	^{t}JITper_dj	-23	23	-21	21	ps	17
	DLL locking	^{t}JITper_lck	-38	38	-33	33	Ps	
Absolute Clock Period		^{t}CK(abs)	^{t}CK(avg)min + ^{t}JIT(per)min_tot	^{t}CK(avg)max + ^{t}JIT(per)max_tot	^{t}CK(avg)min + ^{t}JIT(per) min_tot	^{t}CK(avg)max + ^{t}JIT(per)max_tot	ps	
Absolute clock HIGH pulse width		^{t}CH(abs)	0.45	-	0.45	-	^{t}CK(avg)	
Absolute clock Low pulse width		^{t}CL(abs)	0.45	-	0.45	-	^{t}CK(avg)	
Cycle to Cycle jitter	Total	^{t}JITcc_tot	-	94	-	83	ps	
	DLL locking	^{t}JITcc_lck	-	75	-	67	ps	
Cumulative error across	2 cycles	^{t}ERR(2per)	-69	69	-61	61	ps	
	3 cycles	^{t}ERR(3per)	-82	82	-73	73	ps	
	4 cycles	^{t}ERR(4per)	-91	91	-81	81	ps	
	5 cycles	^{t}ERR(5per)	-98	98	-87	87	ps	
	6 cycles	^{t}ERR(6per)	-104	104	-92	92	ps	
	7 cycles	^{t}ERR(7per)	-109	109	-97	97	ps	
	8 cycles	^{t}ERR(8per)	-113	113	-101	101	ps	
	9 cycles	^{t}ERR(9per)	-117	117	-104	104	ps	
	10 cycles	tERR(10per)	-120	120	-107	107	ps	
	11 cycles	^{t}ERR(11per)	-123	123	-110	110	ps	
	12 cycles	^{t}ERR(12per)	-126	126	-112	112	ps	
	n = 13,14…49, 50 cycles	^{t}ERR(nper)	^{t}ERR*n*per MAX = (1+0.68ln[n]) x ^{t}JITper_tot MAX		^{t}ERR*n*per MIN=(1+0.68ln[n]) x ^{t}JITper_tot MIN		ps	
DQ Input Timing								
Data setup time to DQS_t,DQS_c	Base (calibrated V_{REF})	^{t}DS	Approximately 0.15^{t}CK to 0.28^{t}CK				-	
	Non-calibrated V_{REF}	^{t}PDA_S	Minimum of 0.5UI				UI	22
Data hold time from DQS_t,DQS_c	Base (calibrated V_{REF})	^{t}DH	Approximately 0.15^{t}CK to 0.28^{t}CK				-	
	Non-calibrated V_{REF}	^{t}PDA_H	Minimum of 0.5UI				UI	33
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	-	0.58	-	UI	
DQ Output Timing (DLL enabled)								
DQS_t, DQS_c to DQ skew, per		^{t}DQSQ	-	0.16	-	0.17	UI	

Speed		DDR4-2133		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
gourp, per access							
DQ output hold time from DQS_t,DQS_c	^{t}QH	0.76	-	0.74	-	UI	
Data Valid Window per device: ^{t}QH-$^{t}DQSQ$ each device's output per UI	$^{1}DVW_{d}$	0.64	-	0.64	-	UI	
Data Valid Windo per device, per pin:^{t}QH-$^{t}DQSQ$ each device's output per UI	$^{t}DVW_{p}$	.69	-	0.72	-	UI	
DQ Low-Z time from CK_t,CK_c	$^{t}LZDQ$	-360	180	-330	175	ps	
DQ High-Z time form CK_t,CK_c	$^{t}HZDQ$	-	180	-	175	ps	
DQ Strobe Input Timing							
DQS_t,DQS_c rising edge to CK_t,CK_c rising edge for 1^{t}CKpreamble	$^{t}DQSS_{1ck}$	-0.27	0.27	-0.27	0.27	CK	
DQS_t,DQS_c rising edge to CK_t,CK_c rising edge for 2^{t}CKpreamble	$^{t}DQSS_{2ck}$	-0.50	0.50	-0.50	0.50	CK	
DQS_t,DQS_c differential input low pulse width	$^{t}DQSL$	0.46	0.54	0.46	0.54	CK	
DQS_t,DQS_c differential input high pulse width	$^{t}DQSH$	0.46	0.54	0.46	0.54	CK	
DQS_t,DQS_c falling edge setup to CK_t,CK_c rising edge	^{t}DSS	0.18	-	0.18	-	CK	
DQS_t,DQS_c falling edge hold from CK_t,CK_c rising edge	^{t}DSH	0.18	-	0.18	-	CK	
DQS_t,DQS_c differential WRITE preamble for 1^{t}CKpreamble	$^{t}WPRE_{1ck}$	0.9	-	0.9	-	CK	
DQS_t,DQS_c differential WRITE preamble for 2^{t}CKpreamble	$^{t}WPRE_{2ck}$	1.8	-	1.8	-	CK	
DQS_t,DQS_c differential WRITE postamble	$^{t}WPST$	0.33	-	0.33	-	CK	
DQS Strobe Output Timing (DLL enabled)							
DQS_t,DQS_c rising edge output access time from rising CK_t,CK_c	$^{t}DQSCK$	-180	180	-175	175	ps	
DQS_t,DQS_c rising edge output variance window per DRAM	$^{t}DQSCKi$	-	310	-	290	ps	
DQS_t,DQS_c differential output high time	^{t}QSH	0.4	-	0.4	-	CK	
DQS_t,DQS_c differential output low time	^{t}QSL	0.4	-	0.4	-	CK	
DQS_t,DQS_c Low-Z time (RL-1)	$^{t}LZDQS$	-360	180	-330	175	ps	
DQS_t,DQS_c High-Z time (RL-1)	$^{t}HZDQS$	-	180	-	175	ps	
DQS_t,DQS_c differential READ preamble for 1^{t}CKpreamble	$^{t}RPRE_{1ck}$	0.9	-	0.9	-	CK	20
DQS_t,DQS_c differential READ preamble for 2^{t}CKpreamble	$^{t}RPRE_{2ck}$	1.8	-	1.8	-	CK	20
DQS_t,DQS_c differential READ postamble	$^{t}RPST$	0.33	-	0.33	-	CK	21
Command and Address Timing							
DLL locking time	$^{t}DLLK$	768	-	768	-	CK	2,4
CMD, ADDR setup time to CK_t, CK_c Base	^{t}IS	80	0	62	-	ps	
CMD, ADDR setup time to CK_t, CK_c V_{REFCA}	$^{t}IS_{VREF}$	180	-	162	-	ps	

An Important Notice at the end of this datasheet addresses availability, warranty, changes, use in critical applications, intellectual property matters and other important disclaimers.

Speed			DDR4-2133		DDR4-2400		Units	Note
Parameter		Symbol	MIN	MAX	MIN	MAX		
referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$								
CMD, ADDR hold time to CK_t, CK_c Base referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$	Base	^{t}IH	105	-	87	-	ps	
	V_{REFCA}	$^{t}IH_{VREF}$	180	-	162	-	ps	
CTRL,ADDR pulse width for each input		^{t}IPW	460	-	410	-	ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD				ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP				ns	
ACTIVATE to PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS				ns	12
ACTIVATE to ACTIVATE or REFcommand period		^{t}RC	See Speed Bin Tables for ^{t}RC				ns	12
ACTIVATE to ACTIVATE or command period to different bank groups for Rev B		$^{t}RRD\_S$ (1KB)	MIN=greater of 4CK or 3.7ns		MIN=greater of 4CK or 3.3ns		CK	1
ACTIVATE to ACTIVATE or command period to different bank groups for Rev A		$^{t}RRD\_S$ (2KB)	MIN=greater of 4CK or 5.3ns		MIN=greater of 4CK or 5.3ns		CK	1
ACTIVATE to ACTIVATE or command period to same bank groups for Rev B		$^{t}RRD\_L$ (1KB)	MIN=greater of 4CK or 5.3ns		MIN=greater of 4CK or 4.9ns		CK	1
ACTIVATE to ACTIVATE or command period to same bank groups for Rev A		$^{t}RRD\_L$ (2KB)	MIN=greater of 4CK or 6.4ns		MIN=greater of 4CK or 6.4ns		CK	1
Four ACTIVATE windows for Rev B		^{t}FAW (1KB)	MIN=greater of 20CK or 21ns		MIN=greater of 20CK or 21ns		ns	
Four ACTIVATE windows for Rev A		^{t}FAW (2KB)	MIN=greater of 28CK or 30ns		MIN=greater of 28CK or 30ns		ns	
WRITE recovery time		^{t}WR	MIN = 15ns				ns	5,9,1
		$^{t}WR_2$	MIN = 1CK + ^{t}WR				CK	5,10,1
WRITE recovery time when CRC and DM are both enabled		$^{t}WR\_CRC\_DM$	MIN = ^{t}WR + greater of (5CK or 3.75ns)				CK	6,9,1
		$^{t}WR\_CRC\_DM_2$	MIN = 1CK + $^{t}WR\_CRC\_DM$				CK	6,10,1
Delay from start of internal WRITE transaction to internal READ command – Same bank group		$^{t}WTR\_L$	MIN = greater of 4CK or 7.5ns				CK	5,9,1
		$^{t}WTR\_L_2$	MIN = 1CK+$^{t}WTR\_L$				CK	5,10,1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled		$^{t}WTR\_L\_CRC\_DM$	MIN = $^{t}WTR\_L$ + greater of (5CK or 3.75ns)				CK	6,9,1
		$^{t}WTR\_L\_CRC\_DM_2$	MIN = 1CK + $^{t}WTR\_L\_CRC\_DM$				CK	6,10,1
Delay from start of internal WRITE transaction to internal READ command – different bank group		$^{t}WTR\_S$	MIN = greater of (2CK or 2.5ns)				CK	5,7,8,9,1
		$^{t}WTR\_S_2$	MIN = 1CK + $^{t}WTR\_S$				CK	5,7,8,10,1
Delay from start of internal WRITE transaction to internal READ command – different bank group when CRC and DM are both enabled		$^{t}WTR\_S\_CRC\_DM$	MIN = $^{t}WTR\_S$ + greater of (5CK or 3.75ns)				CK	6,7,8,9,1
		$^{t}WTR\_S\_CRC\_D_2$	MIN = 1CK + $^{t}WTR\_S\_CRC\_DM$				CK	6,7,8,10,1

Speed		DDR4-2133		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
READ to PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns				CK	1
CAS_n to CAS_n command delay to different bank group	^{t}CCD_S	4	-	4	-	CK	
CAS_n to CAS_n command delay to same bank group	^{t}CCD_L	MIN = greater of 4CK or 5.355ns	-	MIN = great er of 4CK or 5ns	-	CK	14
Auto precharge write recovery + precharge time	^{t}DAL (MIN)	MIN = WR + ROUND^{t}RP/^{t}CK (AVG); MAX=N/A				CK	8
MRS Command Timing							
MRS command cycle time	^{t}MRD	8	-	8	-	CK	
MRS command cycle time in PDA mode	^{t}MRD_PDA	MIN = greater of (16nCK, 10ns)				CK	1
MRS command cycle time in CAL mode	^{t}MRD_CAL	MIN=^{t}MOD + ^{t}CAL				CK	
MRS command update delay	^{t}MOD	MIN = greater of (24nCLK, 15ns)				CK	1
MRS command update delay in PDA mode	^{t}MOD_PDA	MIN = ^{t}MOD				CK	
MRS command update delay in CAL mode	^{t}MOD_CAL	MIN = ^{t}MOD + ^{t}CAL				CK	
MRS command to DGS drive in preamble training	^{t}SDO	MIN = ^{t}MOD + 9ns				ns	
MPR Command Timing							
Multipurpose register recovery time	^{t}MPRR	MIN = 1CK				CK	
Multipurpose register write recovery time	^{t}WR_MPR	MIN = ^{t}MOD + AL + PL					
CRC Error Reporting Timing							
CRC error to ALERT_n latency	^{t}CRC_ALERT	3	13	3	13	ns	
CRC Alert_n pulse width	^{t}CRC_ALERT_PW	6	10	6	10	CK	
Parity latency	PL	4	-	5	-	CK	
Command uncertain to be executed during this time	^{t}PAR_UNKNOWN	-	PL	-	PL	CK	
Delay from errant command to ALERT_n assertion	^{t}PAR_ALERT_ON	-	PL + 6ns	-	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	^{t}PAR_ALERT_PW	64	128	72	144	CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^{t}PAR_ALERT_RS_P	-	57	-	64	CL	
CAL Timing							
CS_n to command address latency	^{t}CAL	4	-	5	-	CK	19
CS_n to command address latency in gear-down mode	^{t}CALg	N/A	-	N/A	-	CK	
MPSM Timing							
Command path disable delay upon MPSM entry	^{t}MPED	MIN = ^{t}MOD (MIN) + ^{t}CPED (MIN)				CK	1
Valid clock requirement after MPSM entry	^{t}CKMPE	MIN = ^{t}MOD (MIN) + ^{t}CPED (MIN)				CK	1
Valid clock requirement after MPSM exit	^{t}CKMPX	MIN = ^{t}CKSRX (MIN)				CK	1
Exit MPSM to commands not requiring a locked DLL	^{t}XMP	^{t}XS (MIN)				CK	

Speed			DDR4-2133		DDR4-2400		Units	Note
Parameter		**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Exit MPSM to commands requiring a locked DLL		^{t}XMPDLL	MIN = ^{t}XMP (MIN) + ^{t}XSDLL (MIN)				CK	1
CS setup time to CKE		^{t}MPX_S	MIN – ^{t}IS (MIN) + ^{t}IH (MIN)				ns	
CS_n HIGH hold time to CKE rising edge		^{t}MPX_HH	MIN = ^{t}XP				ns	
CS_n LOW hold time to CKE rising edge		^{t}MPX_LH	12	^{t}XMP-10ns	12	^{t}XMP-10ns	ns	
Connectivity Test Timing								
TEN pin HIGH to CS_n LOW – Enter CT mode		^{t}CT_Enable	200	-	200	-	ns	
CS_n LOW and valid input to valid output		^{t}CT_Valid	-	200	-	200	ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		^{t}CTCKE_Valid	10	-	10	-	ns	
Calibration and V_{REFDQ} Train Timing								
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	1024	-	1024	-	CK	
	Normal operation	^{t}ZQoper	512	-	512	-	CK	
ZQCS command: Short calibration time		^{t}ZQCS	128	-	128	-	CK	
The V_{REF} increment/decrement step time		VREF_time	MIN = 150 ns				ns	
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		^{t}VREFDQE	MIN = 150 ns				ns	
Exit V_{REFDQ} training mode to the first write command delay		^{t}VREFDQX	MIN = 150 ns				ns	
Initialization and Reset Timing								
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC (MIN) + 10 ns				CK	1
RESET_L pulse low after power stable		^{t}PW_RESET_S	1.0	-	1.0	-	µs	
RESET_L pulse low at power up		^{t}PW_RESET_L	200	-	200	-	µs	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200				ms	
RESET_n LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 0				ns	
Refresh Timing								
Refresh to ACTIVATE or REFRESH command period (all banki groups)	4Gb	^{t}RFC1	MIN= 260				ns	1,11
		^{t}RFC2	MIN = 160				ns	1,11
		^{t}RFC4	MIN = 110				ns	1,11
	8Gb	^{t}RFC1	MIN = 350				ns	1,11
		^{t}RFC2	MIN = 260				ns	1,11
		^{t}RFC4	MIN = 160				ns	1,11
	16Gb	^{t}RFC1	MIN = 350				ns	1,11
		^{t}RFC2	MIN = 260				ns	1,11
		^{t}RFC4	MIN =160				ns	1,11
Average periodic refresh interval	-40°C ≤T_C≤85°C	^{t}REFI	MIN = N/A;MAX = 7.8				µs	11
	85°C≤T_C≤ 95°C	^{t}REFI	MIN = N/A;MAX = 3.9				µs	11

Speed			DDR4-2133		DDR4-2400		Units	Note
Parameter		Symbol	MIN	MAX	MIN	MAX		
	95°C≤T_C≤ 105°C	^{t}REFI	MIN = N/A;MAX = 1.95				µs	11
Self Refresh Timing								
Exit self refresh commands not requiring a locked DLL		^{t}XS	MIN= = ^{t}RFC + 10ns				ns	1
Exit self refresh commands not requiring a locked DLL in self refresh abort		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10ns				ns	1
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)		^{t}XS_FAST	MIN= ^{t}RFC4 + 10ns				ns	1
Exit self refresh commands requiring a locked DLL		^{t}XSDLL	MIN= ^{t}DLLK (MIN)				CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + 1*n*CK				CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled		^{t}CKESR_PAR	MIN = ^{t}CKE (MIN) + 1*n*CK + PL				CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)		^{t}CKSRE	MIN=greater of (5CK, 10ns)				CK,ns	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled		^{t}CKSRE_PAR	MIN = greater (5CK, 10ns) + PL				CK,ns	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit		^{t}CKSRX	MIN = greater of (5CK, 10ns)				CK,ns	1
Power-Down Timing								
Exit power-down with DLL on to any valid command		^{t}XP	MIN = greater of 4CK or 6ns				CK,ns	1
Exit power-down with DLL on to any valid command when CA parity is enabled		^{t}XP_PAR	MIN = (greater of 4CK or 6ns) + PL				CK,ns	1
CKE MIN pulse width		^{t}CKE (MIN)	MIN = greater of 3CK or 5ns				CK,ns	1
Command pass disable delay		^{t}CPDED	4	-	4	-	CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 x ^{t}REFI				CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL-1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC – REFRESH command to CKE LOW time				CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XSDLL				CK	
Power-Down Entry Minimum timing								
ACTIVATE command to power-down entry		^{t}ACTPDEN	2	-	2	-	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	2	-	2	-	CK	
REFRESH command to power-down entry		^{t}REFDEN	2	-	2	-	CK	
MRS command to power-down entry		^{t}MRSDEN	MIN= ^{t}MOD (MIN)				CK	1
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1				CK	1

Speed		DDR4-2133		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)				CK	1
WRITE command to power-down entry (BC4MRS)	^{t}WRPBC4DEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)				CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRAPDEN	MIN = WL + 4 + WR + 1				CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	^{t}WRAPBC4DEN	MIN = WL + 2 + WR + 1				CK	1
ODT Timing							
Direct ODT turn-on latency	DODTLon	WL -2 = CWL + AL + PL -2				CK	
Direct ODT turn-off latency	DODTLoff	WL -2 = CWL + AL + PL -2				CK	
R_{tt} dynamic change skew	^{t}ADC	0.3	0.7	0.3	0.7	CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	^{t}AONAS	1	9	1	9	ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	^{t}AOFAS	1	9	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1^{t}CK	6	-	6	-	CK	
	ODTH8 2^{t}CK	7	-	7	-		
ODT HIGH time without WRITE command or with WRITE command and BC8	ODTH4 1^{t}CK	4	-	4	-	CK	
	ODTH4 2^{t}CK	5	-	5	-		
Write Leveling Timing							
First DQS_t, DQS_c rising edge after write leveling mode is programmed	^{t}WLMRD	40	-	40	-	CK	
DQS_t, DQS_c delay after write leveling mode is programmed	^{t}WLDQSEN	25	-	25	-	CK	
Write leveling setup from rising CK_t. CK_c crossing ro rising DQS_t, DQS_c crossing	^{t}WLS	0.13	-	0.13	-	^{t}CK(avg)	
Write leveling hold from rising CK_t. CK_c crossing ro rising DQS_t, DQS_c crossing	^{t}WLH	0.13	-	0.13	-	^{t}CK(avg)	
Write leveling output delay	^{t}WLO	0	0.95	0	0.95	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	ns	

Notes:

(1) Start of internal write transaction is defined as follows:
   a. For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   b. For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   c. For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

(2) A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled

(3) Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

(4) tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

(5) WR in clock cycles as programmed in MR0.

(6) tREFI depends on TOPER.

(7) CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

(8) Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.

(9) For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

(10) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

(11) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

(12) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
(13) The max values are system dependent.
(14) DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.
(15) The deterministic component of the total timing.
(16) DQ to DQ static offset relative to strobe per group.
(17) This parameter will be characterized and guaranteed by design.
(18) When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output) Deratings are relative to the SDRAM input clock).
(19) DRAM DBI mode is off.
(20) DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
(21) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
(22) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
(23) There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
(24) tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
(25) tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
(26) Total jitter includes the sum of deterministic and random jitter terms for a specified BER.
(27) The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
(28) This parameter has to be even number of clocks
(29) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
(30) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
(31) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
(32) After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
(33) After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width). UI=tCK(avg).min/2

9 Appendix

9.1 Appendix A

The table below maps MCP signals to JEDEC DDR4 288 Pin UDIMM & 260 Pin SO-DIMM. The Table provides a cross reference between standard JEDEC signals and or Embedded Processor / Memory Controller and MCP sorted by functional groups. Rev A part is configured for x16 & Rev B part is configured for x8.

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
J11	DQ0	DataByte 0	5	DQ0	8	DQ0
H11	DQ1		150	DQ1	7	DQ1
G9	DQ2		12	DQ2	20	DQ2
F9	DQ3		157	DQ3	21	DQ3
H7	DQ4		3	DQ4	4	DQ4
H9	DQ5		148	DQ5	3	DQ5
J7	DQ6		10	DQ6	16	DQ6
G7	DQ7		155	DQ7	17	DQ7
G12	DQS0_t		153	DQS0_t	13	DQS0_t
F12	DQS0_c		152	DQS0_c	11	DQS0_c
G11	DM0_n		7	DM0_n, DBI0_n, NC	12	DM0_n, DBI0_n, NC
G15	DQ8	DataByte 1	16	DQ8	28	DQ8
E16	DQ9		161	DQ9	29	DQ9
F15	DQ10		23	DQ10	41	DQ10
H15	DQ11		168	DQ11	42	DQ11
F13	DQ12		14	DQ12	24	DQ12
G13	DQ13		159	DQ13	25	DQ13
H13	DQ14		21	DQ14	38	DQ14
E13	DQ15		166	DQ15	37	DQ15
F17	DQS1_t		164	DQS1_t	34	DQS1_t

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
G17	DQS1_c		163	DQS1_c	32	DQS1_c
H16	DM1_n		18	DM1_n, DBI1_n, NC	33	DM1_n, DBI1_n, NC
B15	DQ16	DataByte 2	27	DQ16	50	DQ16
A16	DQ17		172	DQ17	49	DQ17
C15	DQ18		34	DQ18	62	DQ18
A15	DQ19		179	DQ19	63	DQ19
B13	DQ20		25	DQ20	46	DQ20
C14	DQ21		170	DQ21	45	DQ21
A13	DQ22		32	DQ22	58	DQ22
C13	DQ23		177	DQ23	59	DQ23
C17	DQS2_t		175	DQS2_t	55	DQS2_t
B17	DQS2_c		174	DQS2_c	53	DQS2_c
D16	DM2_n		29	DM2_n, DBI2_n, NC	54	DM2_n, DBI2_n, NC
D9	DQ24	DataByte 3	38	DQ24	70	DQ24
A11	DQ25		183	DQ25	71	DQ25
C11	DQ26		45	DQ26	83	DQ26
B11	DQ27		190	DQ27	84	DQ27
B7	DQ28		36	DQ28	66	DQ28
B9	DQ29		181	DQ29	67	DQ29
A7	DQ30		43	DQ30	79	DQ30
C9	DQ31		188	DQ31	80	DQ31
C12	DQS3_t		186	DQS3_t	76	DQS3_t
D12	DQS3_c		185	DQS3_c	74	DQS3_c
D11	DM3_n		40	DM3_n, DBI3_n, NC	75	DM3_n, DBI3_n, NC
AA9	DQ32	DataByte 4	97	DQ32	174	DQ32
AB11	DQ33		242	DQ33	173	DQ33

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
Y11	DQ34		104	DQ34	187	DQ34
AC11	DQ35		249	DQ35	186	DQ35
AC7	DQ36		95	DQ36	170	DQ36
AB9	DQ37		240	DQ37	169	DQ37
AB7	DQ38		102	DQ38	183	DQ38
Y9	DQ39		247	DQ39	182	DQ39
AA12	DQS4_t		245	DQS4_t	179	DQS4_t
Y12	DQS4_c		244	DQS4_c	177	DQS4_c
AA11	DM4_n		99	DM4_n, DB14_N, NC	178	DM4_n, DB14_N, NC
AB15	DQ40	DataByte 5	108	DQ40	195	DQ40
AC16	DQ41		253	DQ41	194	DQ41
AA15	DQ42		115	DQ42	207	DQ42
AC15	DQ43		260	DQ43	208	DQ43
AC13	DQ44		106	DQ44	191	DQ44
AA14	DQ45		251	DQ45	190	DQ45
AB13	DQ46		113	DQ46	203	DQ46
AA13	DQ47		258	DQ47	204	DQ47
AA17	DQS5_t		256	DQS5_t	200	DQS5_t
AB17	DQS5_c		255	DQS5_c	198	DQS5_c
Y16	DM5_n		110	DM5_n, DB15_n, NC	199	DM5_n, DB15_n, NC
U15	DQ48	DataByte 6	119	DQ48	216	DQ48
W16	DQ49		264	DQ49	215	DQ49
V15	DQ50		126	DQ50	228	DQ50
T15	DQ51		271	DQ51	229	DQ51
U11	DQ52		117	DQ52	211	DQ52
U12	DQ53		262	DQ53	212	DQ53

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
T13	DQ54		124	DQ54	224	DQ54
U13	DQ55		269	DQ55	225	DQ55
V17	DQS6_t		267	DQS6_t	221	DQS6_t
U17	DQS6_c		266	DQS6_c	219	DQS6_c
T16	DM6_n		121	DM6_n, DB16_n, NC	220	DM6_n, DB16_n, NC
V9	DQ56	DataByte 7	130	DQ56	237	DQ56
T11	DQ57		275	DQ57	236	DQ57
U9	DQ58		137	DQ58	249	DQ58
R11	DQ59		282	DQ59	250	DQ59
T7	DQ60		128	DQ60	232	DQ60
T9	DQ61		273	DQ61	233	DQ61
R7	DQ62		135	DQ62	245	DQ62
U7	DQ63		280	DQ63	246	DQ63
V13	DQS7_t		278	DQS7_t	242	DQS7_t
W13	DQS7_c		277	DQS7_c	240	DQS7_c
V12	DM7_n		132	DM7_n, DB17_n, NC	241	DM7_n, DB17_n, NC
K16	CB0	ECC Byte	49	CB0, NC	92	CB0, NC
J16	CB1		194	CB1, NC	91	CB1, NC
K14	CB2		56	CB2, NC	101	CB2, NC
K11	CB3		201	CB3, NC	105	CB3, NC
K13	CB4		47	CB4, NC	88	CB4, NC
J14	CB5		192	CB5, NC	87	CB5, NC
K9	CB6		54	CB6, NC	100	CB6, NC
J13	CB7		199	CB7, NC	104	CB7, NC
J17	DQS8_t		197	DQS8_t	97	DQS8_t
K17	DQS8_c		196	DQS8_c	95	DQS8_c

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
J15	DM8_n		51	DM8_n, DBI8_n, NC	96	DM8_n, DBI8_n, NC
M15	CK0_t	Clock	74	CK0_t	137	CK0_t
M14	CK0_c		75	CK0_c	139	CK0_c
N13	CKE0		60	CKE0	109	CKE0
N4	A0	Address	79	A0	144	A0
M4	A1		72	A1	133	A1
N2	A2		216	A2	132	A2
N6	A3		71	A3	131	A3
M6	A4		214	A4	128	A4
N5	A5		213	A5	126	A5
L4	A6		69	A6	127	A6
M3	A7		211	A7	122	A7
N3	A8		68	A8	125	A8
L2	A9		66	A9	121	A9
N9	A10/AP		225	A10/AP	146	A10/AP
M1	A11		210	A11	120	A11
L9	A12		65	A12/BC_n	119	A12
L1	A13		232	A13	158	A13
L12	A14/WE_n		228	WE_n/A14	151	A14/WE_n
N12	A15/CAS_n		86	CAS_n/A15	156	A15/CAS_n
M12	A16/RAS_n		82	RAS_n/A16	152	A16/RAS_n
N7	BA0	Bank Group	81	BA0	150	BA0
L6	BA1		224	BA1	145	BA1
L7	BG0		63	BG0	115	BG0

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
N11	BG1	Connect to Processor / Memory Controller for future migration from 4GB to 8GB MCP	207	BG1	113	BG1
L13	CS0_n		84	CS0_n	149	CS0_n
L11	ACT_n	Miscellaneous	62	ACT_n	114	ACT_n
L3	ALERT_n		208	ALERT_n	116	ALERT_n
M13	ODT0		87	ODT0	155	ODT0
N1	PARITY		222	PARITY	143	PARITY
M5	RESET_n		58	RESET_n	108	RESET_n
A2	GND	Ground / VSS	2	VSS	1	VSS
A4	GND		4	VSS	2	VSS
A6	GND		6	VSS	5	VSS
A8	GND		9	VSS	6	VSS
A10	GND		11	VSS	9	VSS
A12	GND		13	VSS	10	VSS
A14	GND		15	VSS	14	VSS
A17	GND		17	VSS	15	VSS
AA5	GND		259	VSS	230	VSS
AA8	GND		261	VSS	231	VSS
AA16	GND		263	VSS	234	VSS
AB1	GND		265	VSS	235	VSS
AB3	GND		268	VSS	238	VSS
AB8	GND		270	VSS	239	VSS
AB10	GND		272	VSS	243	VSS
AB14	GND		274	VSS	244	VSS
AC2	GND		276	VSS	247	VSS

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AC4	GND		279	VSS	248	VSS
AC6	GND		281	VSS	251	VSS
AC8	GND		283	VSS	252	VSS
AC10	GND		20	VSS	18	VSS
AC12	GND		22	VSS	19	VSS
AC14	GND		24	VSS	22	VSS
AC17	GND		26	VSS	23	VSS
B1	GND		28	VSS	26	VSS
B3	GND		31	VSS	27	VSS
B8	GND		33	VSS	30	VSS
B10	GND		35	VSS	31	VSS
B14	GND		37	VSS	35	VSS
C5	GND		39	VSS	36	VSS
C8	GND		42	VSS	39	VSS
C16	GND		44	VSS	40	VSS
D6	GND		46	VSS	43	VSS
D14	GND		48	VSS	44	VSS
D17	GND		50	VSS	47	VSS
E3	GND		53	VSS	48	VSS
E7	GND		55	VSS	51	VSS
E8	GND		57	VSS	52	VSS
E10	GND		94	VSS	56	VSS
E12	GND		96	VSS	57	VSS
E15	GND		98	VSS	60	VSS
F5	GND		101	VSS	61	VSS
F11	GND		103	VSS	64	VSS

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
F14	GND		105	VSS	65	VSS
F16	GND		107	VSS	68	VSS
G5	GND		109	VSS	69	VSS
H1	GND		112	VSS	72	VSS
H3	GND		114	VSS	73	VSS
H6	GND		116	VSS	77	VSS
H8	GND		118	VSS	78	VSS
H14	GND		120	VSS	81	VSS
H17	GND		123	VSS	82	VSS
J2	GND		125	VSS	85	VSS
J4	GND		127	VSS	86	VSS
J9	GND		129	VSS	89	VSS
J12	GND		131	VSS	90	VSS
K2	GND		134	VSS	93	VSS
K3	GND		136	VSS	94	VSS
K5	GND		138	VSS	98	VSS
K7	GND		147	VSS	99	VSS
K12	GND		149	VSS	102	VSS
K15	GND		151	VSS	103	VSS
L15	GND		154	VSS	106	VSS
M2	GND		156	VSS	107	VSS
M7	GND		158	VSS	167	VSS
M11	GND		160	VSS	168	VSS
M16	GND		162	VSS	171	VSS
N15	GND		165	VSS	172	VSS
P2	GND		167	VSS	175	VSS

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
P3	GND		169	VSS	176	VSS
P5	GND		171	VSS	180	VSS
P7	GND		173	VSS	181	VSS
P12	GND		176	VSS	184	VSS
P15	GND		178	VSS	185	VSS
R2	GND		180	VSS	188	VSS
R4	GND		182	VSS	189	VSS
R9	GND		184	VSS	192	VSS
R12	GND		187	VSS	193	VSS
T1	GND		189	VSS	196	VSS
T3	GND		191	VSS	197	VSS
T6	GND		193	VSS	201	VSS
T8	GND		195	VSS	202	VSS
T14	GND		198	VSS	205	VSS
T17	GND		200	VSS	206	VSS
U5	GND		202	VSS	209	VSS
V5	GND		239	VSS	210	VSS
V11	GND		241	VSS	213	VSS
V14	GND		243	VSS	214	VSS
V16	GND		246	VSS	217	VSS
W3	GND		248	VSS	218	VSS
W7	GND		250	VSS	222	VSS
W8	GND		252	VSS	223	VSS
W10	GND		254	VSS	226	VSS
W12	GND		257	VSS	227	VSS
W15	GND					

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
Rev A (x16) or Rev B (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V

9/18/2018 Rev C3

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
Y6	GND					
Y14	GND					
Y17	GND					
M9	VREFCA		146	VREFCA	164	VREFCA
A3	VDD		59	VDD	135	VDD
A5	VDD		61	VDD	136	VDD
A9	VDD		64	VDD	130	VDD
AB5	VDD		67	VDD	154	VDD
AB12	VDD		70	VDD	141	VDD
AB16	VDD		73	VDD	142	VDD
AC3	VDD		76	VDD	147	VDD
AC5	VDD		80	VDD	159	VDD
AC9	VDD		83	VDD	148	VDD
B5	VDD		85	VDD	153	VDD
B12	VDD		88	VDD	160	VDD
B16	VDD		90	VDD	163	VDD
D8	VDD		92	VDD	111	VDD
D15	VDD		204	VDD	112	VDD
E9	VDD		206	VDD	117	VDD
E11	VDD		209	VDD	123	VDD
E14	VDD		212	VDD	124	VDD
F8	VDD		215	VDD	118	VDD
G8	VDD		217	VDD	129	VDD
G14	VDD		220	VDD		
G16	VDD		223	VDD		
H2	VDD		226	VDD		

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
Rev A (x16) or Rev B (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V

9/18/2018 Rev C3

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
H4	VDD		229	VDD		
H5	VDD		231	VDD		
H12	VDD		233	VDD		
J3	VDD		236	VDD		
J5	VDD					
J6	VDD					
K1	VDD					
K4	VDD					
K6	VDD					
L14	VDD					
L16	VDD					
N14	VDD					
N16	VDD					
P1	VDD					
P4	VDD					
P6	VDD					
R3	VDD					
R5	VDD					
R6	VDD					
T2	VDD					
T4	VDD					
T5	VDD					
T12	VDD					
U8	VDD					
U14	VDD					
U16	VDD					

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72									
Sort by Function									
Byte	0	1	2	3					
Byte	4	5	6	7	ECC				
Control	Clock	Addr	Bank Grp	Miscel					
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8				
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8				
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V				
9/18/2018	Rev C3								
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin				JEDEC SO-DIMM - 260 pin		
Ball	Signal MCP		Pin UDM	Signal UDM			Pin SODM	Signal SODM	
V8	VDD								
W9	VDD								
W11	VDD								
W14	VDD								
Y8	VDD								
Y15	VDD								
A1	VPP		143	VPP			257	VPP	
E17	VPP		286	VPP			259	VPP	
AC1	VPP		287	VPP					
W17	VPP		288	VPP					
			142	VPP					
L17	VTT		221	VTT			258	VTT	
J1	VTT		77	VTT					
M17	VTT								
N17	VTT								
R1	VTT								
G10	ZQ0	Calibration Reference - Connect to GND via 240Ω 1% Resistor							
F10	ZQ1								
C10	ZQ2								
D10	ZQ3								
AA10	ZQ4								
Y10	ZQ5								
U10	ZQ6								
V10	ZQ7								
H10	ZQ8								

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
Rev A (x16) or Rev B (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V

9/18/2018 Rev C3

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
L5	TEN	Active High signal. Must be Low during normal operation				
AA1	NC	No Connect				
AA2	NC					
AA3	NC					
AA4	NC					
AA6	NC					
AA7	NC					
AB2	NC					
AB4	NC					
AB6	NC					
B2	NC					
B4	NC					
B6	NC					
C1	NC					
C2	NC					
C3	NC					
C4	NC					
C6	NC					
C7	NC					
D1	NC					
D2	NC					
D3	NC					
D4	NC					
D5	NC					
D7	NC					

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
Rev A (x16) or Rev B (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V

9/18/2018 Rev C3

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
D13	NC					
E1	NC					
E2	NC					
E4	NC					
E5	NC					
E6	NC					
F1	NC					
F2	NC					
F3	NC					
F4	NC					
F6	NC					
F7	NC					
G1	NC					
G2	NC					
G3	NC					
G4	NC					
G6	NC					
J8	NC					
J10	NC					
K8	NC					
K10	NC					
L8	NC					
L10	NC					
M8	NC					
M10	NC					
N8	NC					

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
Rev A (x16) or Rev B (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V

9/18/2018 Rev C3

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
N10	NC					
P8	NC					
P9	NC					
P10	NC					
P11	NC					
P13	NC					
P14	NC					
P16	NC					
P17	NC					
R8	NC					
R10	NC					
R13	NC					
R14	NC					
R15	NC					
R16	NC					
R17	NC					
T10	NC					
U1	NC					
U2	NC					
U3	NC					
U4	NC					
U6	NC					
V1	NC					
V2	NC					
V3	NC					
V4	NC					

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
V6	NC					
V7	NC					
W1	NC					
W2	NC					
W4	NC					
W5	NC					
W6	NC					
Y1	NC					
Y2	NC					
Y3	NC					
Y4	NC					
Y5	NC					
Y7	NC					
Y13	NC					
		Signals for External	139	SA0	256	SA0
		SPD EEPROM to interface	140	SA1	260	SA1
		to Host Processor /	238	SA2	166	SA2
		Memory Controller	141	SCL	253	SCL
		if used or NC	285	SDA	254	SDA
			284	VDDSPD	255	VDDSPD
		Not Required - NC	219	CK1_c	140	CK1_c
			218	CK1_t	138	CK1_t
			203	CKE1	110	CKE1
			78	EVENT_n	134	EVENT_n
			91	ODT1	161	ODT1
			89	CS1_n	157	CS1_n

Rev A (x16) & Rev B (x8) Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
			93	CS2_n C[0]	162	C0, CS2_n, NC
			237	CS3_n C[1]	165	C1, CS3_N, NC
			234	A17 NC		
			235	C[2] NC		
			1	12V NC		
			145	12V NC		
		Reserved - NC	144	RFU		
			205	RFU		
			227	RFU		
		No Connect	19	NC		
			30	NC		
			41	NC		
			100	NC		
			111	NC		
			122	NC		
			133	NC		
			52	NC		
			8	NC		
			230	NC		

9.2 Appendix B

The table below maps MCP signals to JEDEC DDR4 288 Pin UDIMM & 260 Pin SO-DIMM Rev A (x16) Single Channel x 72. The Table provides a cross reference between standard JEDEC signals and or Embedded Processor / Memory Controller and MCP sorted by MCP Ballout designation. Rev A part is configured for x16 & Rev B part is configured for x8.

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
A1	VPP		143	VPP	257	VPP
A2	GND		2	VSS	1	VSS
A3	VDD		59	VDD	135	VDD
A4	GND		4	VSS	2	VSS
A5	VDD		61	VDD	136	VDD
A6	GND		6	VSS	5	VSS
A7	DQ30		43	DQ30	79	DQ30
A8	GND		9	VSS	6	VSS
A9	VDD		64	VDD	130	VDD
A10	GND		11	VSS	9	VSS
A11	DQ25		183	DQ25	71	DQ25
A12	GND	Ground / VSS	13	VSS	10	VSS
A13	DQ22		32	DQ22	58	DQ22
A14	GND		15	VSS	14	VSS
A15	DQ19		179	DQ19	63	DQ19
A16	DQ17		172	DQ17	49	DQ17
A17	GND		17	VSS	15	VSS
B1	GND		20	VSS	18	VSS
B2	NC					
B3	GND		22	VSS	19	VSS
B4	NC					
B5	VDD		67	VDD	154	VDD

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
B6	NC					
B7	DQ28		36	DQ28	66	DQ28
B8	GND		24	VSS	22	VSS
B9	DQ29		181	DQ29	67	DQ29
B10	GND		26	VSS	23	VSS
B11	DQ27		190	DQ27	84	DQ27
B12	VDD		70	VDD	141	VDD
B13	DQ20		25	DQ20	46	DQ20
B14	GND		28	VSS	26	VSS
B15	DQ16	DataByte 2	27	DQ16	50	DQ16
B16	VDD		73	VDD	142	VDD
B17	DQS2_c		174	DQS2_c	53	DQS2_c
C1	NC					
C2	NC					
C3	NC					
C4	NC					
C5	GND		31	VSS	27	VSS
C6	NC					
C7	NC					
C8	GND		33	VSS	30	VSS
C9	DQ31		188	DQ31	80	DQ31
C10	ZQ2	Calibration Reference				
C11	DQ26		45	DQ26	83	DQ26
C12	DQS3_t		186	DQS3_t	76	DQS3_t
C13	DQ23		177	DQ23	59	DQ23
C14	DQ21		170	DQ21	45	DQ21

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
C15	DQ18		34	DQ18	62	DQ18
C16	GND		35	VSS	31	VSS
C17	DQS2_t		175	DQS2_t	55	DQS2_t
D1	NC					
D2	NC					
D3	NC					
D4	NC					
D5	NC					
D6	GND		37	VSS	35	VSS
D7	NC					
D8	VDD		76	VDD	147	VDD
D9	DQ24	DataByte 3	38	DQ24	70	DQ24
D10	ZQ3	Calibration Reference				
D11	DM3_n		40	DM3_n, DBI3_n, NC	75	DM3_n, DBI3_n, NC
D12	DQS3_c		185	DQS3_c	74	DQS3_c
D13	NC					
D14	GND		39	VSS	36	VSS
D15	VDD		80	VDD	159	VDD
D16	DM2_n		29	DM2_n, DBI2_n, NC	54	DM2_n, DBI2_n, NC
D17	GND		42	VSS	39	VSS
E1	NC					
E2	NC					
E3	GND		44	VSS	40	VSS
E4	NC					
E5	NC					
E6	NC					

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
E7	GND		46	VSS	43	VSS
E8	GND		48	VSS	44	VSS
E9	VDD		83	VDD	148	VDD
E10	GND		50	VSS	47	VSS
E11	VDD		85	VDD	153	VDD
E12	GND		53	VSS	48	VSS
E13	DQ15		166	DQ15	37	DQ15
E14	VDD		88	VDD	160	VDD
E15	GND		55	VSS	51	VSS
E16	DQ9		161	DQ9	29	DQ9
E17	VPP		286	VPP	259	VPP
F1	NC					
F2	NC					
F3	NC					
F4	NC					
F5	GND		57	VSS	52	VSS
F6	NC					
F7	NC					
F8	VDD		90	VDD	163	VDD
F9	DQ3		157	DQ3	21	DQ3
F10	ZQ1	Calibration Reference				
F11	GND		94	VSS	56	VSS
F12	DQS0_c		152	DQS0_c	11	DQS0_c
F13	DQ12		14	DQ12	24	DQ12
F14	GND		96	VSS	57	VSS
F15	DQ10		23	DQ10	41	DQ10

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
F16	GND		98	VSS	60	VSS
F17	DQS1_t		164	DQS1_t	34	DQS1_t
G1	NC					
G2	NC					
G3	NC					
G4	NC					
G5	GND		101	VSS	61	VSS
G6	NC					
G7	DQ7		155	DQ7	17	DQ7
G8	VDD		92	VDD		
G9	DQ2		12	DQ2	20	DQ2
G10	ZQ0	Calibration Reference				
G11	DM0_n		7	DM0_n, DBI0_n, NC	12	DM0_n, DBI0_n, NC
G12	DQS0_t		153	DQS0_t	13	DQS0_t
G13	DQ13		159	DQ13	25	DQ13
G14	VDD		204	VDD		
G15	DQ8	DataByte 1	16	DQ8	28	DQ8
G16	VDD		206	VDD		
G17	DQS1_c		163	DQS1_c	32	DQS1_c
H1	GND		103	VSS	64	VSS
H2	VDD		209	VDD		
H3	GND		105	VSS	65	VSS
H4	VDD		212	VDD		
H5	VDD		215	VDD		
H6	GND		107	VSS	68	VSS
H7	DQ4		3	DQ4	4	DQ4

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
H8	GND		109	VSS	69	VSS
H9	DQ5		148	DQ5	3	DQ5
H10	ZQ8	Calibration Reference				
H11	DQ1		150	DQ1	7	DQ1
H12	VDD		217	VDD		
H13	DQ14		21	DQ14	38	DQ14
H14	GND		112	VSS	72	VSS
H15	DQ11		168	DQ11	42	DQ11
H16	DM1_n		18	DM1_n, DBI1_n, NC	33	DM1_n, DBI1_n, NC
H17	GND		114	VSS	73	VSS
J1	VTT		77	VTT		
J2	GND		116	VSS	77	VSS
J3	VDD		220	VDD	111	VDD
J4	GND		118	VSS	78	VSS
J5	VDD		223	VDD	112	VDD
J6	VDD		226	VDD	117	VDD
J7	DQ6		10	DQ6	16	DQ6
J8	NC					
J9	GND		120	VSS	81	VSS
J10	NC					
J11	DQ0	DataByte 0	5	DQ0	8	DQ0
J12	GND		123	VSS	82	VSS
J13	CB7		199	CB7, NC	104	CB7, NC
J14	CB5		192	CB5, NC	87	CB5, NC
J15	DM8_n		51	DM8_n, DBI8_n, NC	96	DM8_n, DBI8_n, NC
J16	CB1		194	CB1, NC	91	CB1, NC

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
J17	DQS8_t		197	DQS8_t	97	DQS8_t
K1	VDD		229	VDD	123	VDD
K2	GND		125	VSS	85	VSS
K3	GND		127	VSS	86	VSS
K4	VDD					
K5	GND		129	VSS	89	VSS
K6	VDD					
K7	GND		131	VSS	90	VSS
K8	NC					
K9	CB6		54	CB6, NC	100	CB6, NC
K10	NC					
K11	CB3		201	CB3, NC	105	CB3, NC
K12	GND		134	VSS	93	VSS
K13	CB4		47	CB4, NC	88	CB4, NC
K14	CB2		56	CB2, NC	101	CB2, NC
K15	GND		136	VSS	94	VSS
K16	CB0	ECC Byte	49	CB0, NC	92	CB0, NC
K17	DQS8_c		196	DQS8_c	95	DQS8_c
L1	A13		232	A13	158	A13
L2	A9		66	A9	121	A9
L3	ALERT_n		208	ALERT_n	116	ALERT_n
L4	A6		69	A6	127	A6
L5	TEN	Active High signal. Must be Low during normal operation				
L6	BA1		224	BA1	145	BA1
L7	BG0		63	BG0	115	BG0

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
L8	NC					
L9	A12		65	A12/BC_n	119	A12
L10	NC					
L11	ACT_n	Miscellaneous	62	ACT_n	114	ACT_n
L12	A14/WE_n		228	WE_n/A14	151	A14/WE_n
L13	CS0_n		84	CS0_n	149	CS0_n
L14	VDD					
L15	GND		138	VSS	98	VSS
L16	VDD					
L17	VTT		221	VTT	258	VTT
M1	A11		210	A11	120	A11
M2	GND		147	VSS	99	VSS
M3	A7		211	A7	122	A7
M4	A1		72	A1	133	A1
M5	RESET_n		58	RESET_n	108	RESET_n
M6	A4		214	A4	128	A4
M7	GND		149	VSS	102	VSS
M8	NC					
M9	VREFCA		146	VREFCA	164	VREFCA
M10	NC					
M11	GND		151	VSS	103	VSS
M12	A16/RAS_n		82	RAS_n/A16	152	A16/RAS_n
M13	ODT0		87	ODT0	155	ODT0
M14	CK0_c		75	CK0_c	139	CK0_c
M15	CK0_t	Clock	74	CK0_t	137	CK0_t
M16	GND		154	VSS	106	VSS

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
M17	VTT					
N1	PARITY		222	PARITY	143	PARITY
N2	A2		216	A2	132	A2
N3	A8		68	A8	125	A8
N4	A0	Address	79	A0	144	A0
N5	A5		213	A5	126	A5
N6	A3		71	A3	131	A3
N7	BA0	Bank Group	81	BA0	150	BA0
N8	NC					
N9	A10/AP		225	A10/AP	146	A10/AP
N10	NC					
N11	BG1	Connect to Processor / Memory Controller for future migration from 4GB to 8GB MCP	207	BG1	113	BG1
N12	A15/CAS_n		86	CAS_n/A15	156	A15/CAS_n
N13	CKE0		60	CKE0	109	CKE0
N14	VDD					
N15	GND		156	VSS	107	VSS
N16	VDD					
N17	VTT					
P1	VDD					
P2	GND		158	VSS	167	VSS
P3	GND		160	VSS	168	VSS
P4	VDD					
P5	GND		162	VSS	171	VSS

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
P6	VDD					
P7	GND		165	VSS	172	VSS
P8	NC					
P9	NC					
P10	NC					
P11	NC					
P12	GND		167	VSS	175	VSS
P13	NC					
P14	NC					
P15	GND		169	VSS	176	VSS
P16	NC					
P17	NC					
R1	VTT					
R2	GND		171	VSS	180	VSS
R3	VDD					
R4	GND		173	VSS	181	VSS
R5	VDD					
R6	VDD					
R7	DQ62		135	DQ62	245	DQ62
R8	NC					
R9	GND		176	VSS	184	VSS
R10	NC					
R11	DQ59		282	DQ59	250	DQ59
R12	GND		178	VSS	185	VSS
R13	NC					
R14	NC					

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
R15	NC					
R16	NC					
R17	NC					
T1	GND		180	VSS	188	VSS
T2	VDD					
T3	GND		182	VSS	189	VSS
T4	VDD					
T5	VDD					
T6	GND		184	VSS	192	VSS
T7	DQ60		128	DQ60	232	DQ60
T8	GND		187	VSS	193	VSS
T9	DQ61		273	DQ61	233	DQ61
T10	NC					
T11	DQ57		275	DQ57	236	DQ57
T12	VDD					
T13	DQ54		124	DQ54	224	DQ54
T14	GND		189	VSS	196	VSS
T15	DQ51		271	DQ51	229	DQ51
T16	DM6_n		121	DM6_n, DB16_n, NC	220	DM6_n, DB16_n, NC
T17	GND		191	VSS	197	VSS
U1	NC					
U2	NC					
U3	NC					
U4	NC					
U5	GND		193	VSS	201	VSS
U6	NC					

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
U7	DQ63		280	DQ63	246	DQ63
U8	VDD		231	VDD	124	VDD
U9	DQ58		137	DQ58	249	DQ58
U10	ZQ6	Calibration Reference				
U11	DQ52		117	DQ52	211	DQ52
U12	DQ53		262	DQ53	212	DQ53
U13	DQ55		269	DQ55	225	DQ55
U14	VDD					
U15	DQ48	DataByte 6	119	DQ48	216	DQ48
U16	VDD					
U17	DQS6_c		266	DQS6_c	219	DQS6_c
V1	NC					
V2	NC					
V3	NC					
V4	NC					
V5	GND		195	VSS	202	VSS
V6	NC					
V7	NC					
V8	VDD		233	VDD	118	VDD
V9	DQ56	DataByte 7	130	DQ56	237	DQ56
V10	ZQ7	Calibration Reference				
V11	GND		198	VSS	205	VSS
V12	DM7_n		132	DM7_n, DB17_n, NC	241	DM7_n, DB17_n, NC
V13	DQS7_t		278	DQS7_t	242	DQS7_t
V14	GND		200	VSS	206	VSS
V15	DQ50		126	DQ50	228	DQ50

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
V16	GND		202	VSS	209	VSS
V17	DQS6_t		267	DQS6_t	221	DQS6_t
W1	NC					
W2	NC					
W3	GND		239	VSS	210	VSS
W4	NC					
W5	NC					
W6	NC					
W7	GND		241	VSS	213	VSS
W8	GND		243	VSS	214	VSS
W9	VDD					
W10	GND		246	VSS	217	VSS
W11	VDD					
W12	GND		248	VSS	218	VSS
W13	DQS7_c		277	DQS7_c	240	DQS7_c
W14	VDD					
W15	GND		250	VSS	222	VSS
W16	DQ49		264	DQ49	215	DQ49
W17	VPP		288	VPP		
Y1	NC					
Y2	NC					
Y3	NC					
Y4	NC					
Y5	NC					
Y6	GND		252	VSS	223	VSS
Y7	NC					

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
Y8	VDD		236	VDD	129	VDD
Y9	DQ39		247	DQ39	182	DQ39
Y10	ZQ5	Calibration Reference				
Y11	DQ34		104	DQ34	187	DQ34
Y12	DQS4_c		244	DQS4_c	177	DQS4_c
Y13	NC					
Y14	GND		254	VSS	226	VSS
Y15	VDD					
Y16	DM5_n		110	DM5_n, DB15_n, NC	199	DM5_n, DB15_n, NC
Y17	GND		257	VSS	227	VSS
AA1	NC	No Connect				
AA2	NC					
AA3	NC					
AA4	NC					
AA5	GND		259	VSS	230	VSS
AA6	NC					
AA7	NC					
AA8	GND		261	VSS	231	VSS
AA9	DQ32	DataByte 4	97	DQ32	174	DQ32
AA10	ZQ4	Calibration Reference				
AA11	DM4_n		99	DM4_n, DB14_N, NC	178	DM4_n, DB14_N, NC
AA12	DQS4_t		245	DQS4_t	179	DQS4_t
AA13	DQ47		258	DQ47	204	DQ47
AA14	DQ45		251	DQ45	190	DQ45
AA15	DQ42		115	DQ42	207	DQ42
AA16	GND		263	VSS	234	VSS

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AA17	DQS5_t		256	DQS5_t	200	DQS5_t
AB1	GND		265	VSS	235	VSS
AB2	NC					
AB3	GND		268	VSS	238	VSS
AB4	NC					
AB5	VDD					
AB6	NC					
AB7	DQ38		102	DQ38	183	DQ38
AB8	GND		270	VSS	239	VSS
AB9	DQ37		240	DQ37	169	DQ37
AB10	GND		272	VSS	243	VSS
AB11	DQ33		242	DQ33	173	DQ33
AB12	VDD					
AB13	DQ46		113	DQ46	203	DQ46
AB14	GND		274	VSS	244	VSS
AB15	DQ40	DataByte 5	108	DQ40	195	DQ40
AB16	VDD					
AB17	DQS5_c		255	DQS5_c	198	DQS5_c
AC1	VPP		287	VPP		
AC2	GND		276	VSS	247	VSS
AC3	VDD					
AC4	GND		279	VSS	248	VSS
AC5	VDD					
AC6	GND		281	VSS	251	VSS
AC7	DQ36		95	DQ36	170	DQ36
AC8	GND		283	VSS	252	VSS

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AC9	VDD					
AC10	GND					
AC11	DQ35		249	DQ35	186	DQ35
AC12	GND					
AC13	DQ44		106	DQ44	191	DQ44
AC14	GND					
AC15	DQ43		260	DQ43	208	DQ43
AC16	DQ41		253	DQ41	194	DQ41
AC17	GND					
			142	VPP		
		Signals for External	139	SA0	256	SA0
		SPD EEPROM to interface	140	SA1	260	SA1
		to Host Processor /	238	SA2	166	SA2
		Memory Controller	141	SCL	253	SCL
		if used	285	SDA	254	SDA
			284	VDDSPD	255	VDDSPD
		Not Required - NC	219	CK1_c	140	CK1_c
			218	CK1_t	138	CK1_t
			203	CKE1	110	CKE1
			78	EVENT_n	134	EVENT_n
			91	ODT1	161	ODT1
			89	CS1_n	157	CS1_n
			93	CS2_n C[0]	162	C0, CS2_n, NC
			237	CS3_n C[1]	165	C1, CS3_N, NC
			234	A17 NC		
			235	C[2] NC		

Rev A x16 & Rev B x8 Ballout - Mapped to JEDEC DDR4: 288 Pin UDIMM & 260 Pin SO-DIMM Compatible Rev A (x16) or Rev B (x8) Single Channel x 72					
Sort by Ballout					
Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
			1	12V NC		
			145	12V NC		
		Reserved - NC	144	RFU		
			205	RFU		
			227	RFU		
		No Connect	19	NC		
			30	NC		
			41	NC		
			100	NC		
			111	NC		
			122	NC		
			133	NC		
			52	NC		
			8	NC		
			230	NC		

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Mailing Address: Teledyne e2v Semiconductors SAS, Avenue de Rochepleine, 38120 Saint Egrève, France.

Telephone: +33 4 76 58 30 00

e-mail: hotline-std@teledyne.com