WHITE PAPER

Advanced ATP Maximizes System Performance While Alleviating Production Bottlenecks

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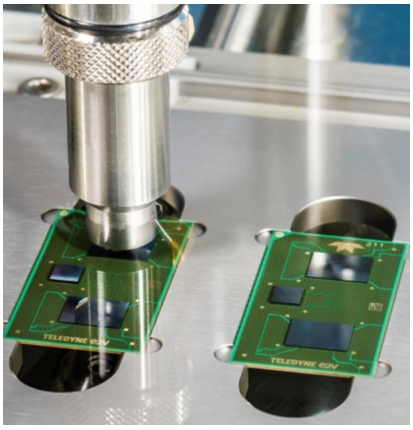
ABSTRACT

Electronic systems are experiencing rapid changes in performance specifications and form factors, along with numerous supply chain bottlenecks. One system level design problem has been consistent throughout—balancing the form factor tradeoffs between the analog and digital circuitry for maximum software/system flexibility (from sensor to the digital processing units' input/output). This fundamental problem requires the system designer to partition (or combine) various circuit components that would allow for maximum softwarization. Now, as the future of advanced ATP technologies accelerate system design implementations from hardware to software centricity; Teledyne e2v's advanced ATP/SiP expertise revolutionizes system level design for maximum flexibility and multi-mission capability. Using state-of-the-art technologies (e.g. flip chip, organic packages, etc.) for RF, Mixed-Signal, and Digital Processing applications for use in: industrial, medical, avionic, instrumentation, telecommunication, defense, and space applications are realized. Teledyne e2v's 40+ years of experience in advanced ATP/SiP technologies gives system designers the highest performance and production flexibility for electronic system platform developments.



SEMICONDUCTOR FABRICATION VS. IMPLEMENTATION

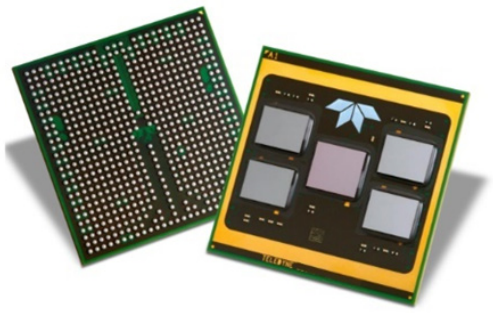
Governments around the world are pushing to domesticate the semiconductor industry by setting up local production facilities through generous financial incentives. For instance, the EU Chips Act recently triggered a further €22 billion investment into the European semiconductor value chain. This latest IPCEI (Important Project of Common European Interest) is generating considerable public and private investments across the European semiconductor industry [1]. More specifically, it recognizes the need to expand industrial capacities of supply chain bottlenecks: materials (including wafers), and equipment (for wafer production, chip production, and advanced ATP (assembly, test, and packaging). Alleviating supply chain bottlenecks becomes even more critical as companies – including many SMEs – continue to focus on front-end/next generation semiconductor device technologies: Processors, AI chips, FPGAs, Memory, Chiplets, and Optical Interconnects, etc. Cutting edge test equipment and packaging materials now becomes another chokepoint in the supply chain to implement these next generation semiconductors for the communications, automotive, industrial automation and IoT sectors, as well as AI, Edge-computing, and other markets.

Massive worldwide investments primarily focusing on the expansion of semiconductor fabrication also create equally massive problems on how to implement these same chips in the real world. The current focus on increasing the capacity for advanced semiconductor fabrication should also be paired with a concurrent emphasis on advanced ATP. Historically, ATP is viewed as a lower level/back-end activity vs. higher level/value-added front-end semiconductor fabrication [2]. Two trends are driving a change in how ATP is viewed: 1) IDMs increasingly recognize how important advanced ATP is to processing power, particularly as Moore's Law slows, and, therefore, 2) IDMs must invest significant financial an intellectual capital to develop materials, equipment, and systems that support an advanced ATP ecosystem in order to implement newer semiconductor solutions. Innovation in advanced ATP will be a key determinant of the depth and breadth of implementing next generation semiconductors into other emerging markets that will also, in turn, influence future semiconductor industry technologies, etc.

Assembly, packaging, and test (ATP) is simply the process of connecting, protecting, and validating finished semiconductors. Advanced packaging is a superset of traditional packaging and involves a series of steps for combining chips into packages, resulting in lower power consumption, increased I/O and performance, and lower cost [3]. Packaging is becoming a bottleneck to semiconductor innovation because "densities of transistors in logic and memory chips have continued to increase exponentially, but the density of interconnects [wires] between logic and memory—governed by packaging— have increased at a much slower rate, leading to communication bottlenecks between chips" [4]. The semiconductor industry has focused fewer resources on addressing this problem in favor of continuing traditional CMOS scaling as dictated by Moore's Law. However, as transistor density reaches physical limits, the industry seeks novel ways to increase chip performance. New packaging techniques promise to increase interconnect density, which will accelerate signal speed and reduce energy requirements [4]. Advanced packaging uses new techniques and materials to increase integrated circuit performance, power, modularity, and durability. These advanced packages have a variety of benefits: lower latency, increased bandwidth, better efficiency and power delivery, and higher input/output density [5]. Package types are most commonly differentiated and segmented by interconnect type.

ADVANCED PACKAGING INCREASES PERFORMANCE & LOWERS VOLUME PRODUCTION FOR ALL MARKET SEGMENTS

Currently, the distinctions between assembly, packaging, and test (ATP) of semiconductors are becoming increasingly blurred, especially when advanced packaging is utilized [2]. Conventional semiconductor ATP begins with the inspection of fabricated wafers for defects and dicing them into individual ICs. These ICs are then attached and wired bonded to a substrate or PCB and encased for connection (and protection) into a larger electronic system. Conventional semiconductor packaging is an inherently sequential process. "Advanced packaging" combines many of these process steps in parallel, and increasingly makes use of front-end processes and tools such as lithography and metrology equipment [2].



Advanced packaging, like conventional packaging, is developed by either: (1) IDMs or Foundries with in-house ATP services performed during post-fabrication, or (2) OSAT (Outsourced Semiconductor Assembly and Test) firms (e.g. Teledyne e2v) for third-party customers. OSAT customers include IDMs, Foundries and Fabless companies. Wire bonds are still the most common advanced package interconnect method to connect an IC to a PCB for electronic signal transfer. The current challenge with wire bonds is that their size does not scale relative to increased transistor densities. Fundamentally, transistors exhibit greater processing power than wires are capable of transmitting. Advanced packaging solves this interconnecting problem utilizing "bumps," "balls," or "wafer-level packaging" rather than wires to connect ICs. This minimizes package size and maximizes performance while reducing costs. As semiconductor content increases, there is also an increased demand for advanced packaging services.

System-in-package technology (SiP) uses the previously described interconnect methods while combining a number of integrated circuits and passive components enclosed in a single chip carrier package that can perform the functions of an entire system. SiPs compare directly to system-on-a-chip (SoC) integrated circuit architectures that continue to experience severe limitations due to the slowing of Moore's Law. As the cost of producing SoCs increases exponentially, chiplets have risen in popularity and packaged utilizing SiP platform technology. A chiplet is an integrated circuit block that has been specifically designed to communicate with other chiplets to emulate more complex ICs. Large complex chip designs can be subdivided into functional circuit blocks (i.e. reusable IP blocks called chiplets). Chiplets are then recombined onto a high density SiP advanced package. Chiplets allow an electronic system to behave like it is one integrated circuit even though it is composed of different/multiple/smaller integrated circuits. This is accomplished using heterogeneous integration of separately manufactured components into a higher-level assembly SiP. Overall, this provides lower development costs, reduced timeframes, enhanced functionality, quick reconfiguring modifications, and improved performance characteristics" [6] [7].

The advantage of using chiplets mounted on SiP advanced packaging platforms are: (1) Smaller ICs which increase yield (chips/wafer), (2) Heterogeneous integration of advanced and mature chips in the same system, (3) Mixing and matching ICs to optimize system performance for specific applications, (4) Enabling the usage of different process technologies (e.g., gallium nitride, or GaN) to provide better performance beyond silicon, 5) Integration increases functionality and performance while reducing overall production volumes, 6) SiP designs implementing passive and active components further enable SWaP reductions, 7) High-density SiP technologies also lower inductance reducing the need for decoupling capacitors. For example, high density IC interconnect SiP technology, combined with embedded passives, have been shown to achieve as much as 27X reduction in physical size for existing printed wiring board assemblies, with significant reductions in weight and power consumption [8]. Primary reductions in power are due to reduced interconnect lengths and corresponding loads. Shorter interconnects can also reduce or eliminate the need for termination resistors for some net topologies.

TELEDYNE E2V'S ADVANCED ATP SERVICES

System design engineers understand their markets, applications, and circuit performance specification requirements; but their design parameters such as risk, technology choices, form factors, development schedules (including schedule synchronization), reliabilities, costs and supply chain constraints are highly variable. These design parameters, coupled with continually changing system performance specification requirements, ultimately result in narrower design implementation "intersection" options (Figure 1). Of course, making mistakes within any design parameter is extremely costly. Therefore, flexibilities that can be built into the design development, that adds value to the project is a worthy investment.

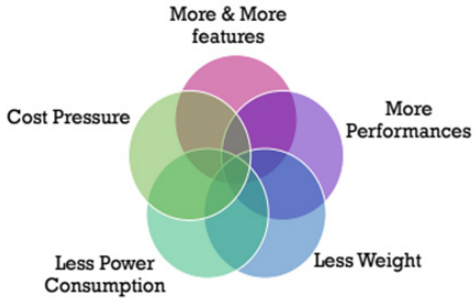


Figure 1 - Increasing design parameters, AND system level performance requirements, yields narrower "intersection" options

Utilizing advanced ATP SiP technology is one design parameter that can increase flexibility for both the development phase, and ultimately achieve necessary production volumes and market performance. In the past, continual advances in semiconductor process technologies have enabled system level designers to implement complete circuit functions within the SoC (System-on-Chip) environment. Particularly, SoC applications that require heavy digital computing, have been realized using semiconductor technology as gate lengths approach 10nm and smaller. Unfortunately, as semiconductor feature sizes decrease, the cost of chip development increases exponentially (Figure 2).

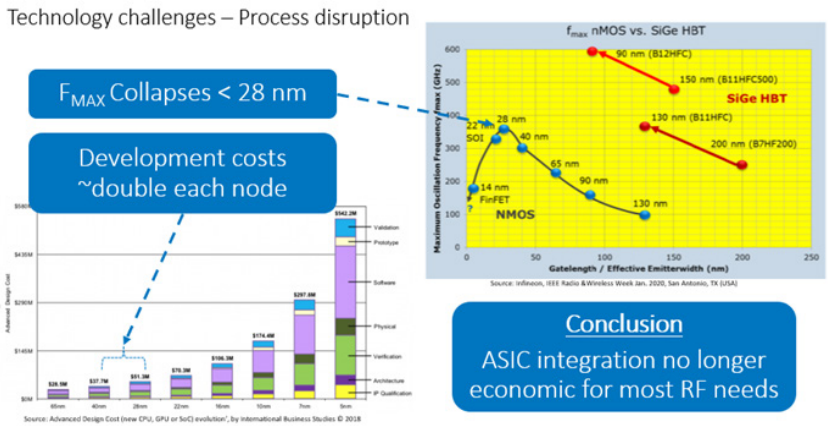


Figure 2

Te2v offers a broad range of supply chain management services for SiP design developments including: die design, package design, high-reliability assembly, high performance at-speed testing and qualification services including the Semiconductor Lifecycle Management under the SLiM™ brand. With over 40+ years of advanced ATP/design experience (including ADCs, DACs, Microprocessors, Memories, and In-house test and qualification services); Te2v provides advanced SiP products and services to all market segments at any qualification level requirement. Te2v's advanced ATP/SiP expertise includes: wire-bonding, flip-chip, organic and ceramic packaging (hermetic and non-hermetic), as well as heterogeneous assembly.

High reliability applications for high performance computing in space, defense, medical and industrial applications continually drive advanced ATP technologies towards increased functionality and performance with decreasing degrees of size, weight and power (SWaP). The substrate technology selected for the electronics packaging is a key enabling technology towards achieving SWaP and minimizing bottlenecks in production. Standard printed circuit boards (PCBs) utilize dielectric materials which limit circuit density and performance, as well as inhibit the ability to achieve reliable assemblies with multiple semiconductor components. Ceramic substrates used for chip packaging have disadvantages of weight, electrical performance and reliability as compared to organic substrate technologies. Alternative materials used in SiPs include thin organic substrates, liquid crystal polymer (LCP) and microflex which also support SWaP while overcoming the limitations of PCBs and ceramic [8].

TELEDYNE E2V'S ADVANCED PACKAGING TECHNOLOGIES

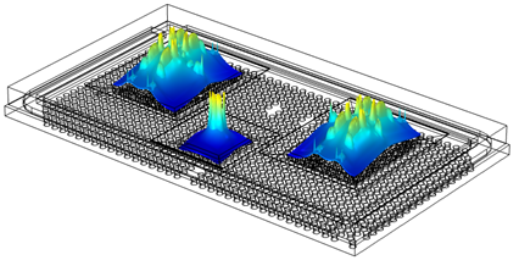


Figure 3 - SiP Thermal Simulation

Advanced ATP/SiP developments require package simulations as well as measured package characterizations for both thermal and reliability considerations. Thermal simulations are required to accurately predict junction temperatures on the most critical areas of the components. Te2v uses boundary conditions, discussed with system designers, to simulate performance that will ultimately match with measured results that would be required for the necessary components embedded within the SiP platform (Figure 3). In addition, Te2v utilizes high-frequency structure simulator analysis (Ansys HFSS) for the simulation and design of RF SiP developments. HFSS is a commercial finite element method that analyzes electromagnetic structures for the package design of complex RF electronic circuits, semiconductor elements, filters, and transmission lines contained within the SiP package. In this example, an RF analog front-end is co-designed at Te2v in collaboration between the package team and the semiconductor design team which accounts for Te2v's natural SiP process development flow [9].

Designing for SiP reliability is a significant engineering challenge due to the diverse silicon technologies that are embedded in a single organic substrate, with RoHS solder joints in C4 (controlled collapse chip connection - flip chip bumps) and C5 (solder balls) electro-mechanical interfaces. Te2v utilizes advanced techniques to quickly and precisely predict warpage and board level reliability with thermo-mechanical analysis, taking into account non-linear behavior such as solder creep and viscoplasticity (see Figure 4).

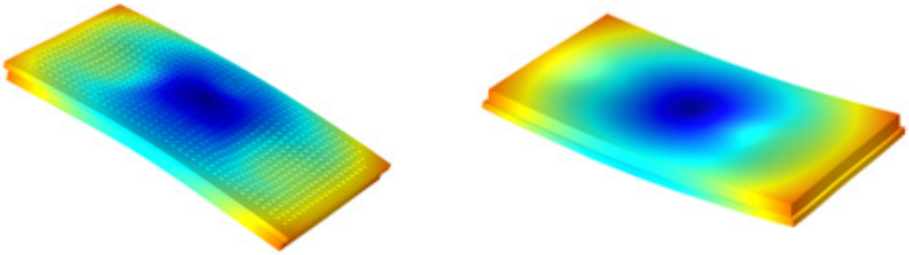


Figure 4 – 50x magnification of packaging warpage after assembly at room temperature.

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Specific design and assembly services also include: custom products, low and medium volume, high-reliability/high-end QML-V and QML-Y certifications, as well as space qualification. Te2v's advanced SiP design and assembly services becomes a "one-stop shop" for all market segments and product types (see Figures 5a and 5b). Simply put, because Te2v provides design, package, assembly, test, and qualification services for space-level applications, all other market segments, applications, and quality levels can also be realized as well.

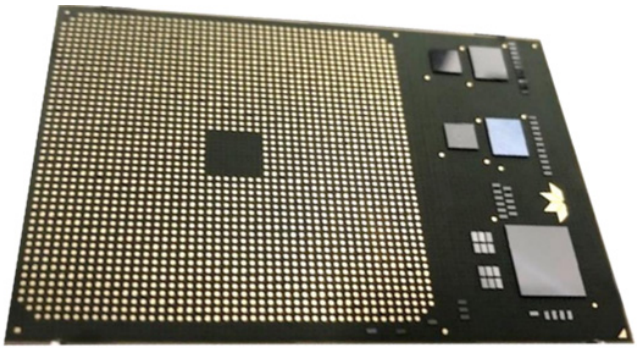

Figure 5a – an example of SiP on Organic Substrate (50mm x 60mm), Double-sided, 32 Steps, Top & Bottom

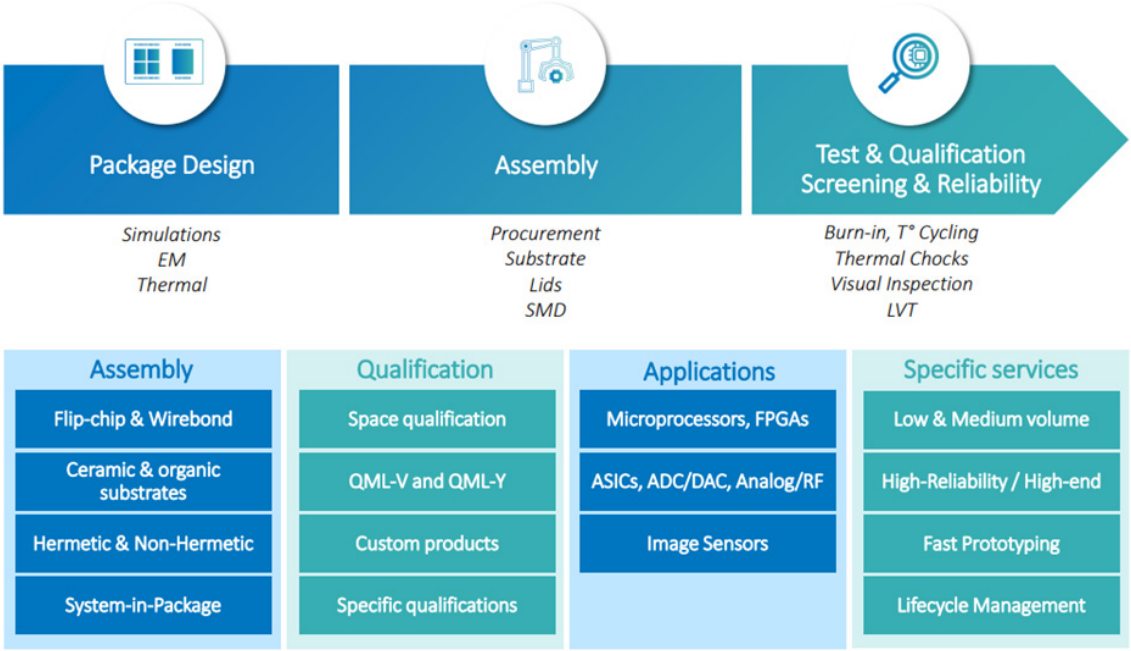

Figure 5b – Teledyne e2v ATP Services

Finally, as the future of advanced system developments enter the next decade, utilizing SiP technologies becomes of paramount importance in assembling devices with ever decreasing gate lengths which ultimately increase the area dimensions of the semiconductor. As larger and larger SoC's increasingly become one, of many other components contained within a SiP, the requirement to reliably assemble (wire-bond or flip chip) utilizing organic substrates and packaging materials require significant technological investments. Currently, Te2v is preparing these ATP technological advancements in the years to come, with all technological developments also being sponsored by ESA and IPCEI .

CONCLUSION

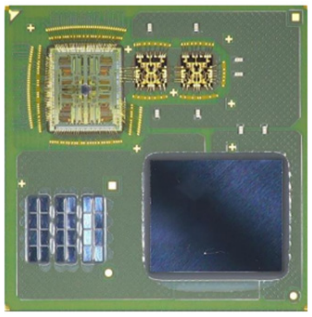

Figure 6 – Heterogeneous SiP Organic Substrate (20mm x 20mm) Si + GaAs + SMD Flip Chip, Copper Pillar, Wire bond Die-to-Die Bonding

Currently, system designers are experiencing crucial design parameter challenges in regards to semiconductor process choices (and geometries), circuit miniaturization requirements, along with increasing development costs and production bottlenecks. In addition, newer ADC, DAC, Microprocessor, and Memory components continue to become available for advanced system developments (see Figure 6). From industrial, to medical, to avionics, to instrumentation, to telecommunications, defense, and space applications; one system level design problem has been consistent throughout—balancing the form factor tradeoffs for maximum software/system flexibility and unimpeded production flow. Now, as the future of advanced ATP/SiP assembly technologies accelerate design implementations from hardware to software centricity, for all advanced market segments and applications; Teledyne e2v's ATP/SiP expertise revolutionizes system level design for maximum flexibility and multi-mission capability. Teledyne e2v's advanced ATP/SiP technologies give system designers the highest performance and value for present and future system platforms developments.

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