WHITE PAPER

Learn how Teledyne e2v characterizes its Space edge processing components against radiations:

Case study of a 4x Arm® Cortex® A72 + 4GB DDR4 computing module

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ABSTRACT

Radiation effects in Space are of the utmost importance to consider because they can cause d**amage to electronic components and systems**, leading to potential failures or malfunctions. High-energy particles, such as heavy-ions and protons, can cause **Single Event Effects (SEE)** in electronic devices, which can result in **temporary or permanent changes to the device's performance**. Additionally, **long-term exposure** to radiation can cause **degradation in electronic components and systems**, leading to **reduced reliability and performance** over time. **Considering radiation effects in the design, testing of space systems is essential to ensure their proper functioning and longevity in the harsh radiation environment of space**.

Next generations Space systems are always seeking at **higher computing performances to serve modern use cases** (Real-time image/video processing, Scientific data analysis, Communications, Autonomous operations, Artificial Intelligence, avionics) with **new perimeters in mission profiles** (orbits, lifetime in space, satellites redundancy / constellations). Since the high computing performance cannot be served by traditional Radiation Hardened devices, **designers have now to consider more standard computing solutions from the industrial market**, not radiation hardened, and **ensure at the same time that the system they will build with these solutions can still safely operate under radiations and with an acceptable lifetime**.

Teledyne e2v is providing compute intensive Radiation Tolerant digital processing solutions, such as an Arm® Cortex®-A72 processor and a high speed DDR4 memory. **QLS1046-Space is a very optimized radiation tolerant module based on these two standalone components**.

In the first section of this paper, the **strategy adopted by Teledyne e2v to test and fully characterize against radiations** its high-speed digital processing solutions is described. Then, the **QLS1046-Space product and its Space specific features are presented**. Afterwards, the **radiation test setups and methods** applied on the QLS1046-Space are presented, along with **results obtained in heavy-ions, protons, TID, and mitigations**.

Keywords: Edge computing, High speed processing, Radiations, SEE, TID, SEL, Protons, Mitigations

GENERAL RADIATION TESTING STRATEGY FOR SPACE RADIATION TOLERANT COMPONENTS

Radiation performance of the electronic components is one of the key topics in Space applications, and components have to be extensively tested against radiations to characterize their behaviour. Radiation Tolerant components are typically devices that have been initially designed with high level of computing performance for the industrial market. These devices are selected for Space because they offer high disruptive functional performance together with good level of radiation performance in terms of TID and Latch-up immunity (SEL). With regards to radiations, the Radiation Tolerant devices can endure upsets (SEU) and functional interrupts (SEFI) events. Project teams involved in the development of Space systems require radiation characterization data of the components they use to be able to calculate and predict the error rates in flight. If the error rates are too high, mitigation techniques are implemented.

Teledyne e2v performs complete radiation testing campaigns on its Radiation Tolerant processing solutions. The radiation testing strategy relies on three key pillars (Figure 1).

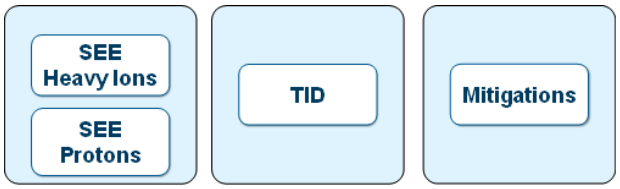

Figure 1: Key pillars of the radiation testing strategy

The initial step is the SEE heavy-ions testing, allowing to verify the SEL immunity of the device, and to characterize SEU and SEFI effects occurring when exposed to heavy-ions. SEE protons testing can then be performed to complement the heavy-ions testing, since LEO missions will be more subject to protons, and recent devices can exhibit a higher sensitivity to protons. TID testing is then performed to verify how much radiation dose the part is capable to sustain without degrading the functional performance. TID typically relates to the mission duration for which the part can be used, depending on the orbit altitude. The final part of the radiation testing consists in the mitigations of the radiation events, focusing on SEU and SEFI. Methods for recovering the events are proposed, implemented, and then tested under the beam. Based on the results, some mitigation methods or IPs can be proposed to the users for handling the radiation effects. It is sometimes required to go several times under the beam for the same type of testing, especially for complex devices such as processors.

To perform the different tests under radiations, Teledyne e2v designs and manufactures specific test boards to meet the needs of the tests. It means for instance the capability to monitor the supplies, adding the relevant peripherals, and handling the heat dissipation of the device. On top of the hardware, there is also some specific test software that is developed to exercise the different functional blocks of the part to be tested.

This comprehensive radiation testing strategy has been applied to the QLS1046-Space processing module from Teledyne e2v. In the next chapter, the device is quickly described. Then, the different radiation test results obtained are presented.

DESCRIPTION OF QLS1046-SPACE

QLS1046-Space is an integrated Space Radiation Tolerant Compute Intensive integrated solution, designed by Teledyne e2v in an optimized form factor of 44 x 26mm [2]. It embeds Teledyne e2v LS1046-Space & DDR4T04G72 products.

This common computer device can serve many applications requiring compute intensive capabilities in Space and serves as well Space systems embedding Artificial Intelligence as it can run deep learning AI algorithms, for image processing in Space for example. It brings the technical benefits of pre-processing information at the edge and reduce the downlink bandwidth when sending to the ground. The typical end applications of QLS1046-Space include:

- Communication Satellites / Constellations, embedding AI / Security
- Landing and avionics space systems, Robotics and control of mechanical arm
- Human Mission Exploration, Science Missions
- Early Warning, Observation Satellites - Security / Automated situation detection & awareness / AI
- Defense In Space
- High bandwidth Space Observation
- Meteorological Satellites

LS1046-Space is a Quad-Core ARM Cortex-A72 based processor, running at up to 1.8GHz and featuring 30k DMIPS computing capabilities, ECC-protected L1 and L2 cache, and a rich set of peripherals such as packet processing acceleration, 1/10 Gb Ethernet, PCIe® Gen3, SPI, I²C, UART. It is qualified for Space up to Level 1 (NASA EEE-INST-002 - Section M4 – PEMs & ECSS-Q-ST-60-13C).

DDR4T04G72 is a 4GB Radiation Tolerant DDR4 Memory Multi-Chip Package (MCP), capable to reach up to 2.4GT/s. It is qualified for Space up to Level 1 (NASA EEE-INST-002 - Section M4 – PEMs & ECSS-Q-ST-60-13C).

Figure 2: LS1046-Space, DDR4T04G72, QLS1046-Space

The following sections present the results of the radiation testing campaigns performed to characterize the QLS1046-Space module. Since the module features two active devices, the testing strategy applied was to irradiate the components one at a time to characterize their radiation performance independently. For each test, the setup is first presented, and then a highlight of the main results is provided. A summary of all results obtained is given, but a particular focus is realized on the protons testing and results, since it is the latest test campaign performed.

SEE - HEAVY IONS, INCLUDING SEL

LS1046-SPACE PROCESSOR

The test setup used is composed of 3 different boards. The "STB026" allows to log the data (voltage/current) and reset/reboot the board latch-up management. The "DIB430A" features the QLS1046-Space module and realizes the essentials functions to operate it (Memories, Clocks, ...). The "DIB378A" features the peripherals and performs the interface with the rest of the system. A computer is used to manage the test setup and to store all the data timestamped by the FPGA.

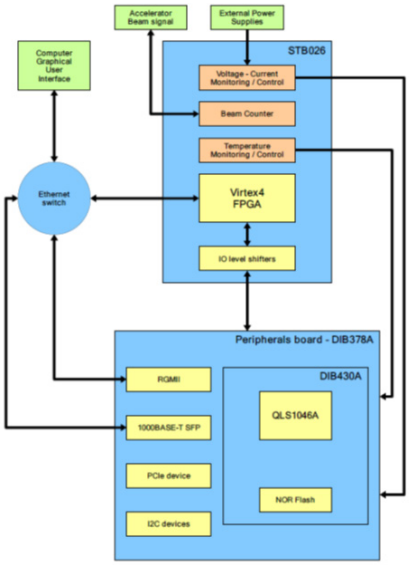

Figure 3: Test Setup for SEE of QLS1046-Space

During the test, the CPU communicates with the test board using different interfaces. One UART is used for generic purposes and debugging. Another UART is used for heartbeat and boot detection. The flash controller of the processor (IFC) is used to send test data from the CPU to the FPGA, and to get the test configuration from the FPGA. Two Ethernet links (one SGMII and one RGMII) are connected to the FPGA so that these interfaces can be tested. The CPU test software is configured by the FPGA to select dynamically the interfaces and peripherals exercised during the radiation testing. The CPU sends periodically some heartbeat to the FPGA though UART. The FPGA monitors the CPU activity and can initiate actions if a SEFI is detected, i.e. when the heartbeat stops. In case of SEFI, a simple algorithm is used to classify and cure the SEFI condition as shown on Figure 4. This allows classifying the SEFI events by recovering method.

Figure 4: SEFI classification flow

Since the LS1046 processor has a flip-chip construction, the test samples were thinned to allow the radiation beam to interact with the active part of the die. Tests were performed at RADEF facilities [3], and effective LET at surface of the samples is shown on Figure 5.

Latch-up testing (SEL) was performed at maximum operating temperature of 125°C and maximum operating voltage. Three devices were tested up to a fluence of 1e7 ions/cm². No permanent damage induced by a SEL was recorded while the devices was hit by an ion beam with a LET of 62 MeV/(mg/cm²).

16.3 MeV/n cocktail in air			
Ion	Range	LET at surface	LET in air and through 75µ of Silicon
	microns	MeV/(mg/cm²)	MeV/(mg/cm²)
17O6+	481	1.52	1.8
20Ne7+	360	2.3	2.6
40Ar14+	264	7.2	8
57FE20+	214	13.3	16
89Kr29+	185	24.5	32
126Xe44+	157	48.5	62.5

Figure 5: Effective LET

For SEU and SEFI testing, characterization was also performed up to 62 MeV/(mg/cm²), at normal operating voltage and room temperature. The CPU SEFI cross-section resulting of the testing of the device was calculated and some simulated error rates are given in Table 1. An important result is that no power cycle was required to recover from a SEFI event.

Orbit	GEO (35784 km)	GEO (35784 km)	ISS 51.50 400 km;400 km	ISS 51.50 400 km;400 km	Proba 2 99.28 720 km	Proba 2 99.28 720 km
Magnetic weather	quiet	quiet	quiet	quiet	quiet	quiet
trapped protons	AP8min	AP8min				
solar conditions	solar min	flare (worst day)	solar min	solar worst day	quiet	solar worst day
shielding	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²
SEFI/day	0.01	11.70	0.00	0.01	0.01	2.61

Table 1: SEFI Error rate (OMERE 5.3 with CREME 96)

Regarding SEU performance of the L2 cache and on-chip RAM, the cross section was also drawn, and error rates are drawn on Table 2.

Orbit	GEO (35784 km)	GEO (35784 km)	ISS 51.50 400 km;400 km	ISS 51.50 400 km;400 km	Proba 2 99.28 720 km	Proba 2 99.28 720 km
Magnetic weather	quiet	quiet	quiet	quiet	quiet	quiet
trapped protons	AP8min	AP8min				
solar conditions	solar min	flare (worst day)	solar min	solar worst day	quiet	solar worst day
shielding	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²
SEU/day	0.20	176.00	0.04	0.75	0.11	40.20

Table 2: SEU Error rate (OMERE 5.3 with CREME 96)

Previous SEU/SEFI results characterize the performance of the cores of the processor. The relevant peripherals of the LS1046 were also extensively tested, for instance DDR4 controller, PCIe interface, SPI, ... Because of the number of results, these are not presented in this paper but are available in the corresponding radiation reports.

DDR4 MEMORY DDR4T04G72

The DDR4 memory was tested in two ways. On one hand, it was tested at QLS1046-Space module level, with the same setup as the one described in the previous section (Figure 3). It was also tested in single die configuration, to get fine visibility of what is happening under radiations. Single die testing was performed connecting a SODIMM daughter board to a monitoring system dedicated to test DDR4 memories (Figure 6). In this setup, the memory is interfaced directly to a FPGA, and the power supplies are monitored to detect SEL:

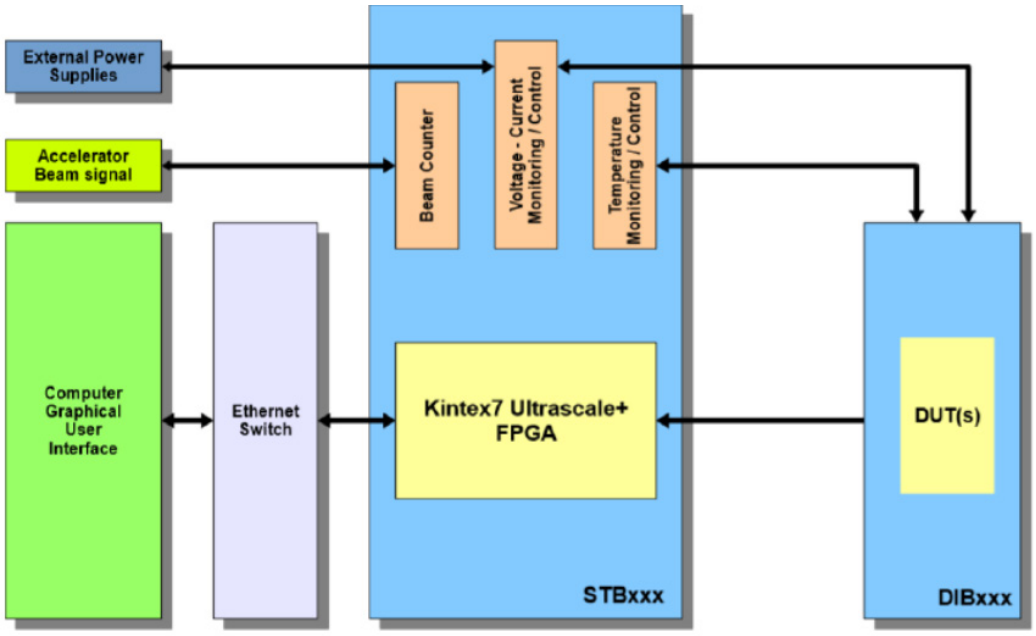

Figure 6: Test setup for DDR4 in single die

SEL testing was performed at RADEF with the single die setup at maximum supply voltage and operating temperature of 95°C. No SEL event was detected for a LET up to 60 MeV/(mg/cm²). SEU/SEFI were also characterized with the same setup, using two test modes, one static and one dynamic, as depicted on Figure 7. These tests were performed at nominal voltages and room temperature.

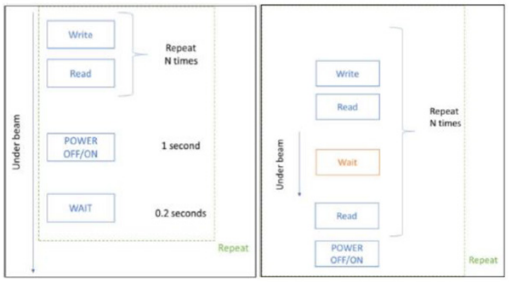

Figure 7: Dynamic mode (left) and static mode (right) test principle

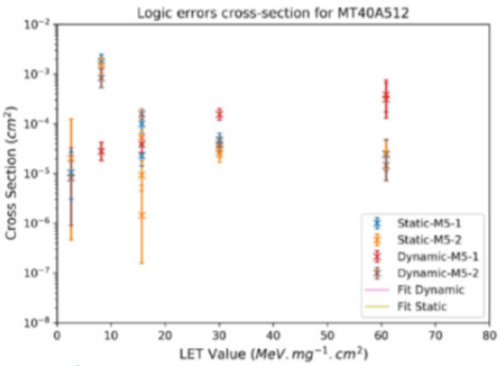

Figure 8: Logic errors cross-section at single die level

Row and column errors are logic errors where a high number of addresses are in error in a single row or column. SEFI, row and column errors were accounted as "logic errors", and resulting cross-section is shown on Figure 8. SEU were also counted, and associated cross-section was drawn.

SEU and SEFI on the DDR4 were also tested at QLS1046-Space module level. Figure 9 shows the resulting SEU cross-section. SEFI classification was performed, and it was demonstrated that a DDR4 reset is sufficient to clear all SEFIs up to a LET up to 25 MeV/(mg/cm²).

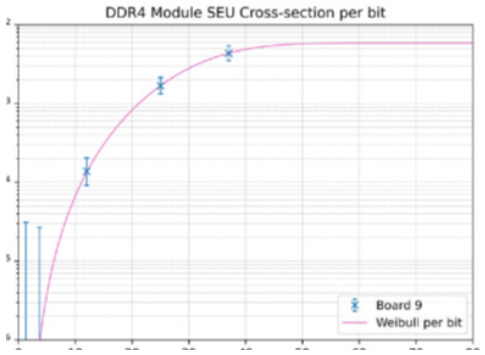

Figure 9: SEU cross-section at module level

An additional test campaign was performed with the single die setup to evaluate mitigation techniques. One technique tested to cure the logic errors consists in resetting simultaneously the DDR4 and the FPGA DDR4 controller. Table 3 shows that for SEFI-free iterations, a large majority of logic errors (LE) were healed after reset. For instance, on RUN006, out of 30 iterations presenting LEs, 29 were successfully recovered. On top of that, even though no refresh was performed during the reset time, the data content was kept safe. This means that in case of logic error, the application could resume immediately to normal operation after applying reset.

RUN	Fluence (ions.cm^{-2})	Iterations with LE Pre-Reset	Iterations with LE Post-Reset	LE on R1	LE on R2	LE on R3 (post-Reset)
RUN003	2.22E+05	13	1	84	83	1
RUN006	6.52E+05	30	1	217	217	1

Table 3: Logic errors recovery using reset

During the different heavy-ions test campaigns, few stuck bits were detected, and it was seen that they tend to heal over time when the memory is not irradiated.

SEE / PROTONS

All protons testing were performed at room temperature and with nominal operating voltages.

LS1046-SPACE PROCESSOR

For protons testing of the LS1046, a beam with a primary energy of 190MeV was used, leading to a maximum beam energy of 187MeV on the two samples. The test method and setup were the same as for heavy ions (Figure 3 and Figure 4). When a SEFI was detected, the beam was stopped until the CPU generated its heartbeat. The software includes routines for testing both on-chip RAM and L2 cache memory. Tests were performed with and without the ECC protection on the L2 cache, and results are given in Table 4. For the on-chip RAM, ECC is always enabled.

Run number	Fluence [cm^{-2}]	Duration [s]	Energy [MeV]	Board id	SD card image	Test mode	L2 cache				OnChip RAM				Effective fluence [cm^{-2}]	L2 SBU cross-section [cm^2]
							SBU	MBU2	Large errors	Large errors (data = 0)	SBU	MBU2	Large errors	Large errors (data = 0)		
RUN005	1.00E+11	1200	187	1	21h27	ECC off	4158	1	0	183	0	0	0	3	9.82E+10	4.24E-08
RUN006	1.00E+11	1117	187	1	21h24	ECC on	0	0	0	0	0	0	0	3	9.27E+10	0.00E+00
RUN007	6.79E+10	790	100	1	21h24	ECC on	0	0	0	0	0	0	0	3	6.48E+10	0.00E+00
RUN008	1.00E+11	1153	100	1	21h27	ECC off	4492	0	1	205	0	0	0	1	9.58E+10	4.69E-08
RUN009	1.00E+11	1190	100	5	21h27	ECC off	4251	0	0	198	1	0	0	1	9.43E+10	4.51E-08
RUN010	1.00E+11	852	187	5	21h27	ECC off	3893	2	2	165	1	0	0	0	9.74E+10	4.00E-08
RUN011	1.00E+11	1046	187	5	21h24	ECC on	0	0	0	0	1	0	0	1	7.11E+10	0.00E+00
RUN012	1.00E+11	1208	100	5	21h24	ECC on	328	0	0	15	0	0	1	2	9.28E+10	3.53E-09
RUN013	1.00E+11	1134	30	5	21h24	ECC on	0	0	0	0	0	1	0	2	8.60E+10	0.00E+00
RUN014	1.00E+11	1287	10	5	21h24	ECC on	1	0	0	1	1	0	0	1	8.70E+10	1.15E-11
RUN015	9.06E+10	1364	10	5	21h27	ECC off	3134	0	0	184	0	0	0	44	7.45E+10	4.21E-08
RUN021	1.00E+11	1538	30	5	21h27	ECC off	5045	1	0	221	0	0	0	3	7.32E+10	6.89E-08
RUN022	1.00E+11	1386	30	1	21h27	ECC off	4710	2	2	253	0	0	0	1	9.16E+10	5.14E-08
RUN023	9.68E+10	1547	10	1	21h27	ECC off	3729	2	0	164	0	0	0	4	8.57E+10	4.35E-08

Table 4: Protons results on LS1046-Space

SEU were observed on both the on-chip RAM and L2 cache. These events were sorted in three categories, SBU (Single Bit Upset), MBU2 (2 bit upset), and large errors (high number of errors in a short period of time). Few SBU have been observed in the on-chip RAM, which is expected since it is always ECC-protected. When ECC is enabled, SBU don't appear in the L2 cache. This demonstrates that the ECC handles SBU. The exception is in RUN012, where "fortuitous SBU" were observed even though the ECC was enabled. An explanation is that the ECC got disabled by a SEU during the run. Figure 10 presents the L2 cache SBU cross-section when ECC is disabled.

Few MBU2 were also detected in both memories. CPU SEFI have been monitored, and their cross-section is on Figure 11.

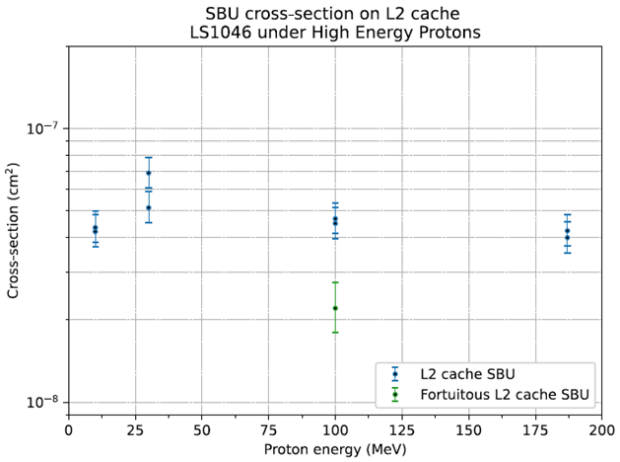

Figure 10: L2 cache SBU cross-section with ECC disabled

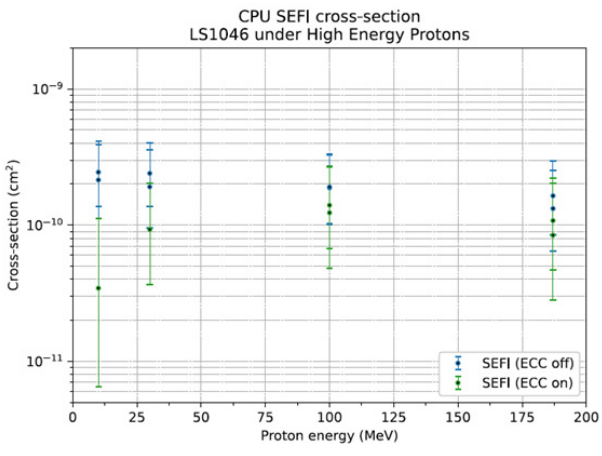

Figure 11: CPU SEFI cross-section

DDR4 MEMORY DDR4T04G72

The DDR4 protons testing was realized with the single die setup (Figure 6). A proton beam with a primary energy of 190MeV was used, and a maximum beam energy of 184MeV on the two samples. Table 5 shows the summary of the test results.

All upsets were Single Bit Upsets (SBU), meaning they should be correctable with the ECC. Figure 12 draws the upset cross-section for the DDR4 in protons. The results show a SEU sensitivity at all energies, in the range of 1e-20 cm^2/bit.

RUN	Proton energy (MeV)	Fluence (p+.cm^{-2})	Dose (krad)	Duration (s)	BoardID	Bits	Upsets	Upset cross-section (cm^2/bit)	Row errors	Column errors
RUN001	100	1.00E+11	9.34	1477	6	8,589,934,592	7	8.15E-21	6770	692
RUN002	190	1.00E+11	6.00	1493	6	8,589,934,592	5	5.82E-21	5144	418
RUN006	190	1.00E+11	6.00	1418	7	8,589,934,592	11	1.28E-20	17505	448
RUN007	100	1.00E+11	9.34	1414	7	8,589,934,592	10	1.16E-20	12075	374
RUN010	50	1.00E+11	15.82	1498	7	8,589,934,592	99	1.15E-19	14595	287
RUN011	30	1.00E+11	23.63	1572	7	8,589,934,592	10	1.16E-20	10024	216
RUN012	30	1.00E+11	23.63	1429	6	8,589,934,592	10	1.16E-20	8148	392
RUN013	50	1.00E+11	15.82	1487	6	8,589,934,592	2	2.33E-21	8665	544

Table 5: Protons results on DDR4 memory

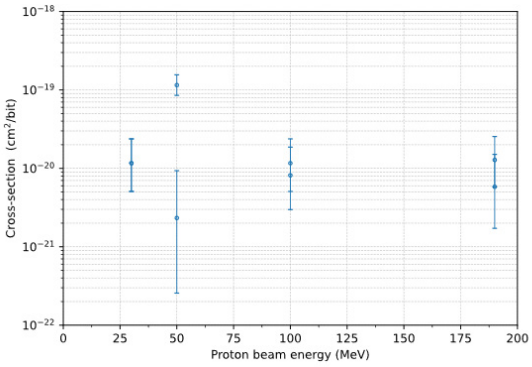

Figure 12: DDR4 SEU cross-section

All row and column errors were recovered by the reset mitigation technique that was previously successfully applied for heavy ions. Under protons, some stuck bits were also appearing over time in the DDR4 memory.

TID

TID testing has been performed both on the LS1046 processor and the DDR4 memory separately. To ensure a full test coverage during electrical tests, Teledyne e2v uses his own industrial tester facility, the UltraFLEX test system. This digital tester is also used for the parts production, and it provides a 100% test coverage fitted with NXP, the original LS1046A manufacturer.

For the LS1046, 6 samples were biased ON using a dummy software and 6 samples were biased OFF with all pins connected to ground on a dedicated bias board with socket. The test was carried out with electrical measurements conducted in the 'not in-flux' method according to [1]. Test was performed up to a dose of 100krad(Si), and all the LS1046 samples successfully passed electrical tests.

For the DDR4 memory, the test method is the same as for the processor, 5 samples were Biased ON and 5 samples were Biased OFF. Testing was also performed up to a dose of 100krad(Si). The Teledyne e2v's DDR4T04G72 memory has been evaluated and set as a suitable part for space applications up to a total ionizing dose of 100krad(Si).

CONCLUSION

This paper has discussed the radiation strategy applied by Teledyne e2v on its QLS1046-Space processing module. A short summary of the test results has been presented to demonstrate the good level of radiation performance obtained with this Radiation Tolerant processing module. Detailed results are available in the official radiation reports, which are available upon request from Teledyne e2v. With the full radiation reports, the radiation experts and system engineers can predict the behavior of their system when exposed to radiations.

REFERENCES

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[3] RADEF radiation testing facilities https://www.jyu.fi/science/en/physics/research/infrastructures/accelerator-laboratory/radiation-effects-facility

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