WHITE PAPER

Can deterministic digital phased array control be delivered over fiber?

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INTRODUCTION

This is the first publication in a short series, reporting progress at Teledyne e2v to replace copper with fiber as the physical transport layer, connecting data converters to digital signal processors. The goal is to substantially simplify high-throughput data converter interconnect to enable remotely positioned converters. In so doing, data and critically control signals, are reliably routed over substantially longer distances than commonplace today. Exploiting lightweight optical fiber is seen as the key here, opening microwave RF systems to future innovation. Such an approach can be particularly advantageous in phased array systems.

Combining high sampling bandwidths extending into the Ka-band with decreasing power consumption and improved size means modern data converters are already poised for co-location with sensitive RF antenna arrays. This could signify an important next step towards building commercially viable digital phased array systems.

According to Teledyne e2v's engineers, achieving these aims stimulates further development of the ESIstream protocol. As proof of concept, they will design a low-cost coding engine able to aggregate all control signals that are subsequently encoded and serialized by applying the ESIstream protocol. Low-cost FPGA code engines will sit at opposite ends of the optical link, bridging data between a target converter such as the forthcoming EV12PS640 or EV12DD700 and their associated DSP modules.

This initial exploration explains the context, challenges, and implementation plans, results will follow later.

Benefits of Fiber

- Long distance communication >> 20 m
- Reduced weight, increased data density
- Enhanced performance – No crosstalk, Zero EMI
- Level of future proofing of the backbone infrastructure

OBJECTIVE

This project sets out to explore the capabilities and limitations of a prototype optical data link bridge. Four categories of system signals are to be transferred via fiber namely: the reference clock, sample data, control data (including SPI and GPIO) together with a synchronization signal to ensure deterministic sampling. Phased array and beam forming systems require sample phase precision; that precision determines spatial accuracy. For this reason, it is paramount to maintain determinism. Therefore, a critical success factor will be establishing a robust methodology that extends Teledyne e2v's SYNC chaining[1] feature across the optical link.

This high-level, precision problem is not dissimilar to one already identified in past advanced scientific research. Projects including CERN's large hadron collider (LHC) were challenged to deliver precision synchronization across distributed experiments connected by ordinarily non-deterministic ethernet. In this case, a special protocol - White Rabbit emerged.

In Teledyne e2v's data converter world, determinism is solved by a novel approach. SYNC chaining allows a massively parallel system of converters to maintain deterministic synchronization throughout. What is a relatively straightforward approach to implement over copper, certainly becomes more challenging in shifting to fiber.

This project will evaluate prototype performance and identify any performance effects introduced by temperature and other environmental factors. In the initial experimental phase, it is assumed the physical fiber link is twenty

[1] Synchronization Chaining, Simplifying Multi-channel Synchronization in Gigahertz Data Converters.

metres long – enabling significant separation between the RF analog and data processing components. The project is helpfully aided with technical contributions from Radiall[2] who have also supplied the electro-optical transceivers used.

Market Demand and the Benefits of Fiber

How does fiber benefit future system architecture and what are the key motivations for such a paradigm shift?

Table 1 highlights some of the differences between conventional RF copper coax and optic fiber. Most benefits fall to fiber, but for two that still slow its adoption in RF systems - namely cost and install complexity. Even so, complexity combined with space means that there is considerable pent-up demand to deliver a practical fiber solution. For Teledyne e2v, this means finding a viable solution to deliver control signals via fiber. One potential approach already exists at the company in the form of the license-free data serialization system ESIstream.

Feature	Fiber	Coax
Cable composition	Plastics and glass inner fiber	Metal foil, copper braid and plastic insulation
Cable losses	Dispersion, bending, absorbtion	Resistive, radiated and dielectric
Weight	Light	Relatively heavier
Diameter	Thin (125µm)	Thicker
Transmission rate/data density	>> Gbps/extremely high	~Mbps/modest
Noise immunity	High	Low
Bandwidth (modulation dependant for both types)	THz	~750 MHz
Attenuation	0.4 dB/km (optical wavelength dependant)	6 dB/30m (signal frequency dependant)
Installation challenge	Hard	Easy
Relative cost	High	Low

Table 1 Fiber and copper coax features assessed

Optical Harness Principle of Operation

Optical links might ease system complexity. However, standing in the way of this goal are a couple of thorny engineering problems:

1. Ensuring that the optical link reliably transports slow control signals and most importantly,
2. That fiber can deliver error-free, deterministic clocking to remote converters ensuring synchronous operation.

The solution proposed (figure 1) takes low-cost, low-power FPGA encode/decode engines to aggregate, format and code serialized control vectors generated from system GPIO or SPI messages. Signals derive from existing high speed data converters; high-end 12-bit devices such as the EV12PS640 ADC or the EV12DD700 DAC. Both evaluation systems conveniently exploit the FPGA mezzanine connector (FMC). In the prototype created, the FMC physical link is broken and two further FMCs (identified as the green blocks in figure 1) are rigged with optical links. Four dedicated CML lanes will carry control signals (GPIO), four LVDS lanes convey system clocks.

The availability of license-free ESIstream provides an ideal interface for the resilient coding of control signals creating a future-proof, universal optical interface ideal for remotely located data converters.

[2] https://www.radiall.com/products/active-optics.html

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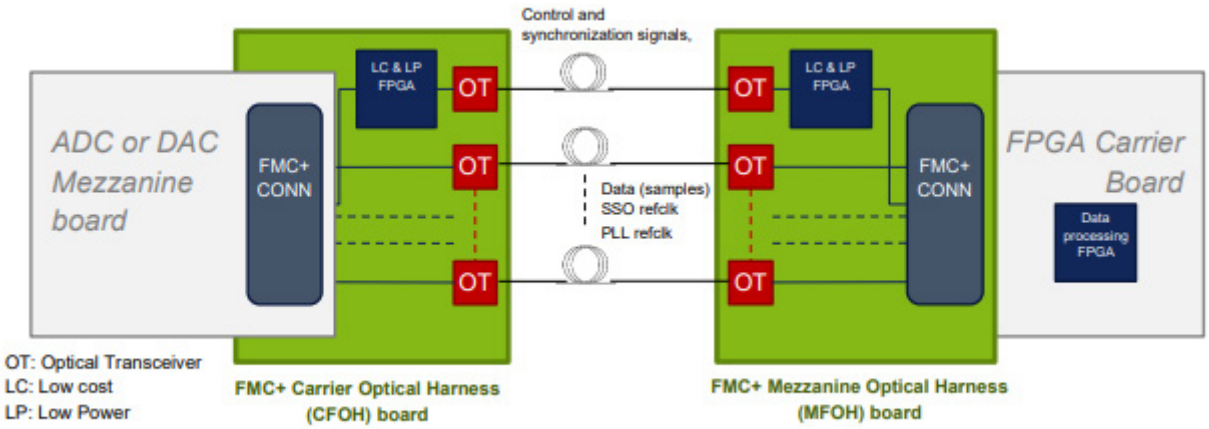

Figure 1 - Block diagram of the FMC optical harness

Background to Digital Phase Shifting

Digital phase shifting for beamforming enables the accurate steering of RF signals allowing multiple frequency bands to be used for multi-target tracking in radar applications for example. Besides the obvious flexibility provided by digital phasing, there are inherent performance reasons to embrace digital arrays. For one, analog phase shift is hard to achieve, digital phase shifting brings much needed phase precision to beamforming for improved sidelobe rejection.

Traditionally, the biggest impediments to building fully digital arrays were size, power consumption, and processing power. Each array element requires the RF signal path electronics to be co-located with the array for spatial accuracy. Physically, circuit elements (the data converters and associated analog components) need to be small enough so that each channel can be sited half a wavelength apart. X-band demands a spacing less than 20 mm placing significant space constraints on the signal path electronics. Moreover, tight spacing raises thermal management concerns, driving a need for much reduced power consumption.

Glossary of terms

- ADC – Analog to digital converter
- CML – Current mode logic
- DAC – Digital to analog converter
- LVDS – Low voltage differential signaling
- FPGA – Field programmable gate array
- GPIO – General purpose I/O
- GT – Gigabit transceiver
- RDC – Running disparity counter
- SPI – Serial peripheral interface

A further challenge in pulling off such sophisticated design, centers on the routing and transfer of data and GPIO control signals. This is particularly impactful, given the density of signaling required for each array and is largely impractical and uneconomic if the design must rely on copper interconnect.

Data serialization is widely used with high-performance converters, yet it remains rare for optical links to prevail over copper. Even so, it is expected that as direct RF conversion extends to higher microwave frequencies, the benefits of fiber may rapidly supersede copper. However, data path innovation is key for this to happen!

Previous Relevant Experimental Work

Before starting this project, some efforts to establish the state-of-the-art were made. One initially promising article[3] from Texas Instruments described the use of fiber based JESD204B in a phased array application.

[3]JESD204B over optical fiber enables new architecture for phased-array radars by Mike Guibord.

Interestingly, this project only describes replacing data lanes with fiber. To achieve deterministic latency or transfer control signals, the author apparently falls back on traditional copper as a simpler approach. There seems to be no specific justification beyond 'simplicity' for overlooking the control signal aspect.

A second article[4] from Lincoln University in the UK, describes an FPGA project used to aggregated SPI and GPIO data, sent via a high-speed optical link. The article provides insights into coding choices for extended transmission distances and illuminates the challenges arising. The key conclusions were:

- Care in establishing link synchronization is demanded, necessitating a reference clock
- Encoding is key to success. In this case, 8b/10b coding proved orders of magnitude better than other simpler schemes (such as XOR, or Grey codes).
- Finally, if latency is a significant issue, the authors demonstrated how the link could be re-synchronized to compensate for known latencies.

Finally, as hinted earlier, scientists challenged to achieve determinism in nuclear physics research environments developed a synchronous ethernet approach using the White Rabbit[5] protocol delivering precision, sub-nanosecond timing.

Implementation Overview

The FPGA code engines are shown in figure 2 (purple outlined blocks). The link is to be clocked by the 100 MHz reference provided by the signal processing FPGA. A synchronizing pre-amble is required to establish link operation and once completed, serialized control vectors will be produced by the transmit code engine. ESIstream encoded vectors are then passed across the link via fast gigahertz CML transceivers. Received vectors will be decoded in the receive code engine and routed appropriately to the connected converter.

Circuitry in addition to the FPGAs will be required on the FMC extender cards. For instance, local power management to supply the FPGA. Clock conditioning and distribution is also needed at the encode end of the link.

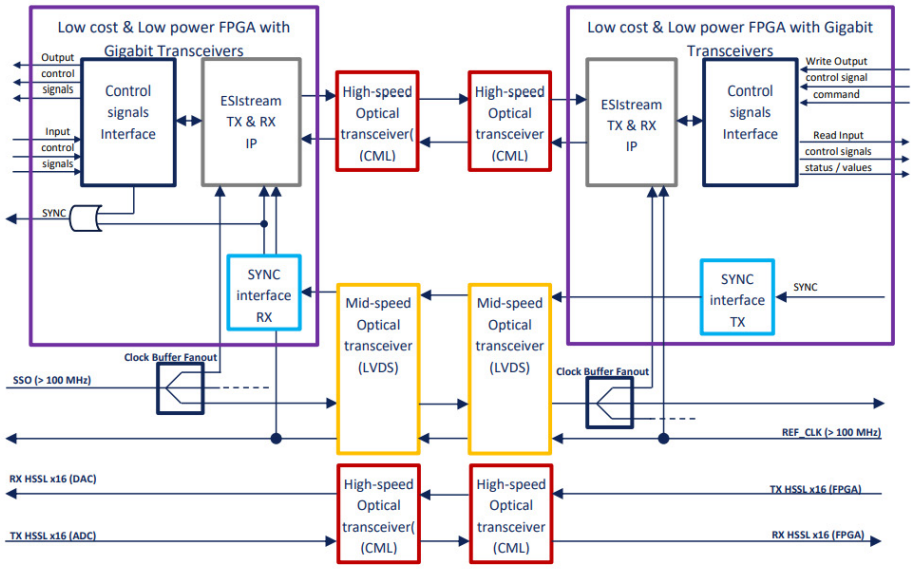

Figure 2 - Detail of optical link showing FPGA based optical coding engines

[4] Low Cost FPGA Implementation of a SPI over High Speed Optical SerDes by Peter Hobden & Saket Srivastava.

[5] The White Rabbit Project - various authors, Proceedings of ICALEPCS2009, Kobe, Japan.

ESIstream Provides a Control Data Coding Approach

As a license-free, efficient, and simple serialized point to point data interface, ESIstream[6] already lends itself to optical deployments. Like other alternatives, ESIstream (figure 3) relies on CML serializers. It uses a 14b/16b encoding algorithm with pseudo random binary sequence (PRBS) encoding to scramble data which is then combined with a disparity bit to ensure a stable DC balanced link. A second overhead bit is specified as a clock bit which enables the far end of the link to monitor and maintain link synchronization lock.

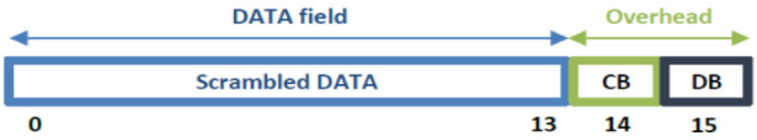

Figure 3 - ESIstream data packet

After scrambling, the resulting 14 bits of data are encoded into a 16-bit data packet in the following manner. The first overhead bit, the clock bit (CB) toggles on consecutive frames. The second disparity bit (DB) is set depending on the state of a continuously running disparity counter (RDC). Two RDC scenarios arise:

1. RDC is less than +/- 16 then the disparity bit has its value set to '0'
2. RDC exceeds +/- 16, then the disparity bit is set to '1' and the data packet is inverted (a bit-to-bit NOT operation is performed)

This disparity behavior satisfies the demand for a minimal number of transitions for the receiver's (decoder) phase locked loop to maintain lock whilst maintaining dc balance. Under normal circumstances, the receiver checks the DB first. If it is set high, then the received data is inverted prior to de-scrambling.

For deterministic operation, ESIstream link set-up demands that the link be synchronized, i.e. data frames are properly aligned between transmitter and receiver. Link synchronization is established in two operational steps:

1. Initial frame alignment takes place, followed by
2. PRBS scrambling starts.

An attractive feature of ESIstream is that it eliminates a complex diversity of record formats resulting from supporting a diversity of data framing options and bit packing demanded the JESD204 alternative industry standard approach. The JEDEC alternative (JESD204B & C), forced as it is to cater to a variety of use cases and different resolution converters, means data frames become hard to debug, latency increases, and en/decode IP becomes increasingly complex and a resource hog.

ESIstream on the other hand is proven, low resource IP solution to code and transfer serialized control vectors.

Prototype Hardware Infrastructure

The right optics

The planned demonstrator uses Radiall optical transceivers. Device configuration registers accessible via I2C are available and offer relevant information such as temperature and optical power. Equally, pre-emphasis and equalizer characteristics can be tuned if loss of transmission is detected, helping with system debug.

Radiall's rugged D-light portfolio offers three data rate grades (10 Mbps, 5 & 12 Gbps) together with multiple package options. These optical components are configured either as four-channel duplex transceivers or 12-channel simplex for receiver and transmitter applications. D-Light is protocol agnostic and offers standard LVDS and CML electrical interfaces.

[6] ESIstream is the Efficient Serial Interface as described in detail at ESIstream official.

Low-cost, low-power logic

A suitable FPGA option combing economy with low power and a gigabit transceiver capability (at least one CML lane) to implement the control signaling is needed. The Xilinx Artix 7 FPGA is a solid choice. Arguably, lower power options exist, but power optimization is not a central goal in the initial phase.

From a project management perspective, development speed is critical, so the use of existing, commercially available FPGA modules is preferred over building a new, full-blown FPGA module. Accordingly, suitable FMC development boards were tracked down. One option, from Trenz Electronic (the TE0712-02-71I36-A) has been selected for the initial code development.

Auditing existing copper interconnects and establishing concept viability

Checking datasheets for the EV12PS640 and EV12DD700 reveals a count of unique control and reference clock signals required for a functional system design as called out in table 2. Serial clocks will be transferred via LVDS links. Meanwhile, the serialized control record will make use of a single CML lane of the Artix 7 FPGA.

From the tabulated information, it is straightforward to define the minimum control record length (in bits) required for serialization. A maximum of 48 control bits must be serialized to support the EV12DD700. Thus. in the context of ESIstream's 14b/16b encoding, a quad word control record length (i.e. 64-bit) is the natural choice, leading to a data rate of 6.4 Gbps @100 MHz reference clock. The record length leads to a continuous data rate comfortably within the limit (6.6 Gbps) of the Artix 7's gigabit transcievers.

Auditing device interconnects (non-power)	EV12PS640 (Microwave ADC)	EV12DD700 (Microwave DAC)
Clocks		
Total Refclock lanes (LVDS)	1 lane	1 lane
Synchronization lanes (LVDS)	1 lane	1 lane
Control bits		
Control signals (bits) to FPGA total	32 bits	44 bits
Other ref clocks (SSO2P, SSO3P, CLKoutB)	3	4 (adds SSO)
Minimum control record length	32 + 3 = 35 bits	44 + 4 = 48 bits

Table 2 Audit of control signals

Providing System Wide Deterministic Synchronization

Sync chaining has been documented in several articles over the last few years, and as stated in the introduction is probably one of the most critical success factors for this project if a truly useful optical alternative to copper is to emerge.

The challenge in transitioning to SYNC over fiber is that, as implemented today, the SYNC signal is flagged by a relatively slow, 10ns level change. It is not to be confused with the SYSref clock in JESD204 implementations. Given the 'un-clocked' nature of SYNC, how can the precise timing be maintained over the fiber?

This is where Manchester coding steps to the rescue. Manchester coding is a simple and early computer era, phase-shift keying method of coding. Binary data controls the phase of a clock (figure 2); effectively it ensures either a positive or negative going mid-bit transition; maintaining DC balance and providing a regular source of data edges to maintain link lock at the remote end of the cable/fiber.

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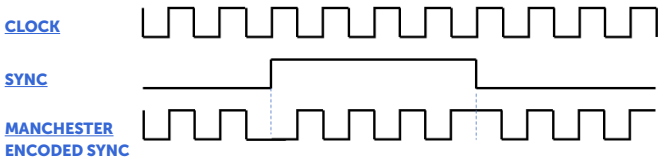

Figure 4 - Manchester encoding ensures mid-bit transitions and DC balance

Manchester is easily implemented by exclusive OR-ing (XOR) the SYNC signal with the reference clock. Even though there may be a steady stream of zeros preceding SYNC assertion, the receiver will register within half a bit period the low to high transition. Latency through fiber is orders of magnitude lower than copper, so adjusting for differing travel times in multi-array systems should prove a vanishingly small activity for most practical applications.

Next Steps

The work described, leverages previous learnings that melds practical and 'proven with copper' methods to transform real-time copper signaling into the sampled time domain for optical transmission. Teledyne e2v engineers are confident in their experimental approach but formal results are pending the completion of the prototype hardware and HDL code creation. Initial project results should emerge early in 2022.

Conclusion

The inherent simplicity and resource efficiency of ESIstream provides a useful and straightforward protocol layer that will support not only sample data transfer over fiber but importantly the transfer of control data. Moreover, a working assumption for this prototype is that a simple solution, Manchester coding, facilitates the transmission of the SYNC chain; critical in maintaining deterministic synchronization. For the time being, these observations remain theoretical, but they will soon be fully evaluated with results reporting to follow soon.

Assuming the initial experimental work is successful, in addition to conventional data lines, each converter node requires two extra LVDS compatible lanes as well as one CML transmit and receive lane pair (read & write) for the aggregated control signaling. Given the large number of data lanes already required, this represents a small cost penalty, especially given that it frees system design to extend communication across significant separations between the front-end and signal processing blocks.

Teledyne e2v welcomes enquiries from companies about this project, especially those interested in fully assessing the outcomes of the experimental work described here. The company can also provide more technical details about both data converters mentioned here.

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For further information, please contact:
Romain Pilard,
Applications Engineer,
Signal Processing Solutions
romain.pilard@teledyne.com

TELEDYNE e2v
Everywhereyoulook™

For further information, please contact:
Stéphane Breysse,
Applications Engineer,
Signal Processing Solutions
stephane.breysse@teledyne.com

TELEDYNE e2v
Everywhereyoulook™

For further information, please contact:
Nicolas Chantier,
Marketing Director
Signal and Data Processing Solutions
nicolas.chantier@teledyne.com

TELEDYNE e2v
Everywhereyoulook™

For further information, please contact:
Jane Rohou,
MarCom Manager.
jane.rohou@teledyne.com