WHITE PAPER

Radiation Mitigation Techniques for Teledyne e2v's Digital Processing Space Products.

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ABSTRACT

State-of-the-art radiation tolerant CPUs and Memories utilize design and fabrication techniques that are impacted by harsh radiation environments in Space. Single event effects (SEEs) arising from strikes from galactic cosmic rays, protons, or neutrons on these critical components, require radiation mitigation. Understanding and characterizing radiation-induced effects, within a particular radiation environment, is essential in order to outline a procedure for designing and validating Space systems using radiation-tolerant components, and to propose effective mitigation techniques. Utilizing the correct radiation mitigation techniques that account for variations in radiation environments and electronic components is critical in order to minimize cost and maximize system availability and throughput bandwidth with minimal errors incurred. During the design phase, modeling and error rate calculations must be understood to predict system performance requirements. Teledyne e2v offers state of the art radiation tolerant digital components with performance and functionality for operation under harsh radiation environments; providing a foundation for identifying radiation mitigation techniques that are suitable for Space, and for engineering modifications that would minimize system level radiation effects that would be necessary for current and future developments. This paper first introduces the general radiation effects that can be observed in semiconductors. Then, the typical radiation effects observed on the compute intensive Space products from Teledyne e2v are presented. Finally, the possible radiation mitigation techniques that can be applied to cope with these kinds of effects are proposed and discussed.

1. INTRODUCTION TO RADIATION EFFECTS IN SPACE

Radiation that impacts semiconductor performance is affected by process technologies, device geometries, circuit implementations, and the radiation environment in Space in which the devices are deployed (Low Earth Orbits (LEOs), Medium Earth Orbits (MEOs), or Geostationary/Geosynchronous Orbits (GEOs/GSOs)). Space contains three primary sources of radiation: Galactic cosmic rays, Solar radiation, and Radiation belts (regions surrounding the Earth where particles accumulate under the influence of the planet's magnetic field). The performance lifetime of semiconductor components within a particular radiation environment is characterized mostly by the total ionizing dose (TID) and the frequency of occurrences of single-event effects (SEEs). The radiation exposure of a deployed electronic system in Space is a function of the specific orbit, the mission duration, and the amount of shielding implemented. Ion fluxes near radiation belts have energy in the range of 0.1 to 10 MeV. This will penetrate the semiconductor package and will result in total ionizing dose (TID) effects and Single-event effects (SEEs). Specifically, radiation ions with kinetic energies in excess of 300 KeV have even more potential to penetrate semiconductors packaged in either plastic, ceramic, or metal and therefore upset the die.

Radiation impacts semiconductors in two ways: 1) Cumulative effects (aging from the passage of many energetic particles) or 2) Events due to the passage of a single particle. Cumulative radiation dose effects are quantified as the total ionizing dose (TID) caused by radiation induced charge generation and trapping within a particular device and are characterized by device parametric shifts that accumulate over time. Events due to the passage of a single particle or photon manifest in Single-event effects (SEEs) which are random/instantaneous disruptions.

SEEs result in either destructive or nondestructive anomalies. Nondestructive SEEs impose corruption in an output or data state that does not damage or destroy the semiconductor component. When a nondestructive SEE occurs, no external input is required to restore the state of the system once the nonequilibrium charge and its effects have recombined and are stable. Nondestructive SEEs include: SETs (Single-event transients), SEUs (Single-event upsets), SEFIs (Single-event functional interrupts), and some SELs (Single-event latch-ups) in which the maximum current is limited in such a way that component damage does not occur. Destructive SEEs impose corruption in an output or data state in which the semiconductor is damaged or destroyed. Destructive SEEs include SELs caused by an ion strike creating a low impedance/high current path resulting in permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off/on) is necessary to restore normal operation. In addition to destructive SELs, SEGR (Single-event gate rupture) and SEB (Single-event burnout) are also catastrophic mechanisms in which low impedance paths suddenly develop between power and ground and remains after the triggering event is over.

2. RADIATION EFFECTS ON TELEDYNE E2V'S DIGITAL PROCESSING SPACE PRODUCTS

Teledyne e2v characterizes samples of their radiation tolerant CPUs and memories with SEE campaigns being performed at an accelerator facility by irradiating the devices under energetic heavy ions and protons. With the DUT powered up and operating under normal conditions (except for SEL which is performed at maximum supply and temperature), supply currents and output states are monitored. The DUT is then bombarded with heavy ions or protons, and any momentary changes in supply currents or output states are recorded. Linear energy transfer is the amount of energy that an ionizing particle transfers to the device traveling per unit distance. LET depends on the ions and energies of the ion beam and therefore ions of different elements will also have different LETs. LET will have an impact on the probability of a SEE. The higher the LET, the more carriers generated in the silicon which increases the probability that the carriers will be trapped in the electric field thereby resulting in a measurable effect.

For digital devices, when irradiated, they are monitored for Single-Event Effects (SEEs) (which are any measurable or observable change in state of performance from a single energetic particle strike). SEEs include Single-event upsets (SEUs), Single-event functional interrupts (SEFIs), Single/Multiple-bit errors (S/MBEs), and Single-event latch-up (SEL). Monitoring for SEEs typically requires opening the package in order to expose the active region of the die. For instance, devices packaged with flip chip construction require removing the lid and thinning the die to approximately 75 microns for maximum radiation interactions.

In addition to SEE tests, TID testing is performed as follows: 1) Assemble units from the wafer into packages, 2) Electrically test the devices under test (DUTs) on automated test equipment (ATE), 3) Place the DUTs in a socketed board with half of them biased under normal operating conditions, and half unbiased 4) Expose the board to the radiation source and irradiate it to the rated TID level at room temperature and monitor, 5) Retest the DUTs on the ATE to verify that the units are still functional and that no critical parameters have drifted outside of the data-sheet limits. For its radiation tolerant components, Teledyne e2v typically targets a dose (TID) capability of 100krad and a latchup (SEL) immunity of at least 60 MeV.cm^2/mg. This allows to target up to GEO orbits. Even though the components have a capability to endure high radiations levels and dose, they still encounter SEU and SEFI events.

For memory products (for instance DDR4), word errors are usually detected (SBE and MBE) which include: 1) Row and Column, 2) SEFI, and 3) Stuck bits. For processor products (i.e. LS1046-Space), errors detected typically include: SEUs on cache memories, and SEFIs on cores and peripherals.

Fundamentally, it is important for Space/satellite development teams to understand exactly what types of errors a particular radiation tolerant Memory and/or CPU device may exhibit during Space flight operations. Obviously, devices that do not exhibit certain types of errors, do not require implementation of any mitigation techniques for those errors that never happen. Memory and processing devices that do exhibit certain errors do require radiation mitigation techniques in order to eliminate or reduce the error rate for optimal Space flight operations.

LS1046-Space example

SEU (core) cross-section

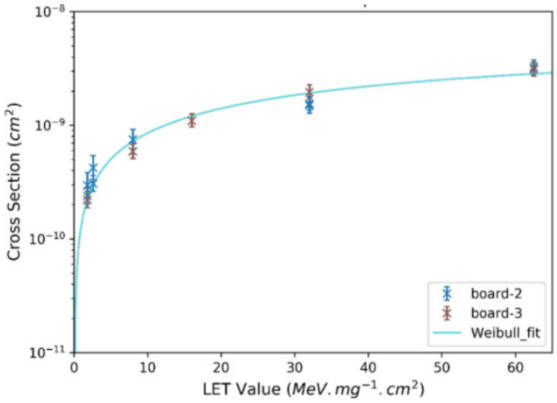

Figure 1 - SEU cross-section/bit - Weibull fit

Weibull parameters

A	5.09E-09
x0	0.1
s	0.81
W	80.16

Teledyne e2v calculates device SEE probabilities (i.e. SEU, SEFI, etc.) by plotting error cross sections versus LET and draws Weibull curves (Figure 1). In order to calculate error-rate predictions in orbit, the data is fitted to a Weibull curve. It may take several test campaigns to fully understand how a device responds to heavy-ion and protons radiations. Any major change to a product, such as a new silicon design or revision generally requires repeating the SEE characterization.

Figure 2 - QLS0146-Space Processing Module

Another example is the QLS0146-Space processing module (Figure 2). This processing module utilizes a LS1046-Space processor, combined with a high speed DDR4 memory. Multiple radiation testing campaigns have been performed to test and characterize the performance of the processor and the memory. For the DDR4 memory, four different types of events are observed: Isolated word errors, Row/ Column errors, SEFI events, and Stuck bits.

During the memory testing, the isolated word errors (Figure 3) are the errors due to local ion strikes on the memory cells, changing the state of one (SBE) or several (MBE) of their bits.

Figure 3 - Example of isolated word error

After characterization of the devices, orbit error rates can be calculated to provide estimates of the frequency of occurrence of events in certain conditions, without any mitigations. Table 1 shows an example of SEU error results for the LS1046-Space.

Orbit	GEO (35784 km)	GEO (35784 km)	GEO (35784 km)	ISS 51.50 400 km;400 km	ISS 51.50 400 km;400 km	ISS 51.50 400 km;400 km	Proba 2 99.28 720 km	Proba 2 99.28 720 km	Proba 2 99.28 720 km
Magnetic weather	quiet	quiet	quiet	quiet	quiet	quiet	quiet	quiet	quiet
trapped protons	AP8min	AP8min	AP8min						
solar conditions	solar min	flare (worst day)	flare (worst 5 min)	solar min	solar worst day	solar worst 5 min	quiet	solar worst day	solar worst 5 min
shielding	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²	1 g/cm²
SEFI/day	0.01	11.70	43.50	0.00	0.01	0.03	0.01	2.61	9.71

Table 1 - SEU Error Rates

3. POSSIBLE MITIGATION TECHNIQUES FOR DIGITAL PRODUCTS

Since the error rates obtained in characterization might not be low enough for certain applications, mitigation techniques can be implemented to further reduce the error rates and reach an acceptable performance or availability of the equipment. Radiation mitigation for Space/satellite developments require teams to select and implement radiation tolerant devices in conjunction with the latest state-of-the-art COTS technologies that balance the tradeoffs between performance versus practically. Space/satellite developments reside within two design methodologies: 1) Traditional: Which has low failure rates and pays high prices for radiation hardened by design (RHBD) components (uniquely designed to be resistant to damage and effects, as well as high levels of ionizing dose) and are built-for-purpose semiconductors that are typically considered to be far from state-of-the-art; and 2) New Space: Which is more focused on mission assurance and is willing to use radiation tolerant devices that utilize the latest technologies offering disruptive functional performance.

A semiconductor's radiation tolerance is dependent upon a variety of controllable and uncontrollable variables all of which may require radiation mitigation. Since errors will happen, it is important to design in radiation tolerant products with built-in error correction circuitry (ECC) that can also be utilized in redundant error correction circuit implementations if necessary. For instance, Teledyne e2v's QLS0146-Space processing module has been developed and characterized to be used in a variety of radiation mitigation techniques (both redundant and non-redundant) that can exhibit the required performance characteristics for a given radiation environment. In order to manage radiation effects, the typical mitigation technique required is to utilize the modules on-board ECC (Error Correction Circuit). The ECC uses a dedicated extra byte in the DDR4 memory such that the 72 bit word size of the memory is split into 64 bits of actual data and 8bits for the correction code. The ECC engine is built into the DDR4 controller of the LS1046-Space processor. Therefore, an ECC byte in the DDR4 memory behaves exactly as any other data byte; and the error mitigation is handled by the LS1046 processor. SBEs are detected and corrected by the ECC, hence ECC should simply be enabled to mitigate these errors. It is important to avoid the accumulation of SBEs (due to multiple ion strikes), which over time could lead to MBEs. The LS1046 also features a scrubbing engine that can sweep periodically across the entire DDR4 memory content, and correct the SBEs that occur.

Methods to reduce SEEs at the circuit level (multi-chip) are also utilized in order to solve radiation tolerant issues. Common circuit level design techniques include: 1) Increasing circuit drive capacity and providing drive redundancy, and 2) Adding additional circuitry for the detection and correction of bit errors. Error detection generally requires an additional bit in order to store the parity of each data word (regardless of word length). When a Single-bit upset (SBU) occurs, the parity of the data will not match the parity bit. Parity circuitry allows for the detection of a single bit error at minimal cost in both circuitry (and memory width). Unfortunately, implementing parity circuitry has two drawbacks: 1) It is only a detection system and unable to correct the error, and 2) Multiple-bit upsets (MBUs) cannot be detected and therefore can also reside in memory. This is known as silent data corruption.

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Today's radiation tolerant systems require increasing levels of reliability while at the same time avoiding silent data corruption and maximizing processor availability and overhead. System level architectures can be implemented with either dual-modular redundant (DMR - Figure 6) or triple-modular redundant (TMR - Figure 7) circuitry. These types of architectures enable the detection of SEU or SEFI errors in a logic path. For a DMR system, error detection happens when two outputs do not agree. In the case of TMR systems, error detection is accomplished by overruling the other two valid inputs to the majority voter. The TMR method uses two to three times the silicon area as an unprotected data path and requires specialized simulation tools to identify the critical logic paths. The most ambitious and expensive error detection and correction circuitry can also be implemented in the form of system-level redundancy. This requires using duplicate redundant processor cores – where multiple, identical cores run in lockstep (executing the same code at the same time). This is expensive in both area and power because the same computation and instruction flow runs on each redundant core. In addition to the aforementioned error correction techniques, data scrubbing is also utilized. Data scrubbing uses a background task to periodically inspect the main memory for errors and corrects the detected errors using redundant data. Data scrubbing reduces the likelihood that single correctable errors will accumulate leading to a reduced risk of uncorrectable errors and provide routing checks of all inconsistencies in the data and thereby preventing hardware and software system failures. Scrub rates are determined by the SEU rate (for example rates can be 1/day to 1/5000 days).

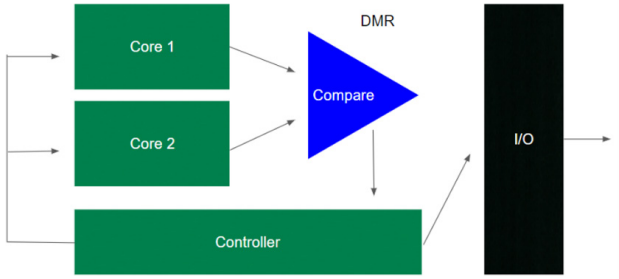

Figure 6

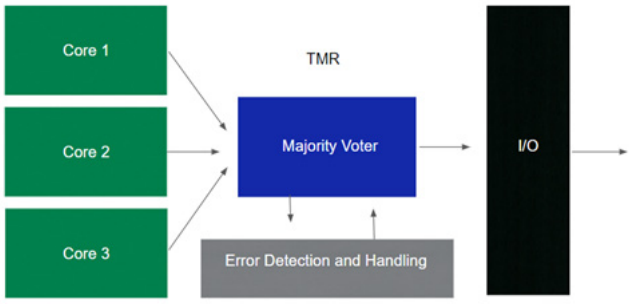

Figure 7

CONCLUSION

State-of-the-art CPUs and Memories continue to become more complex, and therefore become more difficult to test and more sensitive to radiation effects. Implementing new radiation mitigation techniques utilizing these devices is of strategic importance for the development of future Space flight systems. Device SEE errors must be characterized, and the error probabilities calculated, in order to understand the effects and implement the most effective radiation mitigation techniques. It is of the utmost importance to have accurate information about the various error rates and probabilities versus the radiation environment in order to minimize cost and maximize system availability and throughput bandwidth with minimal errors incurred. Teledyne e2v provides extensive information and support on all their radiation tolerant products for development teams. Dedicated radiation mitigation application notes are available to customers upon request.

TELEDYNE e2v Semiconductors

For further information, please contact:

Thomas Guillemain,
Marketing & Business Development,
Data Processing Solutions
thomas.guillemain@teledyne.com

TELEDYNE e2v Semiconductors

For further information, please contact:

Thomas Porchez,
Application Support,
Data Processing Solutions
thomas.porchez@teledyne.com