EV12AS200A
12-bit ADC Demo Kit

User Guide

This document provides a guide to the use of e2v's EV12AS200A (12-bit 1.5GSps ADC) Demo Kit.

Main Features

- 1.5 Gsps sampling rate of analog signals using EV12AS200A 12-bit ADC
- 1 differential input with 4 different configurations
  - Differential driver (2 types of amplifier provided)
  - Balun RF transformer.
  - Direct input.
- Clock Input:
  - External clock,
  - On board PLL (1.5 GHz)
- Interfacing ADC Digital outputs with an on-board FPGA
- Control and Acquisition Display using PC based GUI
  - FFT computation
  - Flexible and easy to operate via USB2
  - Programming of ADC settings
  - Programming of ADC environment
  - Monitoring of ADC currents and junction temperature
- Universal 12V power Adapter

Operating conditions

- Temperature range: 10℃ < Tamb < 40℃
- Operating with a Microsoft Windows PC environment (Windows 2000, Windows XP, Windows Vista, Windows 7) via USB interface.

Applications

- Demonstration and Evaluation of EV12AS200A 12-bit 1.5GSps analog to digital converter

EV12AS200A-DK

1 General overview

The 12-bit Demo Kit enables the easy evaluation of the characteristics and performances of 12-bit ADC EV12AS200A. The Demo kit is ‘plug and play’ and needs little external equipment.

The Demo kit is delivered with software which allows acquisition of data using the on-board FPGA.

This board is designed for use as a reference design.

All front end devices are fitted including: DC-DC regulator, ADC driver, clock generator…. (see chap 3 Main Functions)

The FPGA data acquisition program is provided (see chap 5 FPGA CODE). The vhdl source code is provided upon request to hotline-bdc@e2v.com.

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Its function is as a development system, demonstrating the performance of e2v semiconductors components and not as a final product available on general release.

Since this Development Kit is intended to be used on an industrial workbench and modified by the user to build his prototypes, NO WARRANTY OF ANY KIND can apply.

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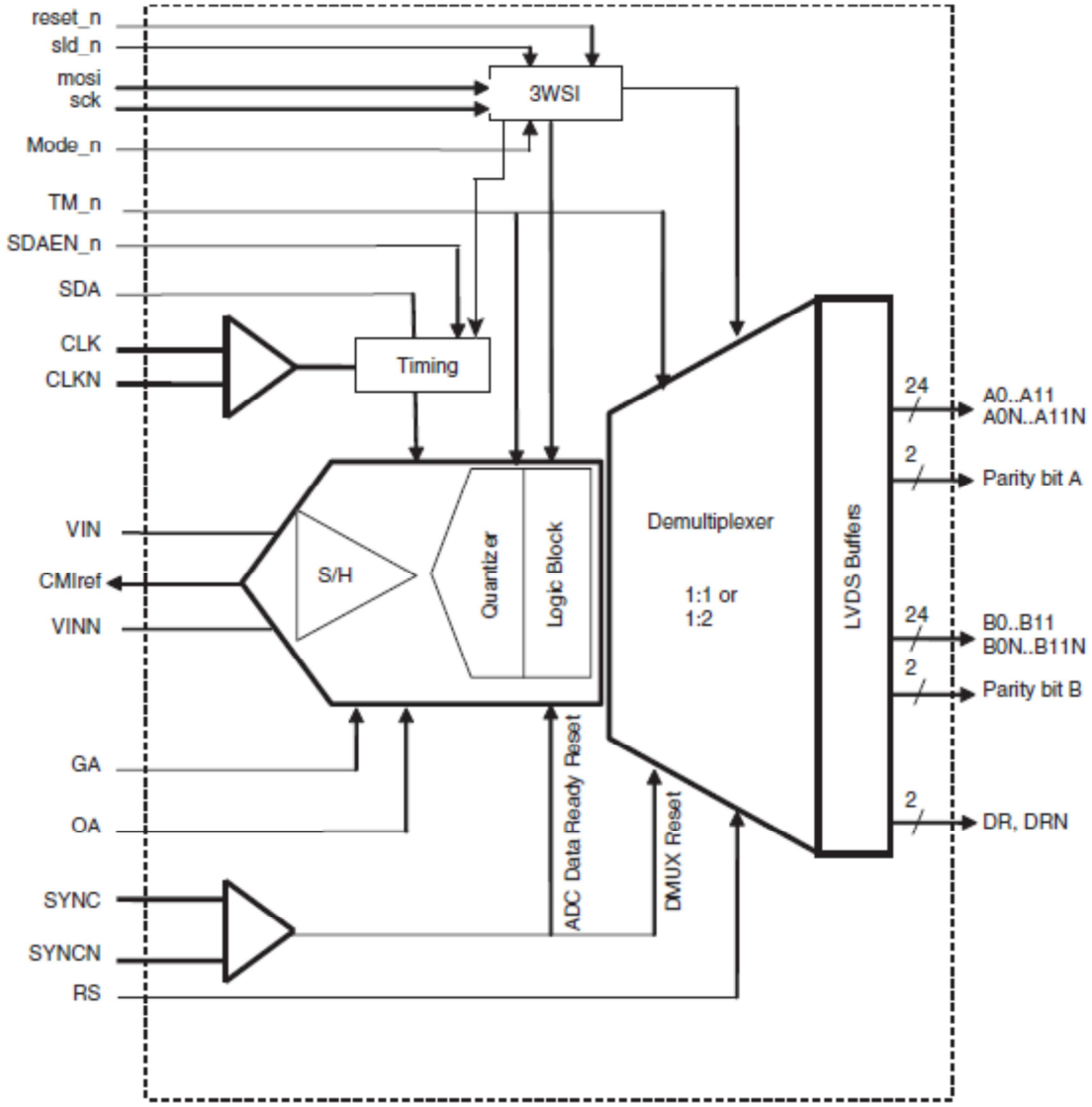
1.2. 12-bit ADC

The EV12AS200A-DK Demo Kit is based on e2v EV12AS200A 1.5 Gsps 12-bit ADC whose block diagram is given on Figure 1.

Figure 1. EV12AS200A 12-bit ADC Block diagram



The EV12AS200A is a 12-bit 1.5 GSps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100 Ω differential output buffers. It integrates 3 Wires Serial Interface (3WSI) circuit (write only), which can be activated or deactivated (via Mode signal).

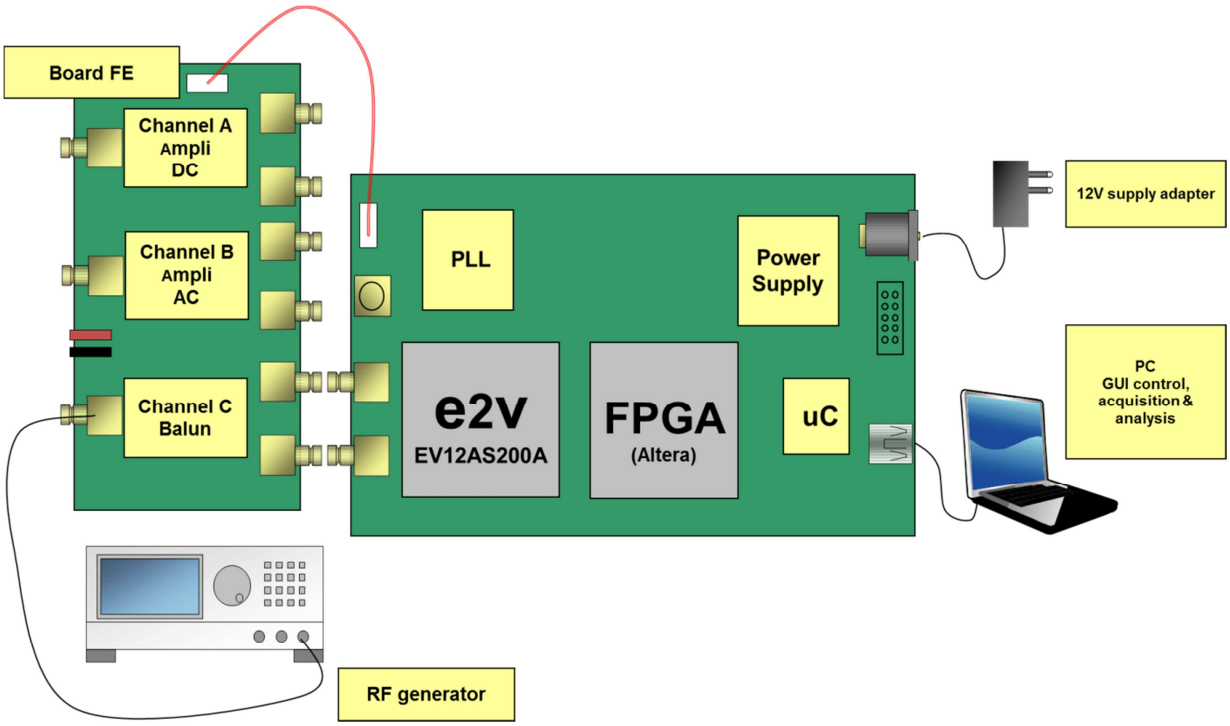
The full datasheet can be found on the e2v website.

http://www.e2v.com/products-and-services/hi-rel-semiconductor-solutions/broadband-data-converters/datasheets/

1.3. Demo Kit

Figure 2 provides an overview of the system architecture.

Figure 2. EV12AS200A-DK Demo Kit system architecture



The complete system is built with the e2v demo kit and an analogue front-end board.

e2v Demo kit contains the following items:

- 12-bit Demo kit with EV12AS200AZPY ADC
- 1 analog front-end board with 3 analog inputs
- Cables & Power Supply
    - Universal 12V power Adapter & Cables
    - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- 2 SMA plugs to connect front-end board on the demo kit board
- CD ROM with GUI Software, FPGA program and documentation

Acquisition and formatting of ADC digital output data are done on the demo kit board.

A USB driver on the ADC Demo kit allows transmission of the data to the computer. Then the computer processes the ADC output data (FFT) and displays the conversion results.

Software and Graphical User Interface are provided with the Demo Kit.

The provided software operates using Labview RunTime (no license required).

Figure 3. Analog front end board

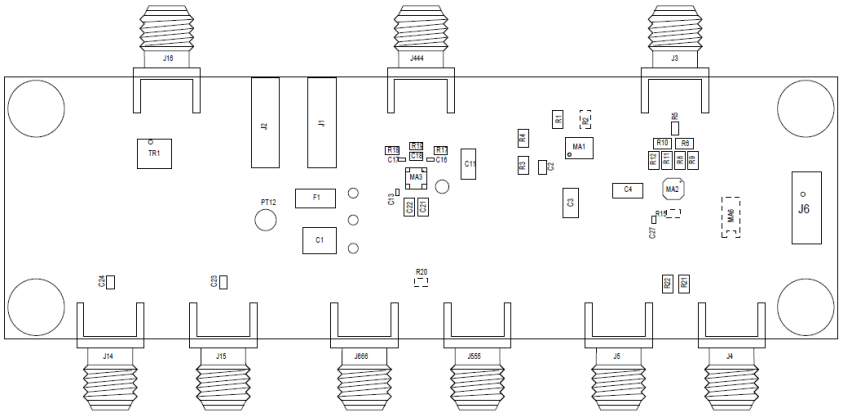


Figure 4. EV12AS200A-DK Demo Kit

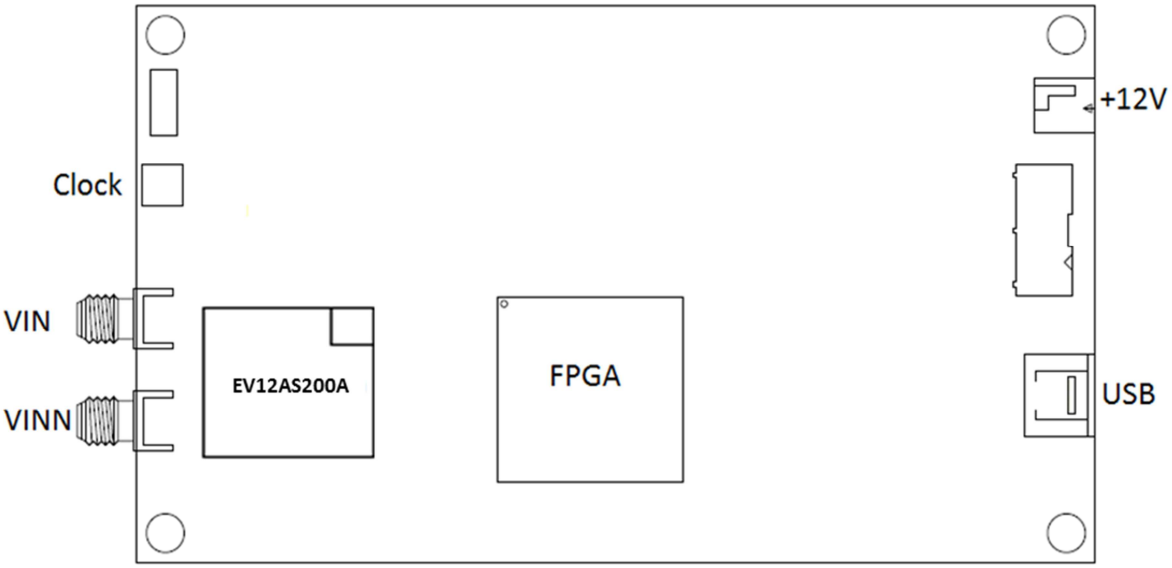
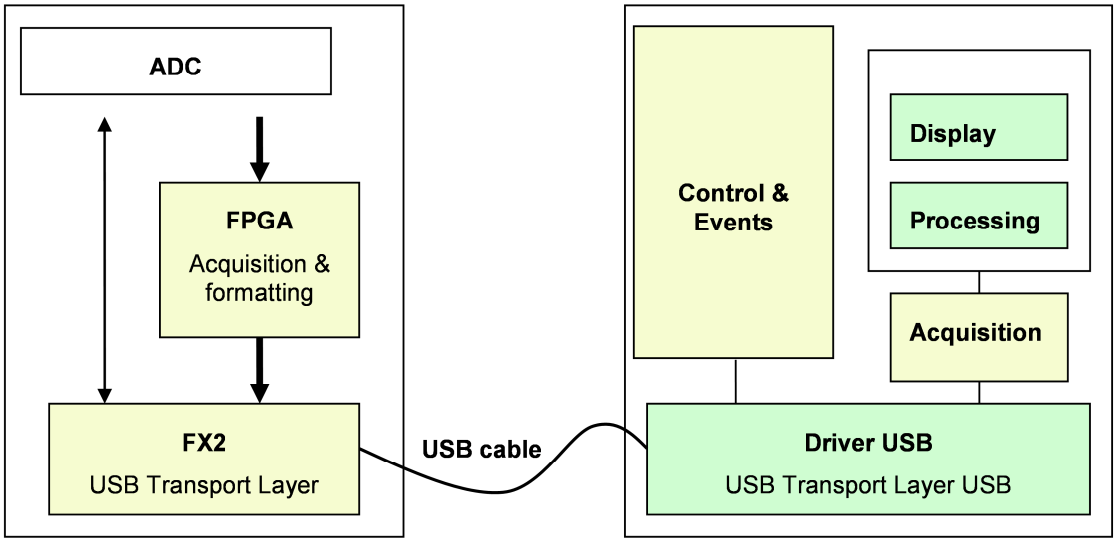


Figure 5. EV12AS200A-DK Demo Kit functional architecture



2 Quick start

2.1. Operating procedure

1. Install the Software as described in section 4 Software Tools.
2. Connect the power supplies EV12AS200A-DK boards.
3. Connect the USB cable.
4. Check if currents are correct (see chap 4.5.5. Power).
5. Connect a RF generator on Analog input.
6. Turn on the RF generator.
7. Launch acquisition (see chap **Erreur ! Source du renvoi introuvable.** Acquisition).

Note 1: Depending on the purity of the signal generator a band-pass filter may be required between the generator and the demo system

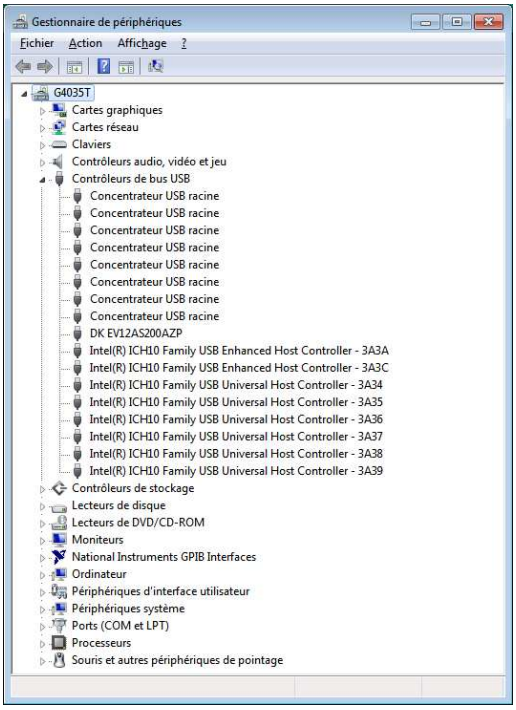
Note 2: Ensure that the absolute maximum rating for the analog input of the device is not exceeded.

2.2. Troubleshooting

2.2.1. Installation

- Check that you own rights to write in the directory (administrator rights).
- Check for the available disk space.
- Check that the USB port is free and properly configured.
    - DK 12 connected to USB 2 driver

Figure 6. USB port driver configuration

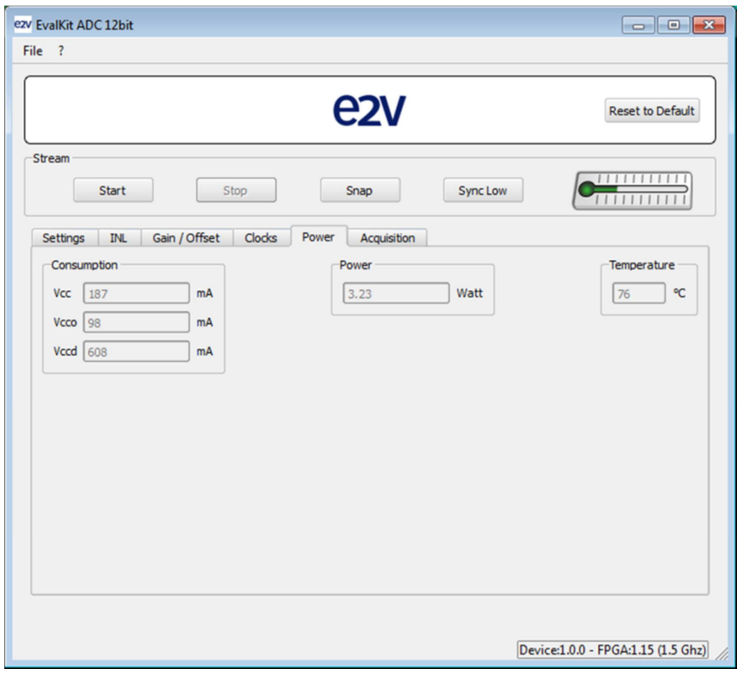


Warning: this installation is done for one USB connector only. If USB connector is changed, USB driver need to be re-installed before use.

2.2.2. Start-up procedure

- Check that supplies are properly powered on and properly connected.
- Check if USB connector is properly plugged.
- Check on the power section that the current consumption is OK (within the specification of the ADC) ,that the junction temperature of the ADC is lower than 90℃ and that heat sink is properly connected.

Figure 7. Junction temperature and consumption monitoring with GUI



2.3. External equipment

The 12-bit Demo Kit needs very little external hardware.

- RF generator for Analog input signal
  - The 12-bit ADC can convert analog signals up to 2.3GHz
  - For optimum performance this generator must have a low phase noise

  Please see Figure 8 for example of signal generator.
- Cables & Power Supply (provided with the demo kit)
  - Universal 12V power Adapter & Cables
  - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- PC with Windows
  - Windows® 2000/98/XP and Windows® NT and Windows 7 (note 32bit only)

  Please see chap 4.1 Overview.

Optional:

- RF generator for clock input signal.
  - The 12-bit Demo Kit provides clock signal at 1.5 GHz using its on-board PLL
  - The 12-bit Demo Kit could be tested with other clock frequency

  Please see chap 6.1 Clock selection.

Figure 8. Example of RF generator

Signal generator
Agilent E4426B 250KHz 4GHz (High spectral purity)
SMA100A 9 KHz 6GHz (High spectral purity)

3 Main functions

3.1. Analog input signal

The user only needs to provide an analog signal at the input of the ADC.

- Directly on EV12AS200A-DK in case of differential signal, or
- Via the analog front end board in case of single ended analog signal

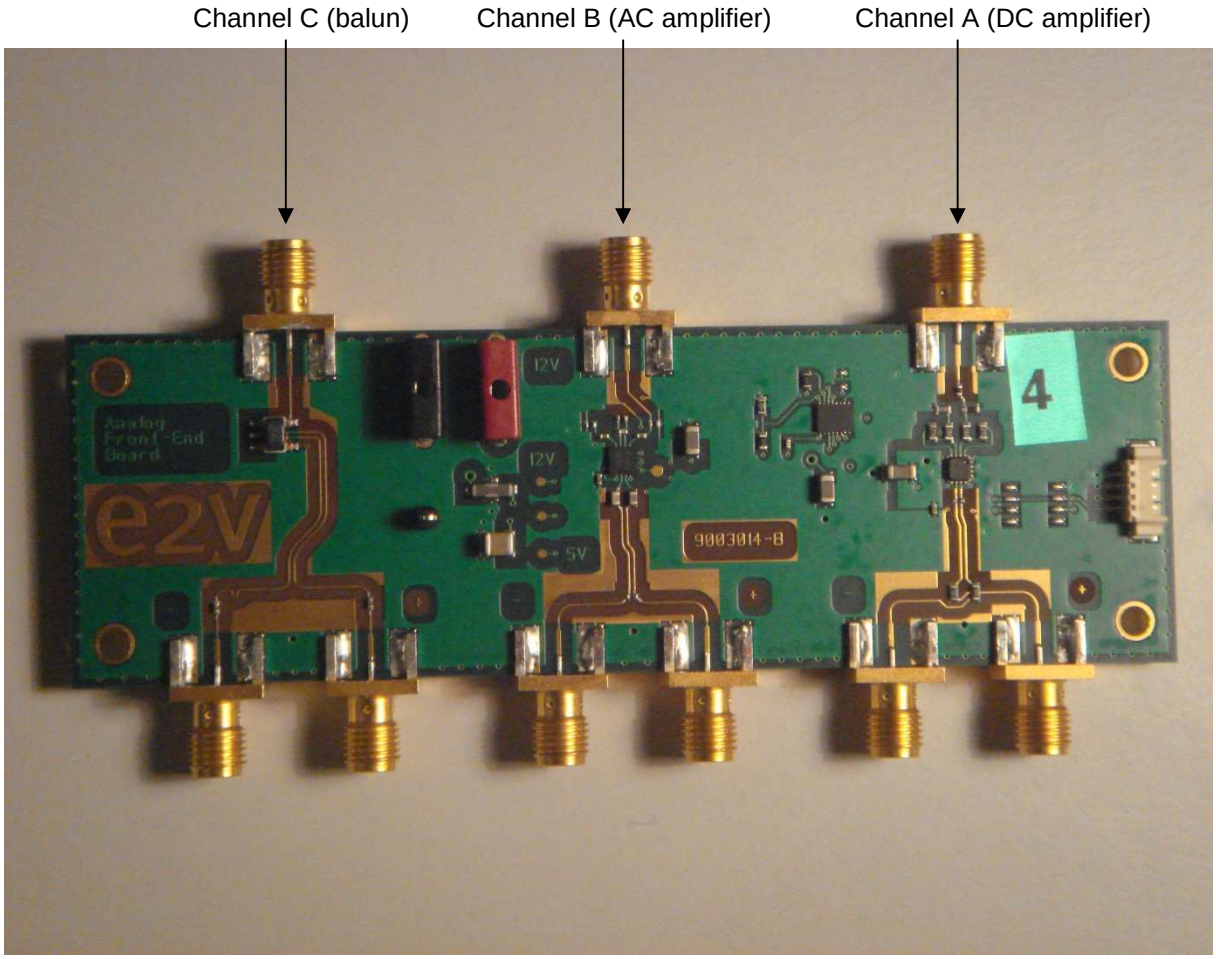
The analog front-end board offers three ways to inject analog signal on the EV12AS200A-DK board:

- Channel A : Single to differential input via DC amplifier (ADA4927-1YCP)
- Channel B : Single to differential input via AC amplifier (ADA4960-1)
- Channel C : Single to differential input via RB balun transformer (ETC1-1-13/MABA-007159)(MABA-010125-TC1113/MABA-010125-TC1113)

Note1: *In order to use amplifier inputs, it is mandatory that the impedance of the single ended is 50Ω*

Note2: *due to an instability in the common mode output the DC input is not recommended.*

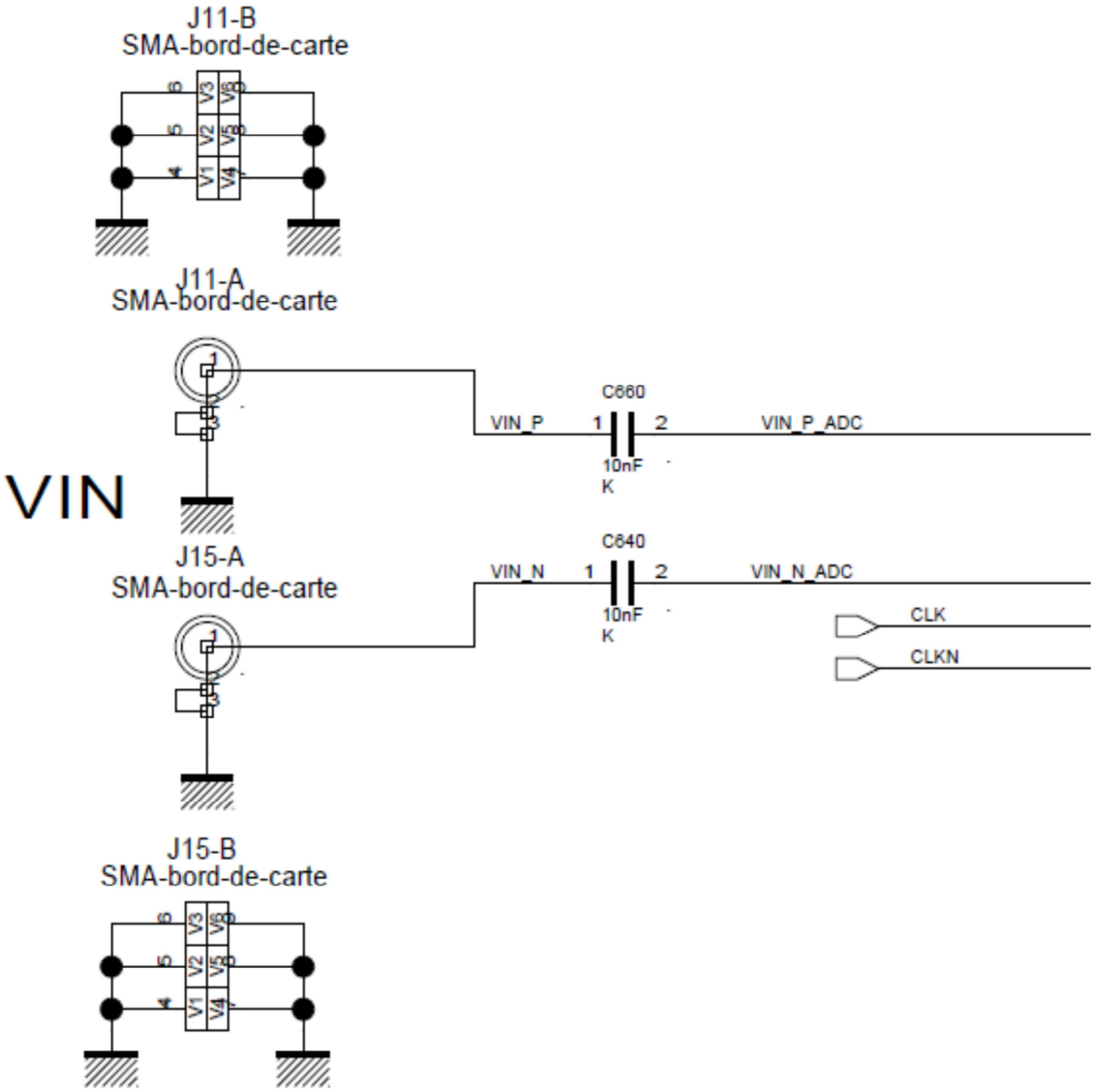
Figure 9. Analog front end-board



3.1.1. Differential input of the EV12AS200A-DK

The differential analog input of the EV12AS200A is connected on the SMA connectors of the EV12AS200A-DK board via two 10nF capa on Vin_N and Vin_P.

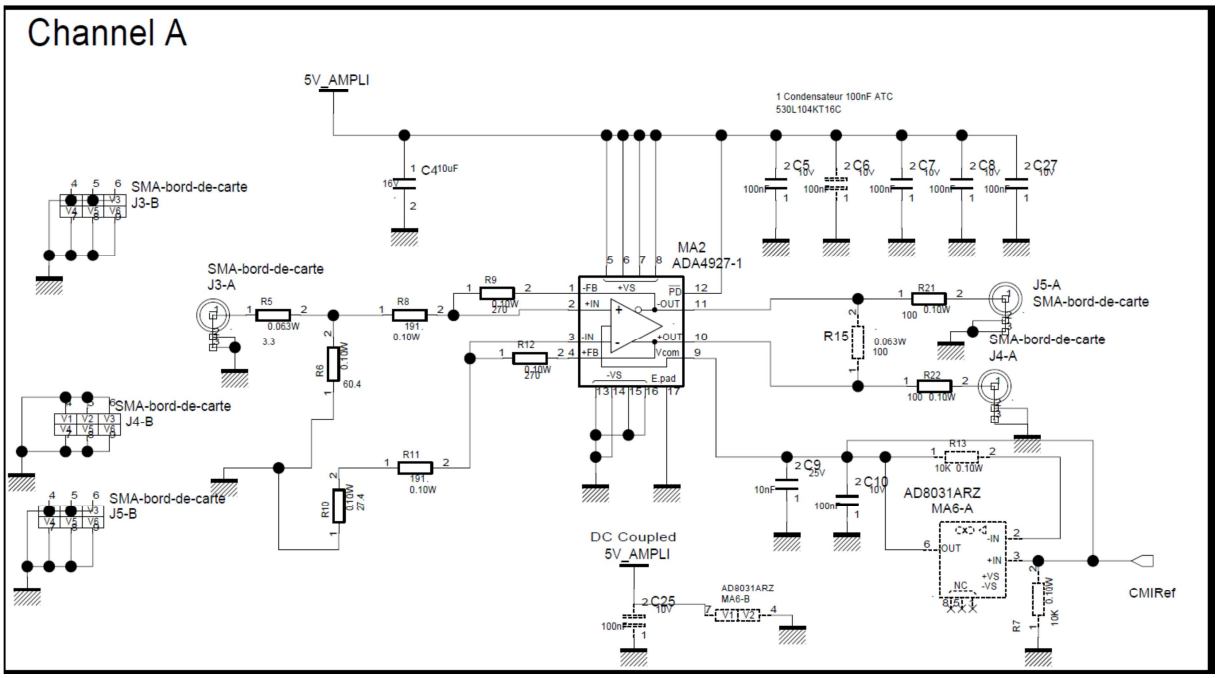
Figure 10. VIN : EV12AS200A analog input schematics (folio 5/11)



3.1.2. Analog input Channel A

The Analog input channel A uses a DC differential amplifier (ADC driver) from Analog Devices ref: ADA4927-1YCP.

Figure 11. Channel A : ADA 4927-1 schematic



The ADA4927-1 is used in DC configuration with output common mode driven by ADC 12-bit.

The input is biased at 2.5V since this is a requirement for best performance from the amplifier, this should be taken into account when using this input.

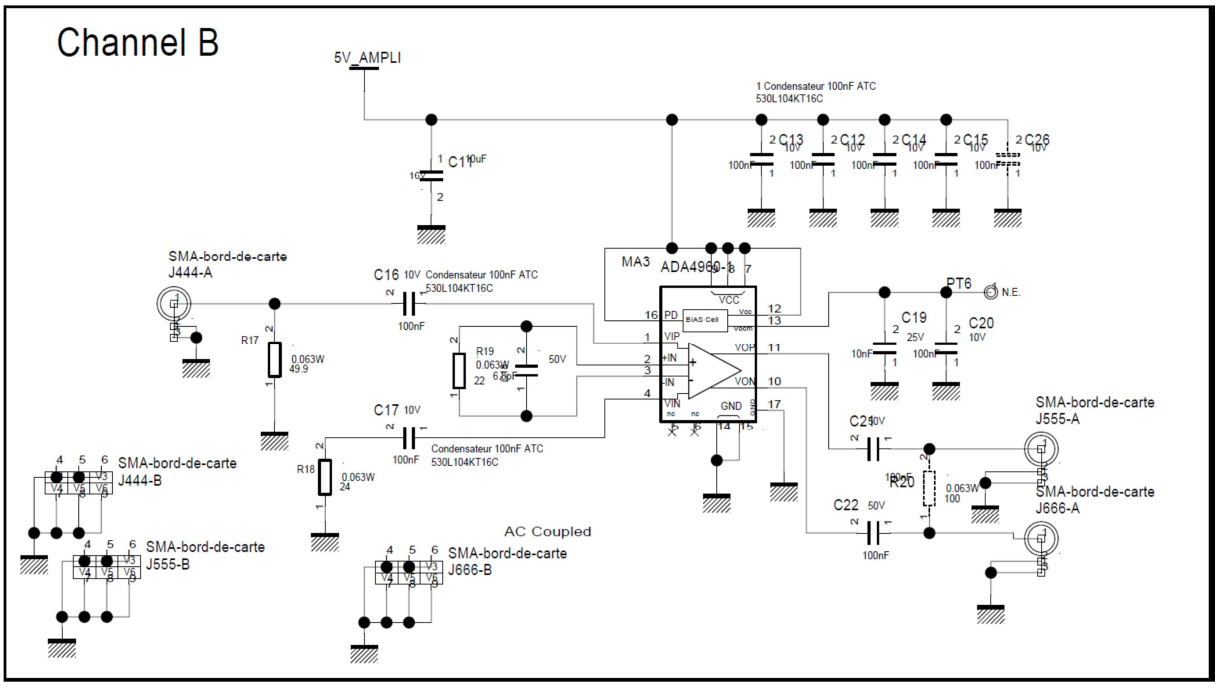
Note1: In order to have a correct biasing of the input of the amplifier, it is mandatory that the impedance of the single ended is 50Ω.

Note2: Be careful that if a DC voltage is added after the RF generator output that this will not damage the generator.,

3.1.3. Analog input Channel B

The Analog input channel B uses an AC differential amplifier (ADC driver) from Analog Devices ref: ADA4960-1.

Figure 12. Channel B : ADA4960-1 schematic



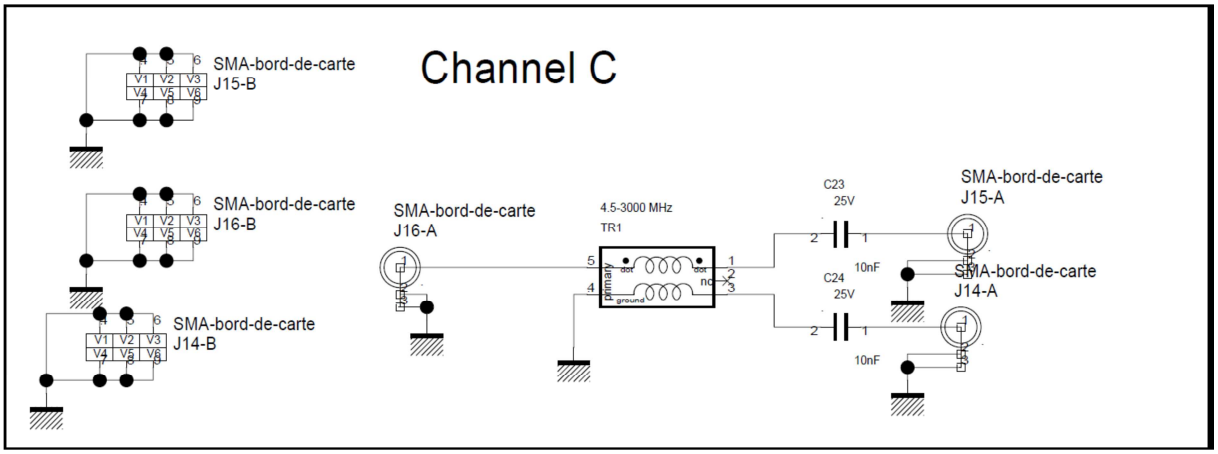
The ADA4927-1 is used in AC configuration.

Note1: Be careful that if a DC voltage is added after the RF generator output that this will not damage the generator.

3.1.4. Analog input Channel C

The Analog input channel C uses an RF Transformer from MACOM ref: ETC1-1-13 / MABA-007159

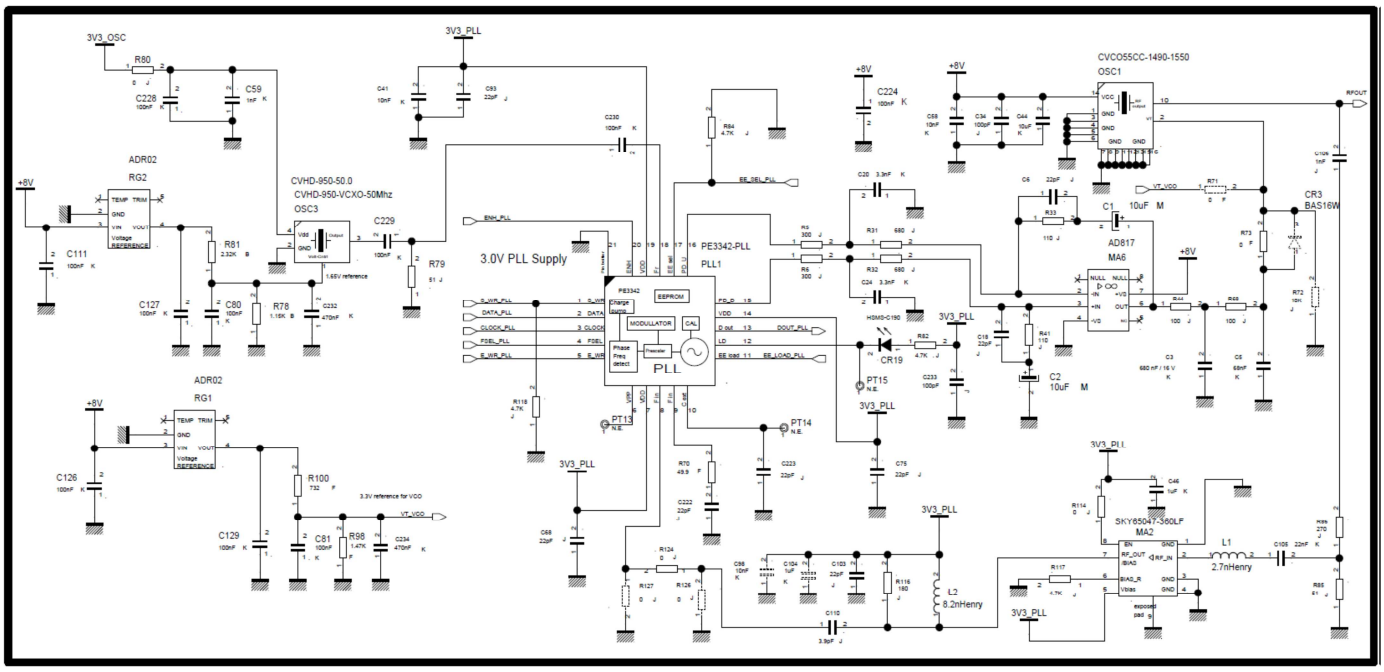
Figure 13. Channel C : ETC1-1-13 / MABA-007159 schematic



3.2. ADC clock input signal

ADC clock input is generated by Peregrine PE3342-PLL PLL associated with the CVC055CC-1490-1550 VCO at 1.5 GHz. This frequency is fixed.

Figure 14. ADC clock input : schematic



Note 1: By default, the on-board PLL clock is selected but an external clock input (provided by a RF generator) is allowed.

Note 2: The clock signal is fed to the board via an SMA connector followed by Single to Differential Balun RF transformer (MABA-010247-2R1250).

Note 3: For operation at different clock frequencies it is probable that the FPGA interface will need to be re-compiled using different timing constraints.

Please see chap 6.1 Clock selection.

3.3. Control of ADC settings

The Graphical User Interface allows for complete monitoring and control of all the settings of EV12AS200A 12-bit ADC such as channel selection, Gain, Offset.

Please see chap 4.5. Operating Modes.

Please refer to datasheet EV12AS200A for more information.

http://www.e2v.com/products-and-services/hi-rel-semiconductor-solutions/broadband-data-converters/datasheets/

By default the SPI signal is controlled by FX2 microcontroller but it could be driven by the FPGA.

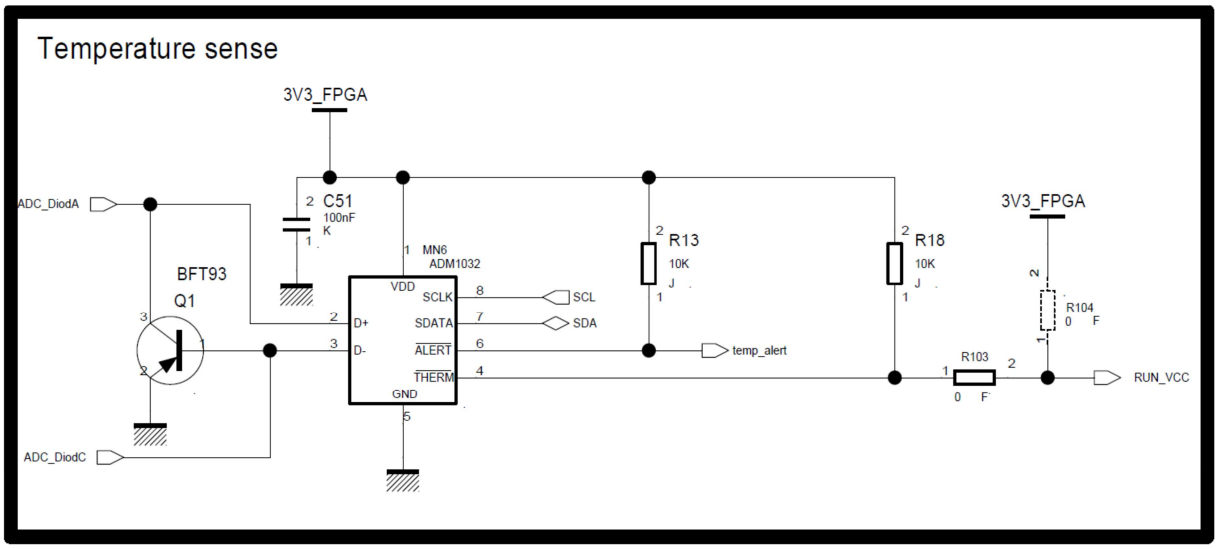
Please refer to chap **Erreur ! Source du renvoi introuvable.**. SPI signal for more information.

3.4. ADC junction temperature monitoring

ADC junction temperature can be monitored by a temperature sensor from ON Semiconductors Ref: ADM1032

http://www.onsemi.com/PowerSolutions/product.do?id=ADM1032

Figure 15. Temperature sense: schematic (folio 3/11)



ADC junction temperature can be displayed on the PC via the GUI with a resolution of ±1℃.

Please see 4.5.5. Power.

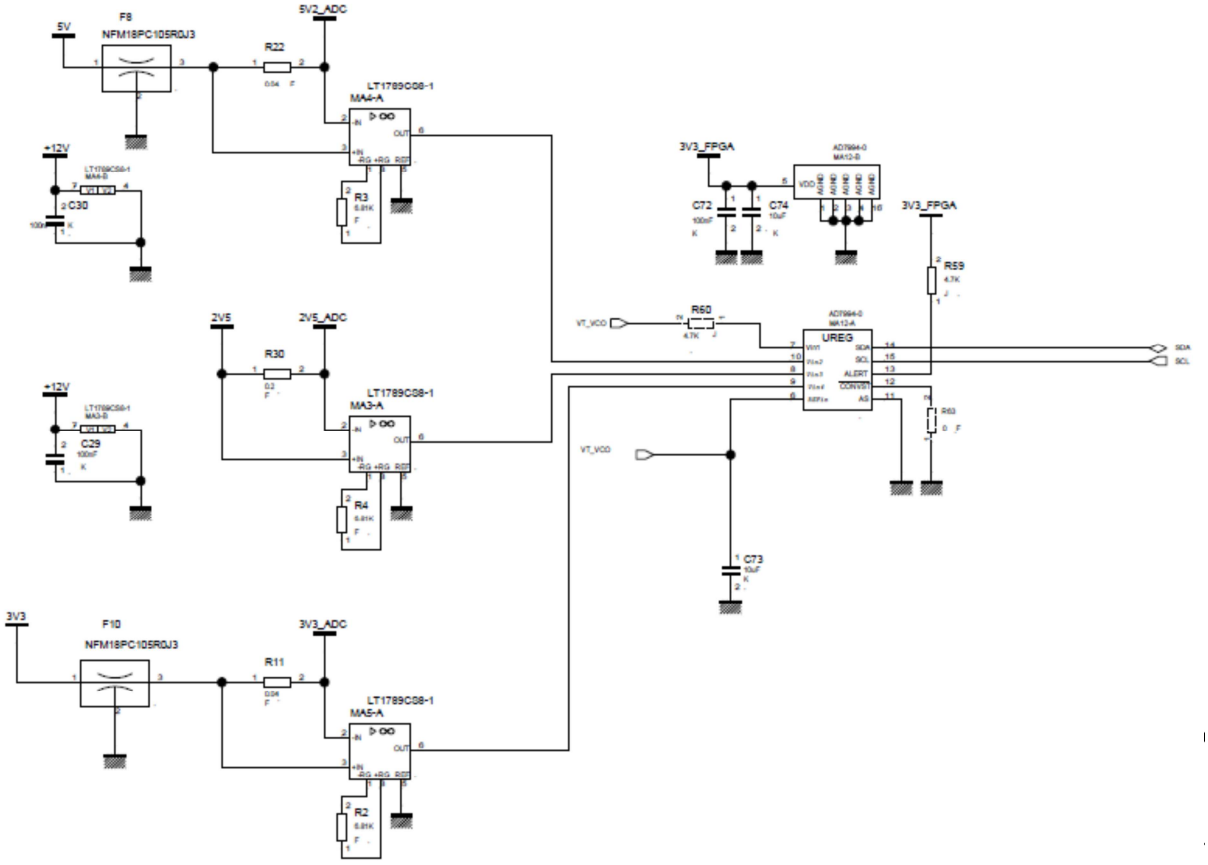
In case of excessive junction temperature, the ADC power supply will be turned OFF and a message will notify the user via the GUI.

The Demo Kit is provided with an external heat sink with internal fan.

3.5. ADC current consumption monitoring

The ADC currents (I_{CC5}, I_{CC3} and I_{CCO}) can be measured by the Demo Kit

Figure 16. ADC current measurement schematic



ADC currents (I_{CC5}, I_{CC3} and I_{CCO}) can also be monitored via the GUI.

Please see chap 4.5.5. Power.

3.6. ADC SYNC signal

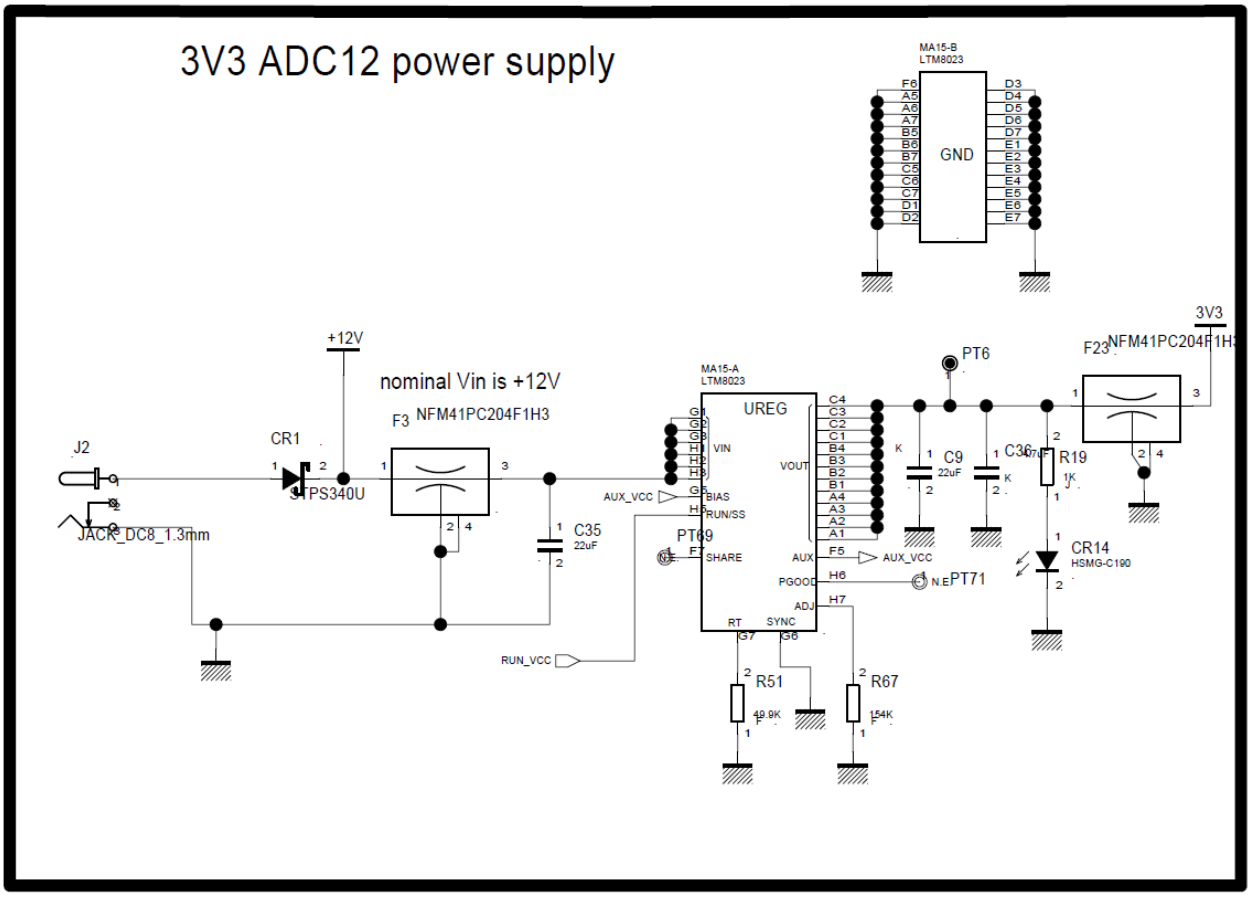
It is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented. Nevertheless, the SYNC is available in case it is necessary to reset the ADC during operation. The SYNC signal is directly driven by the FPGA.

3.7. Power Supply

The power supply for the 12-bit Demo Kit is provided by DC/DC block from Linear Technologies.

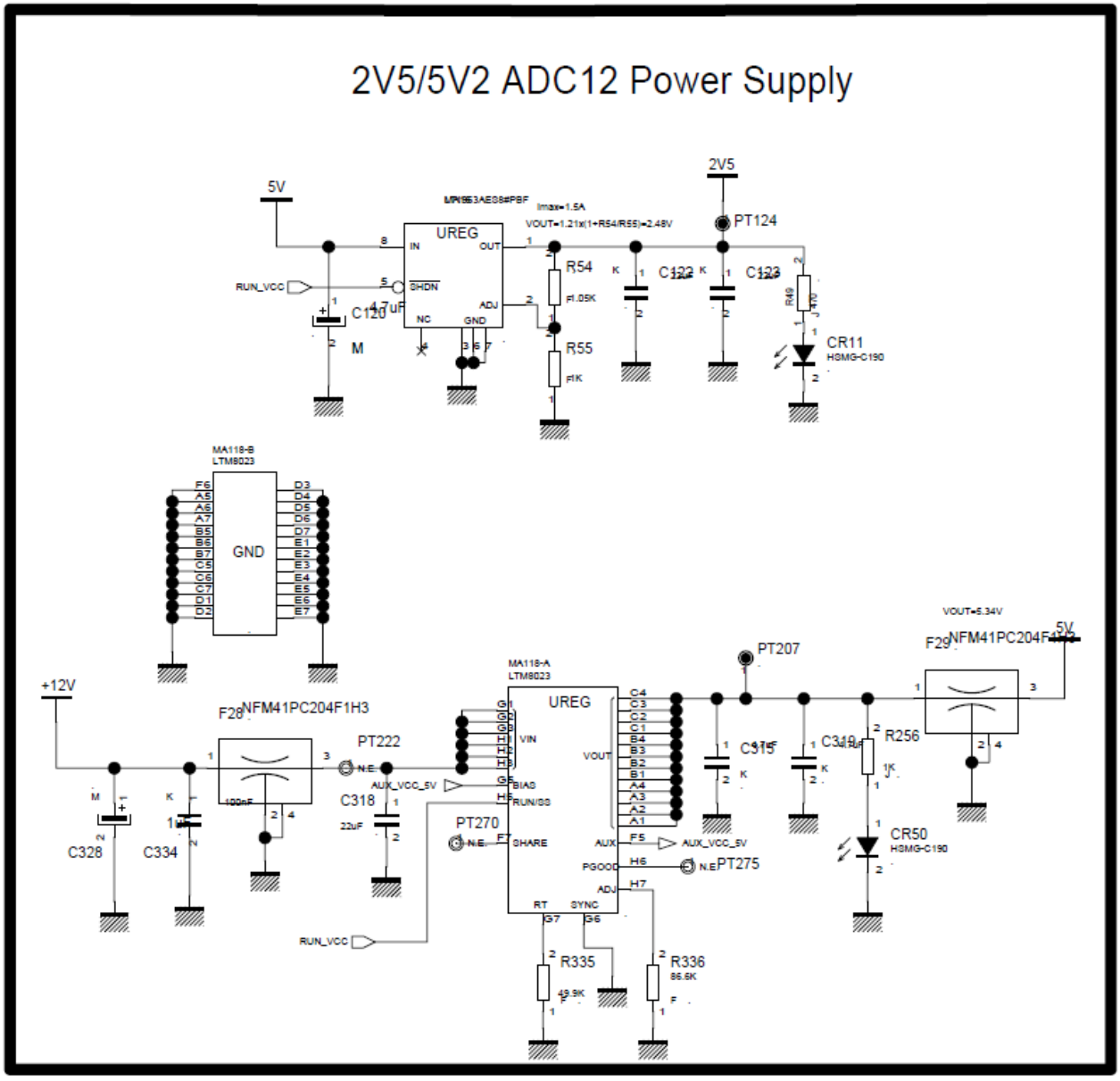
- Vcc3 (3V3) power supply with micro module LTM8023
- http://www.linear.com/product/LTM8023

Figure 17. Vcc3 (3V3) power supply



- Vcc5 (5V) and Vcco (2V5) power supply with micro module LT1963AES8
- http://www.linear.com/product/LT1963A

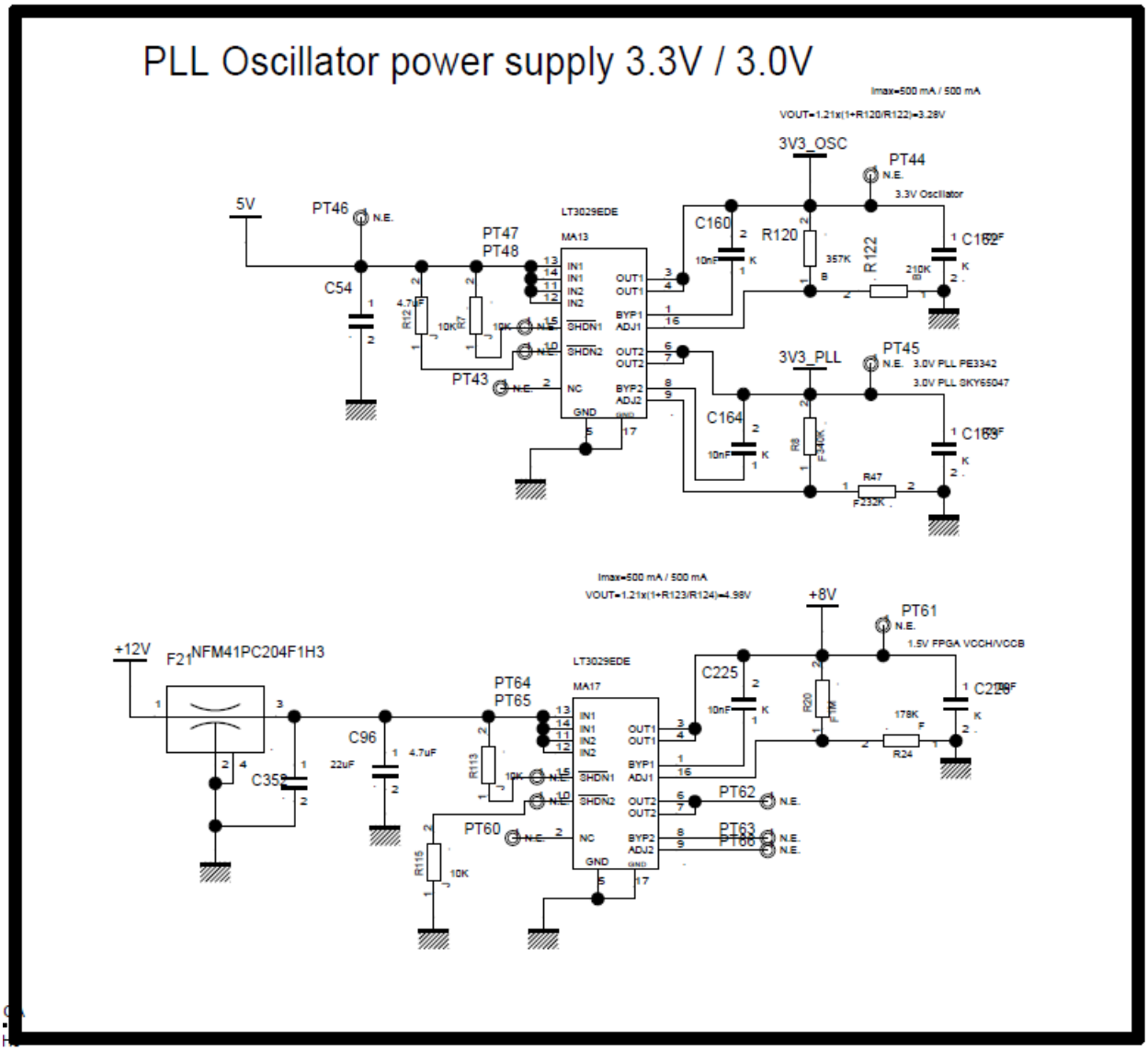
Figure 18. Vcc5 (5V) and Vcco (2V5) power supplies



The amplifier and PLL power supplies use low noise LDO regulators from Linear Technology.

- Oscillator (3V3) and PLL (3V3) power supply with micro module LT3029EDE
- VCO (8V) power supply with micro module LT3029EDE
- http://www.linear.com/product/LT3029

Figure 19. PLL and Oscillator power supply



4 Software

4.1. Overview

The Demo Kit board uses three different kinds of firmware / software:

- FPGA firmware

  e2v provides the FPGA program to be used with EV12AS200A-DK Demo Kit.

  The board is supplied with the FPGA already programmed.

  The source code is available on request through hotline-bdc@e2v.com.

- User Interface software

  The User Interface software is a Visual C++® compiled graphical interface that does not require a licence to run on a Windows® NT® or Windows® 2000/98/XP® PC and windows7 (32 bit)

  The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

- FX2 microprocessor

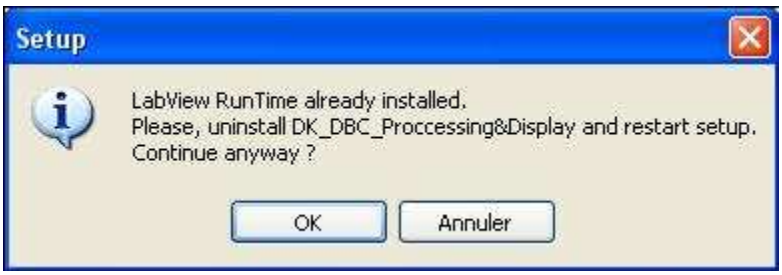
  This processor is the interface between the User Interface software and the FPGA.

  It is supplied already programmed.

Warning: For the software installation, administrative rights are needed.

Warning: If the software is already installed a window appears.

Figure 20. Error message if Labview software is already installed



This applies when a previous version of software is present or another e2v demo is present. When updating an installation it is recommended to uninstall the existing version (but not DK_DBC_Processing&Display).

If any other e2v demo kit software is installed this can be left in place.

Click on OK and continue.

4.2. Configuration

The advised configuration for Windows® 2000/98/XP and Windows® NT is:

- PC with Intel® Pentium® Microprocessor of over 100 MHz
- Memory of at least 24 Mo

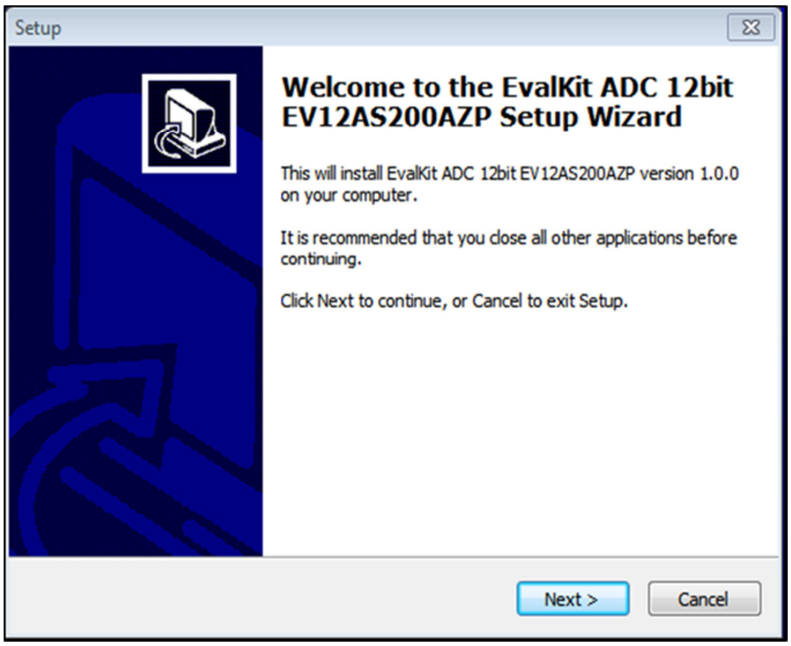
For other versions of Windows® OS, use the recommended configuration from Microsoft.

4.3. User Interface installation

Install the 12-bit Demo Kit application on your computer by launching the Setup_EvalKit_EV12AS200AZP_v1_0_0.exe installer (please refer to the latest version available).

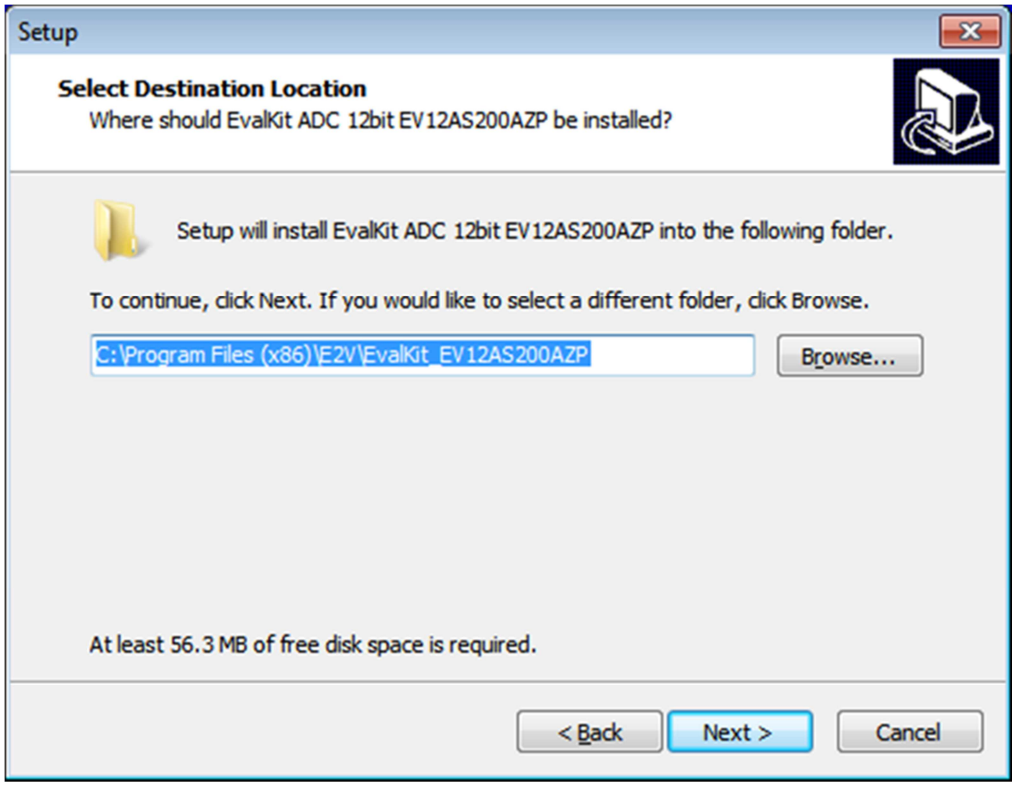
The screen shown in Figure 21 is displayed:

Figure 21. 12-bit Demo Kit application «Setup wizard» window



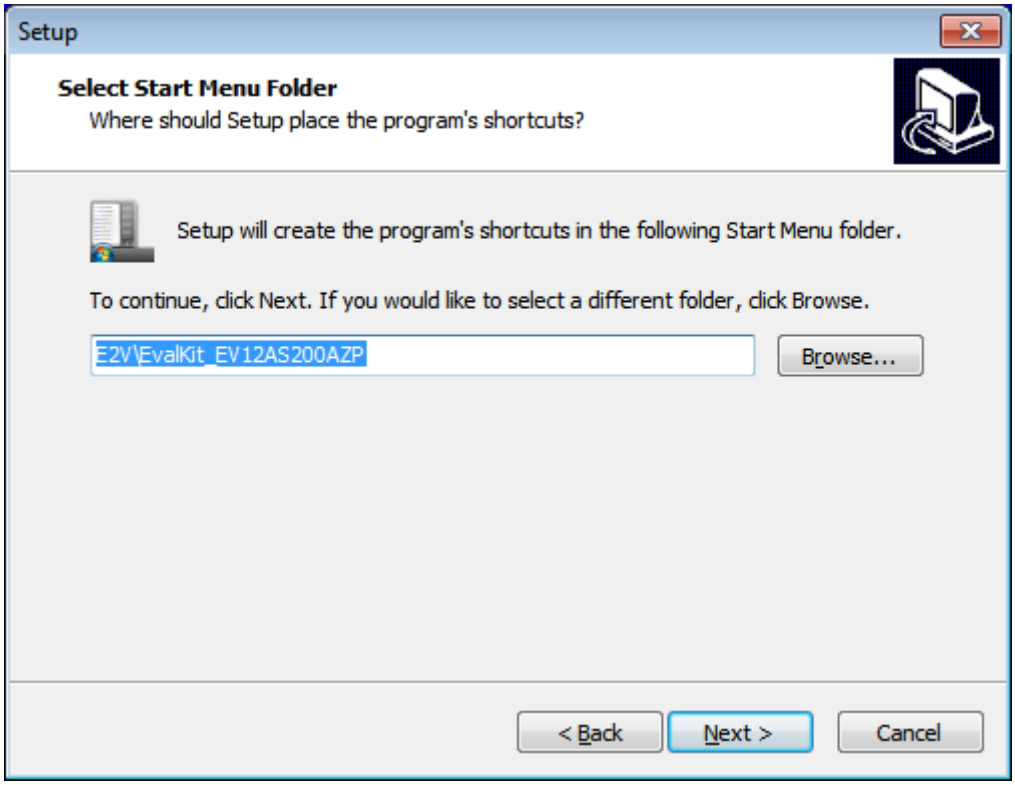
Select Destination Directory

Figure 22. 12-bit Demo Kit application «Select Destination Directory»



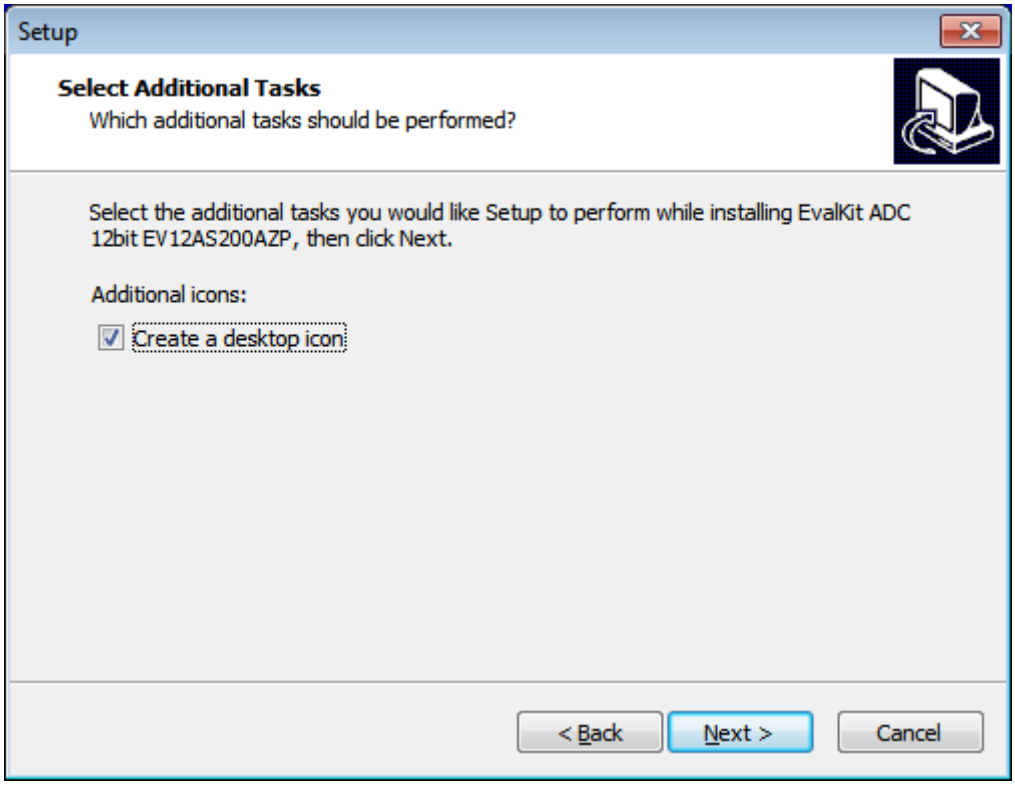
Select Components (Start Menu Folder)

Figure 23. 12-bit Demo Kit application «Start Menu Folder»



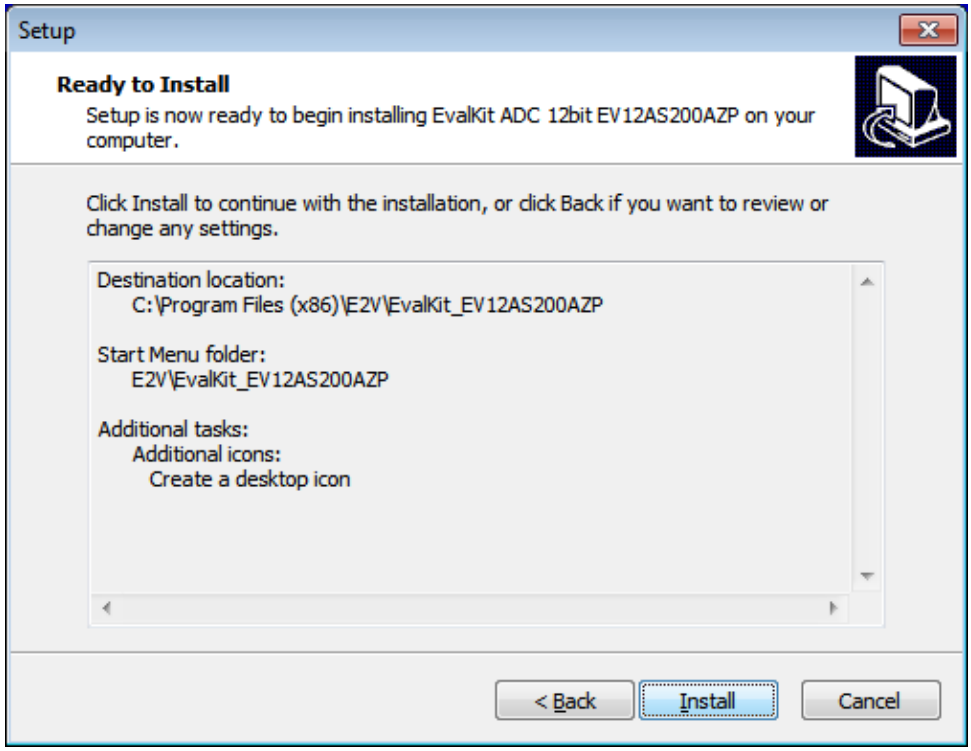
Select Components (Additional Tasks)

Figure 24. 12-bit Demo Kit application «Additional Tasks»



Select Components (Ready to Install)

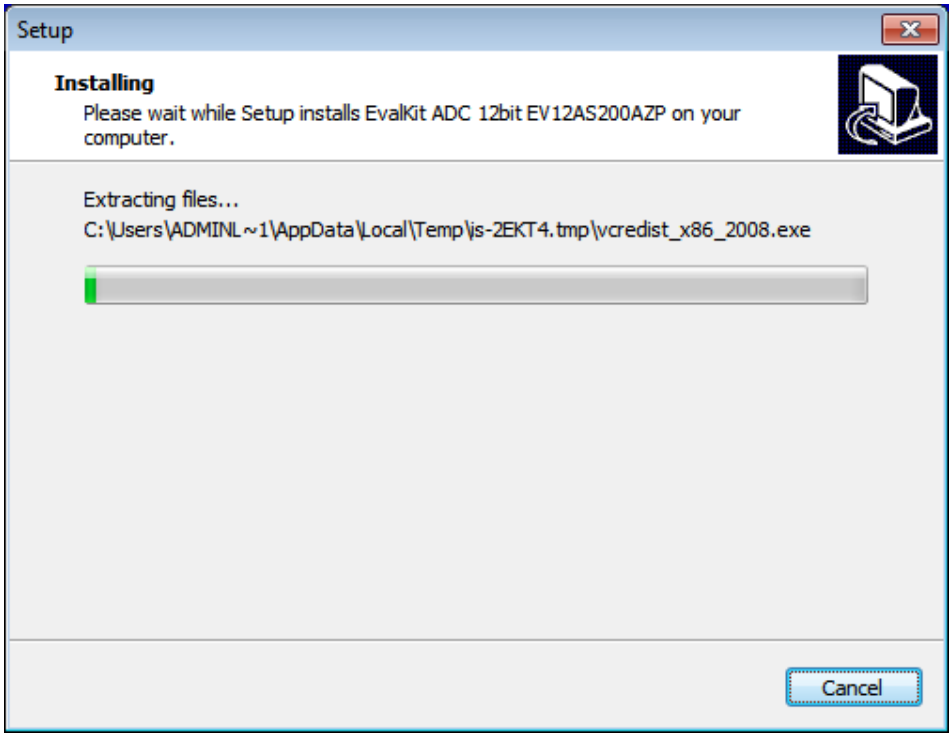
Figure 25. 12-bit Demo Kit application «Ready to Install»

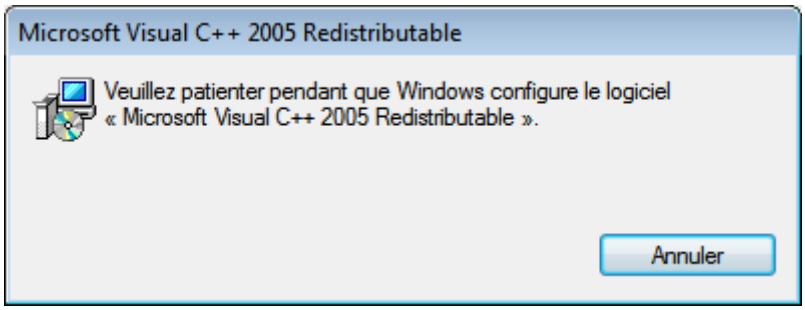


If you agree with the install configuration, press Install button.

The installation proceed

Figure 26. 12-bit Demo Kit installation





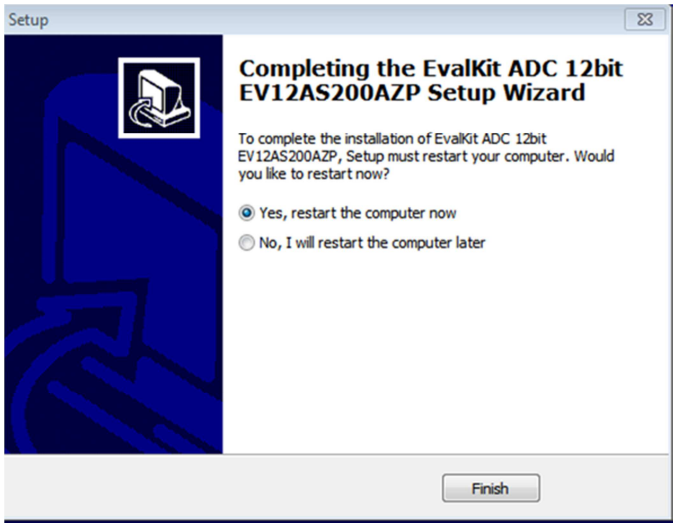
Now a new process of installation started processing and display to install Labview RunTime (no license required).

Please follow instructions.

Figure 27. Labview installation

After that, the installation is completed

Figure 28. 12-bit Demo Kit installation Finished



4.4. USB driver installation

After the installation, 12-bit Demo Kit can be powered up and connected to PC with USB cable.

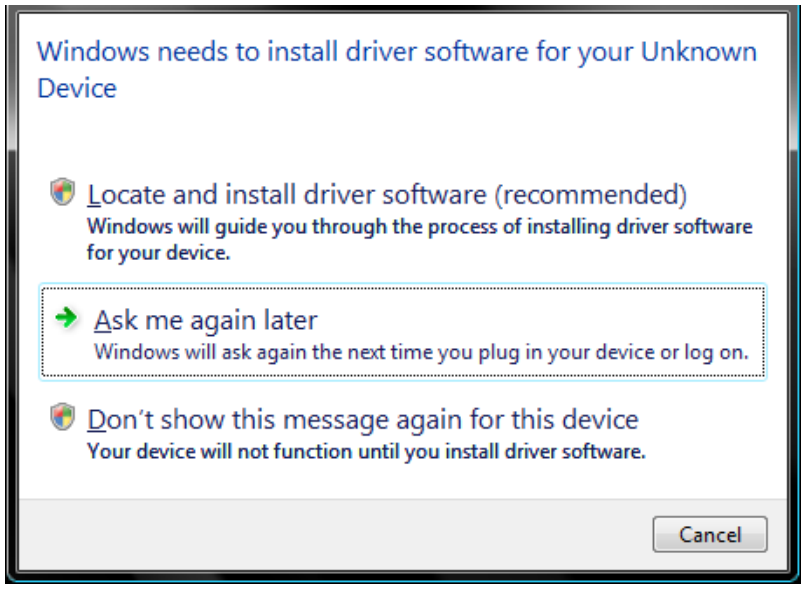
At the first connection a USB driver installation will be launched.

Warning: if the Demo Kit is connected to another USB port on the computer. This installation must be re-started.

The installation is normally fully automatic. If it is not launched automatically, please proceed as described below:

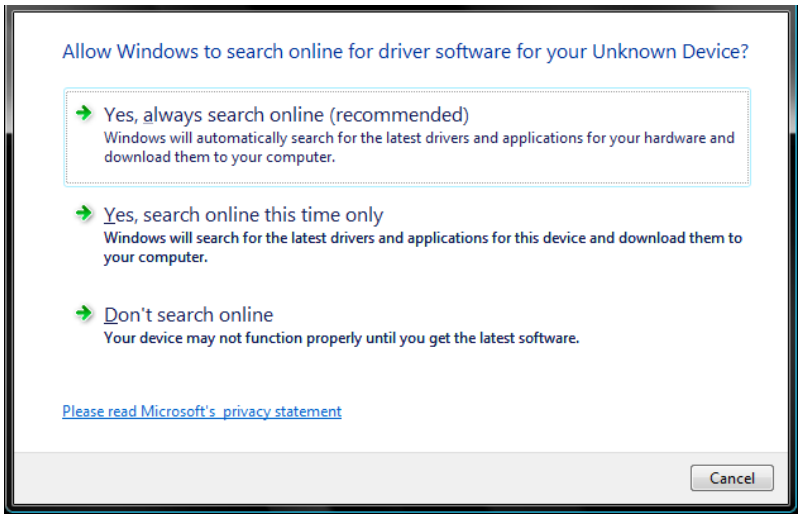
The window shown in Figure 29 will be displayed.

Figure 29. Install driver software



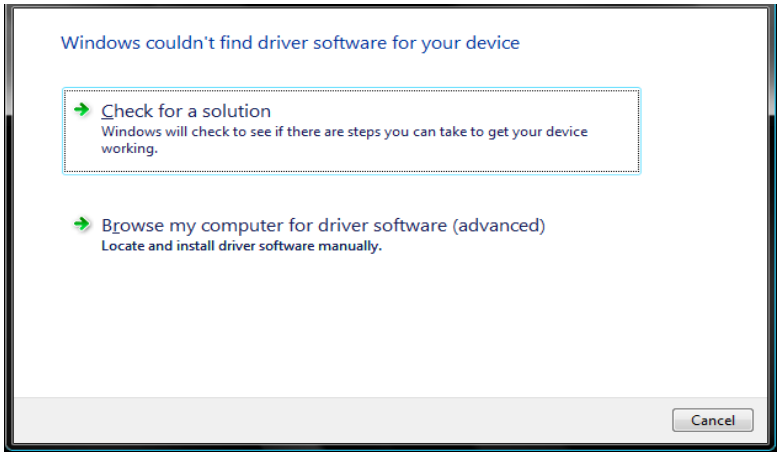
Please choose: Locate and install driver software (recommended)

Figure 30. Allow Windows to search driver



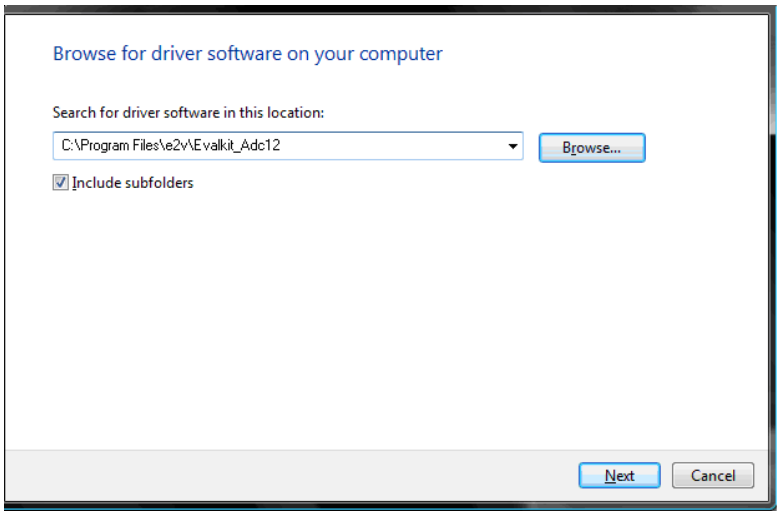
Please choose: Yes, always search online (recommended)

Figure 31. Browse the driver software



Please choose: Browse my computer for driver software (advanced)

Figure 32. Choose the folder



Select C:\Program Files\E2V\Evalkit_Adc12

Figure 33. Warning: installation

Please choose: Install the driver software anyway

A Data transfer has been beginning please wait…

Figure 34. END of new Driver installation

The new driver has been installed

4.5. Operating Modes User Interface

The 12-bit ADC software included with the Demo Kit provides a Graphical User Interface to configure the ADC.

Push buttons, popup menus and capture windows allows easy operation of the system using the different tabs, below:

1. Settings
2. INL
3. Gain / Offset
4. Clock
5. Power
6. Acquisition

The «Reset to Default» button allows re-configuring ADC to the Default Mode. All the windows are reset.

With Clock and Acquisition windows, it is necessary to click on «APPLY» button to validate any command.

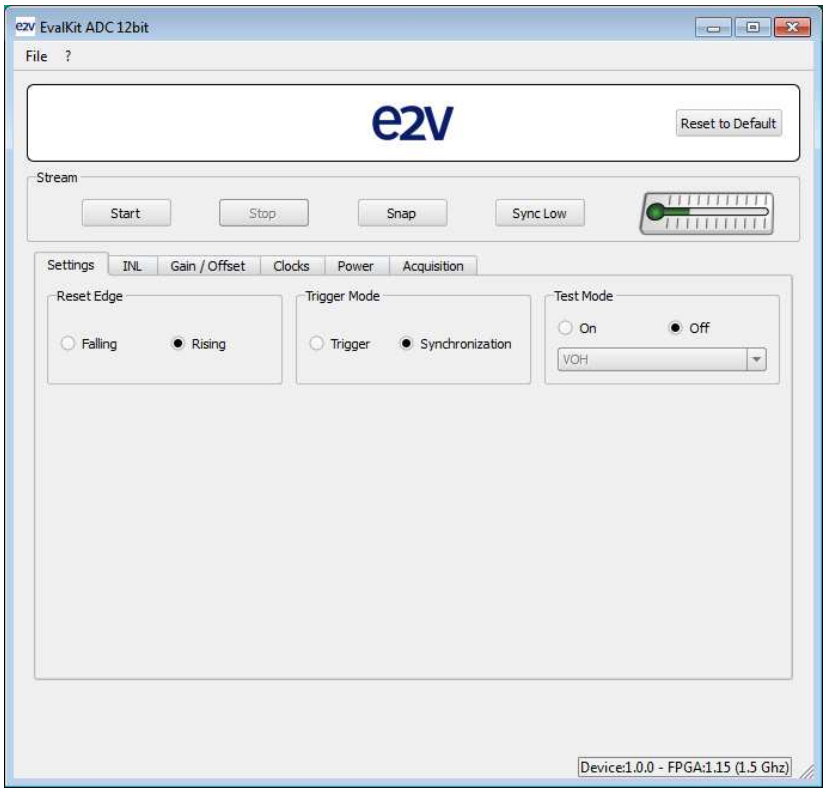
Clicking the «CANCEL» button will restore actual settings.

On the bottom corner the software displays information about software and hardware revision:

- ChipId: revision of 12-bit ADC
- Device: revision of FX2 software
- FPGA: revision of program

4.5.1. Settings

Figure 35. User Interface Demo Kit



In this window, 3 functions are available:

- Standard conversion
- Synchronized conversion
- Test Mode

Standard conversion:

By default the interface is set to process a standard conversion:

The conversion is configured as follow:

- Reset edge: indifferent
- Trigger Mode: Synchronization
- Test Mode: Off

In order to start a conversion, it is necessary to press the «Snap» button. The number of conversions configured in the acquisition sheet is done. Then the conversion results are displayed.

It is also possible to make continuous acquisition by pressing the «Start» button. In this case, as soon as the number of conversions programmed in the acquisition sheet is done, results are displayed and a new acquisition is started. To stop this continuous process, is it necessary to press the «Stop» button. Then, as soon as the on-going acquisition is completed, the results of the latest acquisition are displayed and the ADC stops.

Synchronized conversion:

In order to demonstrate that it is possible to synchronize a conversion with an external event, it is possible to configure the interface in order to emulate an external synchronization event.

To start a synchronized conversion, the interface should be set as follows:

- Reset edge: indifferent
- Trigger Mode: Trigger
- Test Mode: Off

In this case the acquisition will be start as soon as the «Sync» button will toggle according to the reset edge configuration.

Sync button works as follows:

- If «Sync» button is displayed «Sync High», clicking on the button will create a falling edge and the button will be displayed as «Sync Low».

- If «Sync» button is displayed «Sync Low», clicking on the button will create a rising edge and the button will be displayed as «Sync High» again. And so on…

In case the event doesn't happen, a time out error pop-up is displayed.

Figure 36. Timeout warning

Test Mode:

It is possible to test the ADC without any input signal via the test mode.

To start a test conversion, the interface should be set as follows:

- Reset edge: indifferent
- Trigger Mode: indifferent
- Test Mode: On

The test conversion will start according to the Reset edge and the trigger mode configuration.

It is possible to test the lowest code (0) by setting VOL. In this case, the result should be 0 for all samples.

It is possible to test the highest code (4095) by setting VOH. In this case, the conversion result should be 4095 for all samples

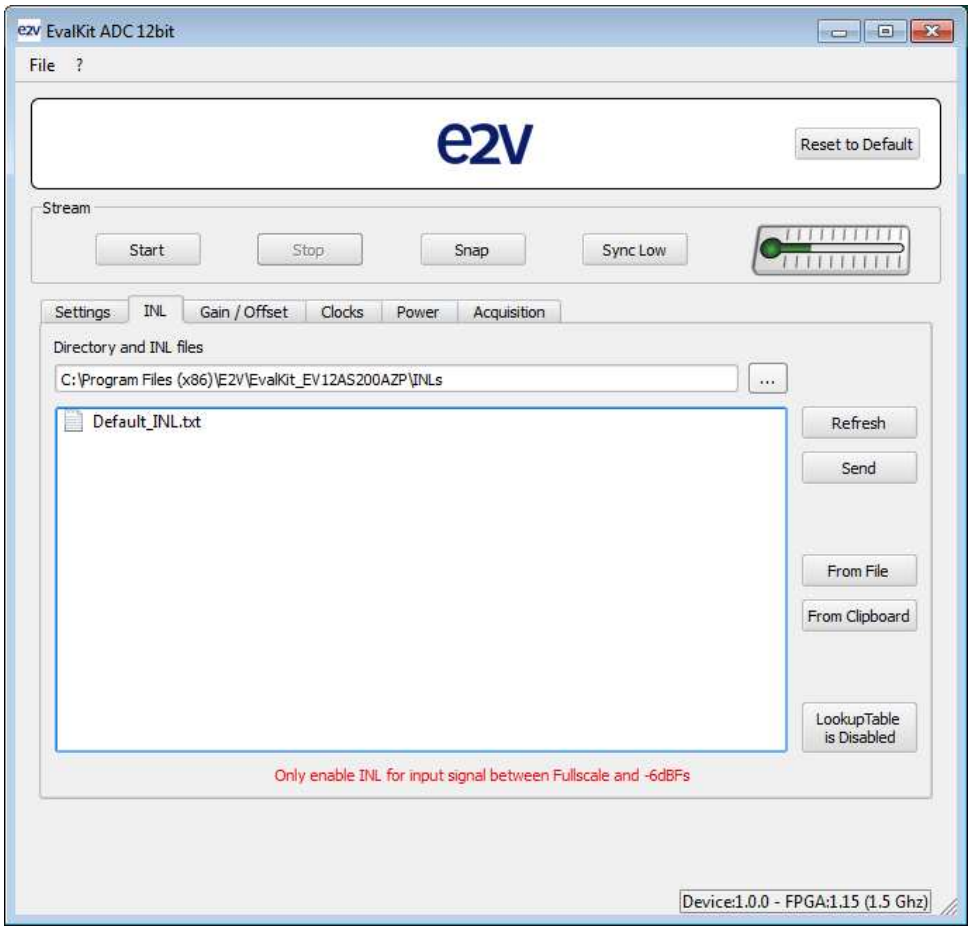
It is possible to use the align pattern by setting Align Pattern. In this case the conversion result should be 8 High, 4 Low, 4 High, 2 Low, 2 High, 2 Low, 2 High, 2 Low, 8 low,… and so on… modulo 32

(see the ADC specification for more information on the test mode).

4.5.2. INL

It is possible to increase the EV12AS200A performance by correcting the INL. The INL correction is done via a look-up table which is loaded on the ADC to adjust the ADC result.

Figure 37. INL



By default there is no INL correction.

In order to make an INL correction, it is necessary to load a lookup table.

- From a file, or
- From the clipboard

There is little part to part INL variation, so it is possible to use the Default_INL.txt INL correction file which is provided with the demo kit.

In this case, use the «send» button.

In case you want to select another INL file from any location you can use the «From file» button and load your own INL file.

If the INL correction values are in your clipboard, you can use the «From Clipboard» button.

In order to use the lookup table you have loaded, the «Lookup Table is Disabled» button should be clicked. This button will then be changed into a «Lookup Table is Enabled» button, and the INL correction will be taken into account on the next acquisition.

In order to disable the INL correction, click again on the «Lookup Table is Enabled» button. This will disable the INL correction and the button will come back as a «Lookup Table is Disabled» button.

In order to create an INL file, it is necessary to start an acquisition with the following configuration:

- Almost full scale signal

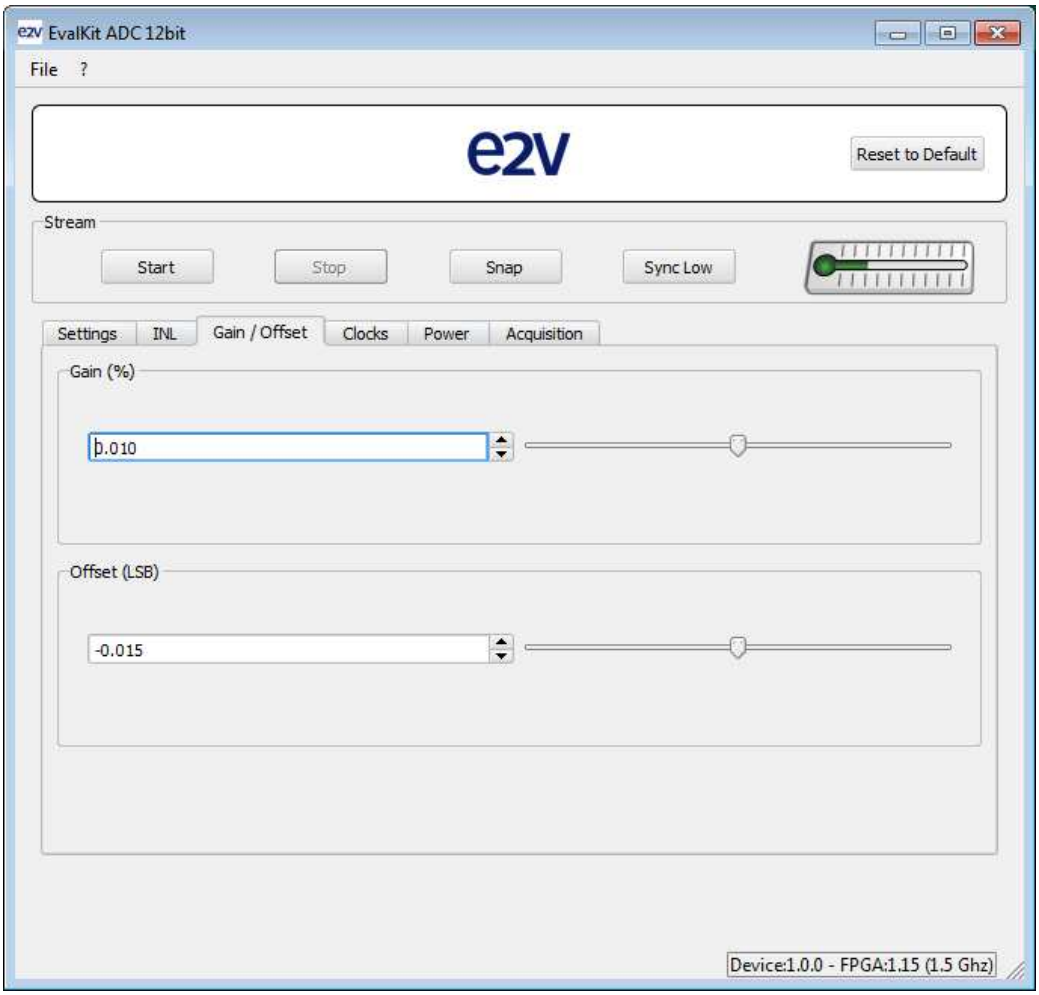
- No INL correction is enabled in the INL window
- INL data saving is activated in the Acquisition window (See chapter 4.6.6. Data Save File)

Then, it is necessary to open the excel file, and to copy the column of INL values into .txt file which will be the INL correction file.

4.5.3. Gain/Offset

It is possible to adjust the gain and the offset of the ADC by sliding the cursor or directly entering an allowed value.

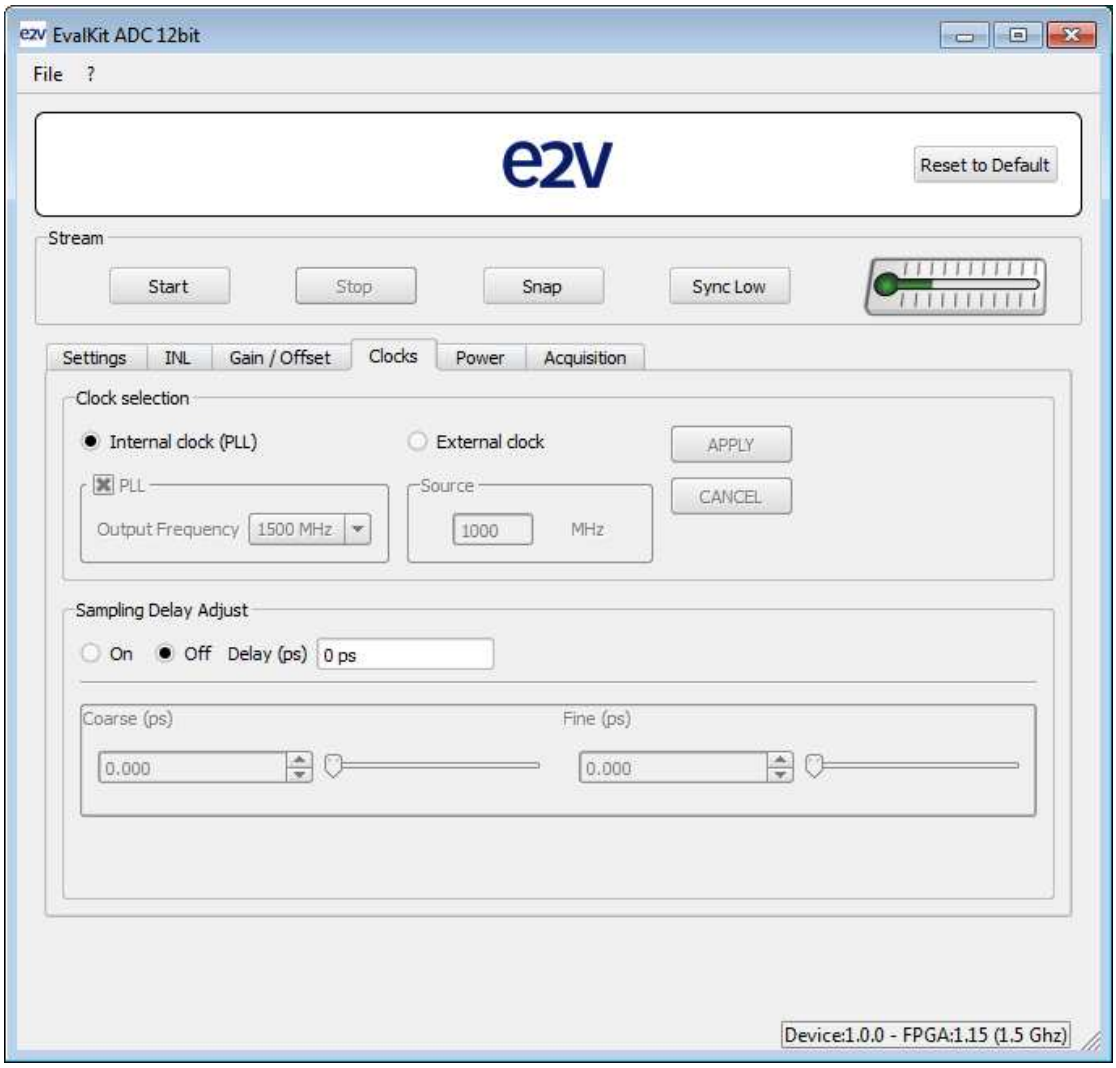
Figure 38. Gain / Offset



4.5.4. CLOCK

It is possible to choose whether to use the internal PLL or an external clock.

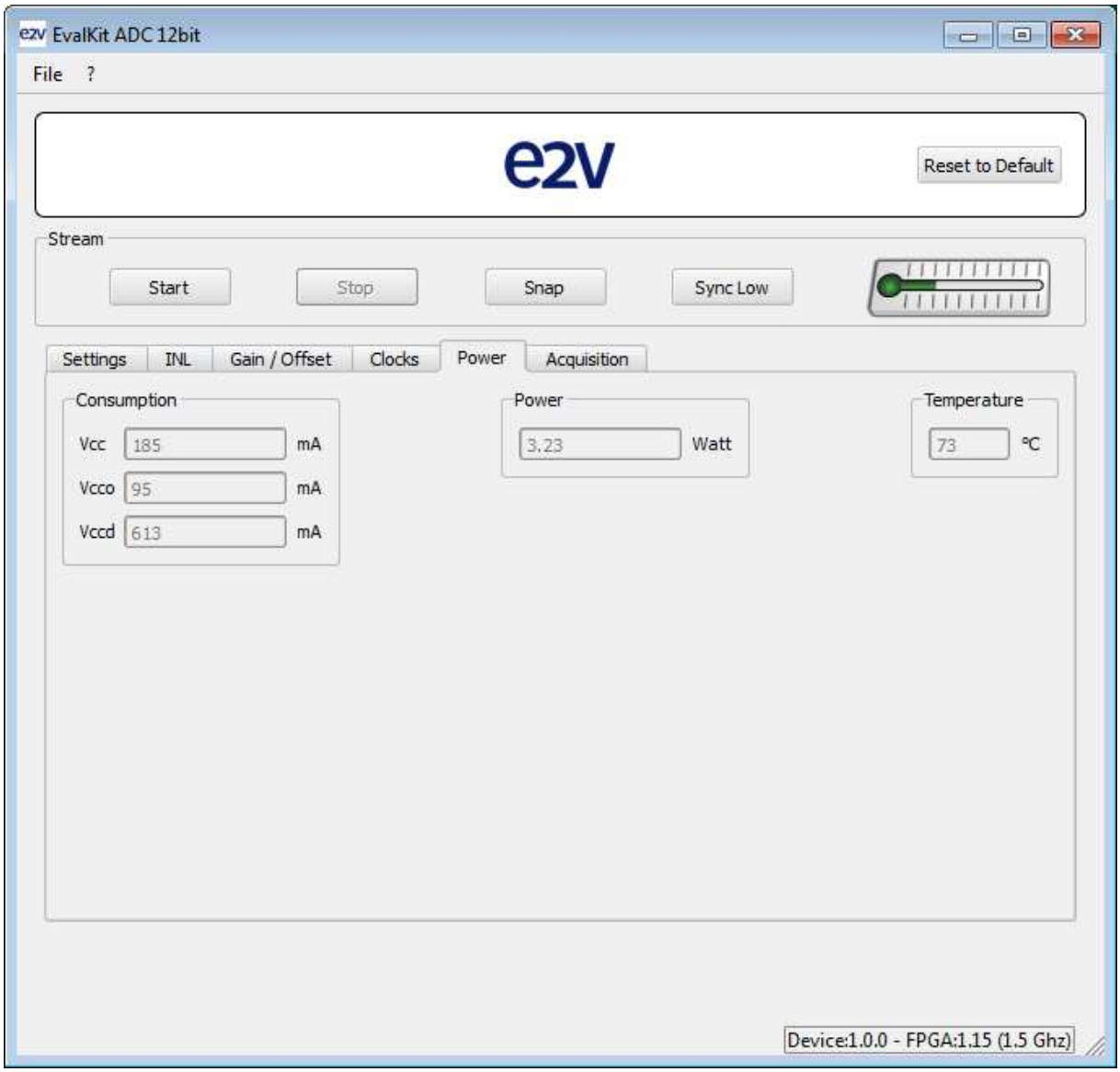
Figure 39. User Interface Demo Kit – Clock settings



4.5.5. Power

It is possible to monitor the power consumption of the EV12AS200A and to control its temperature via the internal junction temperature.

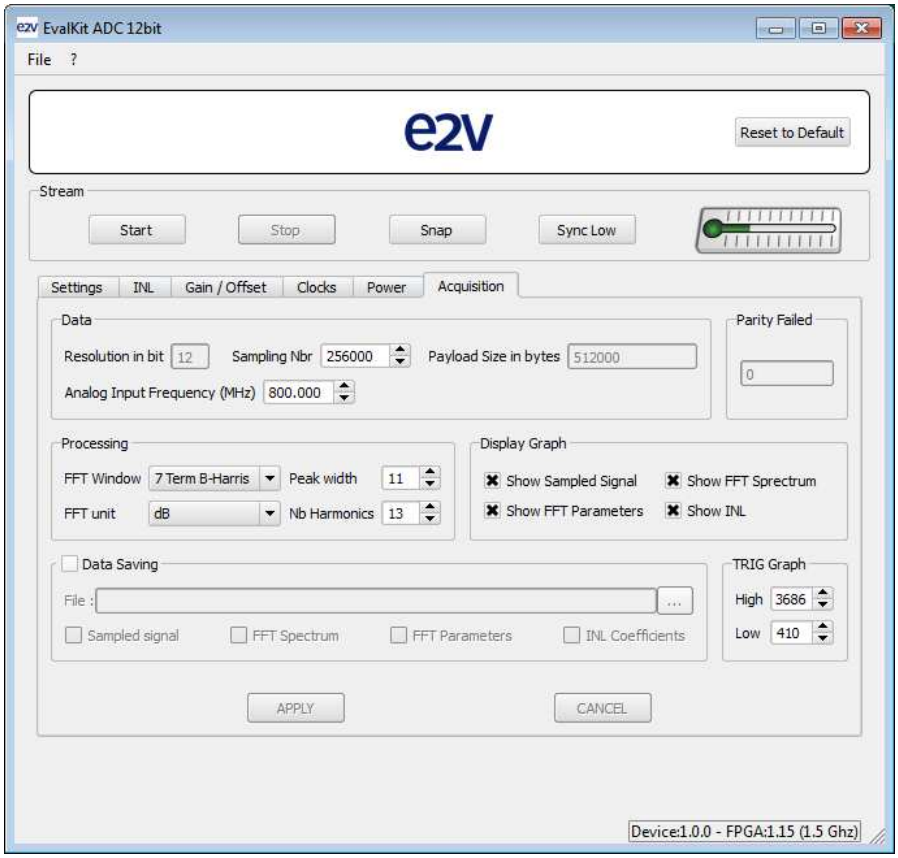
Figure 40. User Interface Demo Kit - Power



4.5.6. Acquisition control

The EV12AS200A should be configured using the Acquisition control interface.

Figure 41. User Interface Demo Kit – Acquisition control



To take into account any change of configuration, it is mandatory to press the «Apply» button.

The Acquisition window allows to set:

- The data sampling
- The data processing
- The graph displaying
- The data saving

Data:

This interface sets the data sampling configuration.

Sampling Nbr:

The number of samples which must be a 2^n number is calculated as followed:

For FFT $N=4X2^n$ (n=number bit of ADC).

For INL $N=16X2^n$ (n=number bit of ADC)

So for a 12-bit ADC, FFT must be computed with 16384 points and INL with 65536 points.

Analog Input Frequency (MHz):

By default the system takes the highest harmonic as the fundamental (H1).

In case the fundamental is not the highest harmonic of the analog input signal, it is possible to enter the Analog Input Frequency that should be considered as the fundamental of the signal.

Processing:

This is the configuration of the FFT processing.

Nb Harmonics:

Number of Harmonics considered for THD and SNR calculation (Default value is 13 harmonics)

Peak width:

When 7 Term B-Harris FFT window is applied, the Harmonic signal is composed of several points.

Default peak width value is set to 11. We advise to set this value at 25.

Display Graphs:

At the end of the acquisition it is possible to display:

- The sampled signal
- The FFT spectrum
- The INL, and
- The FFT parameters

Data saving:

Data can be saved in Excel file by setting the data saving option.

The next conversion data will be saved on the selected excel file with all the wanted values among:

- Sampled signal
- FFT spectrum
- FFT parameters, and
- INL coefficients

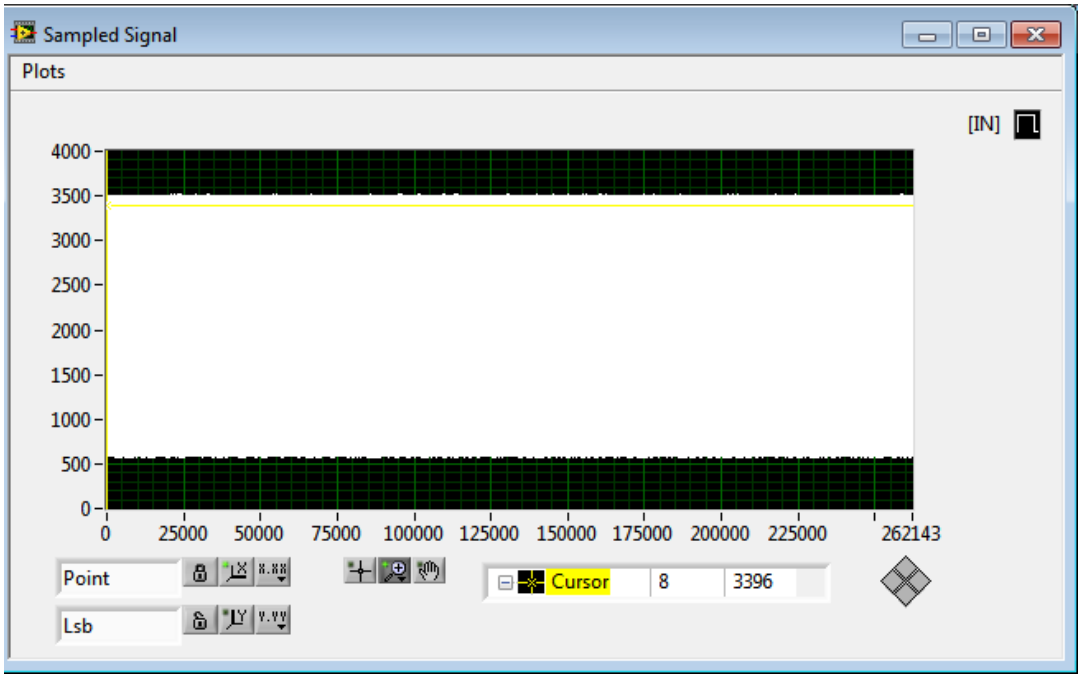
4.6. Results Interface

When an acquisition is completed, the results are displayed on four windows.

4.6.1. Sampled signal

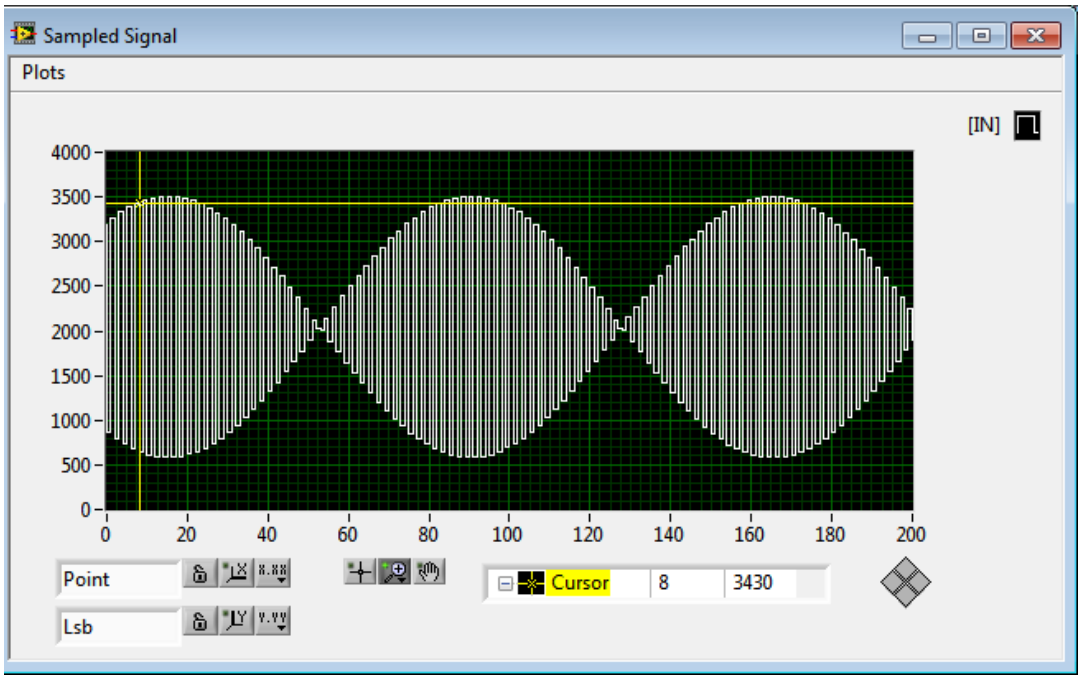
On the first window, we can observe the sampled signal.

Figure 42. Sample signal: example of 740MHz signal sampled 262144 times



By zooming we can observe discrete values.

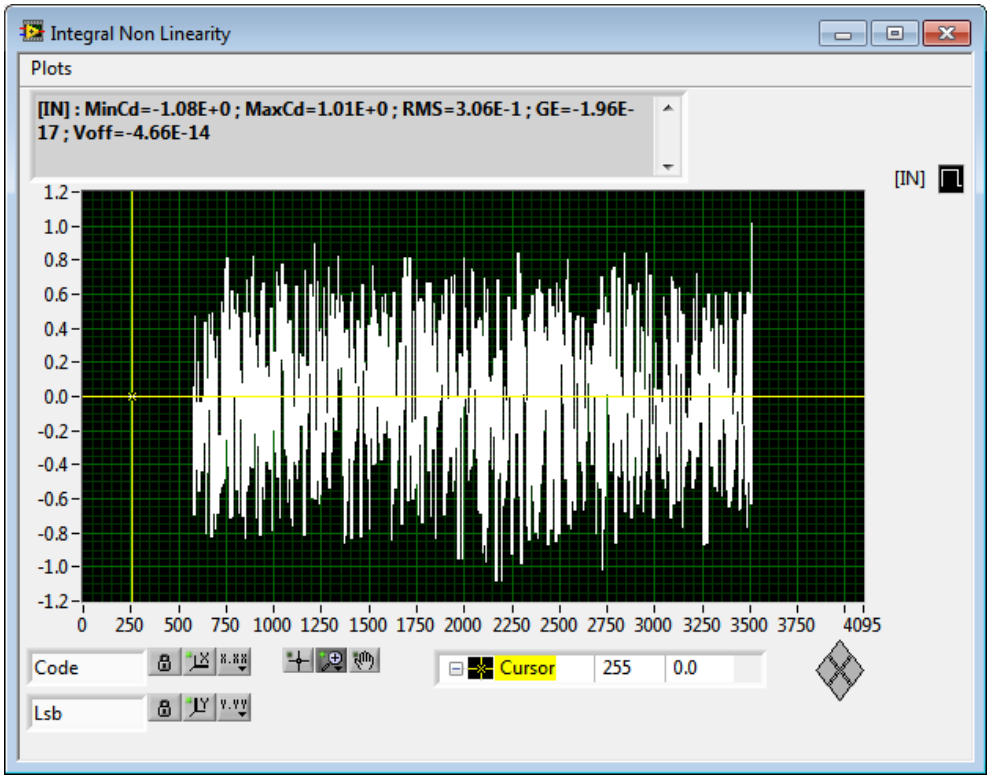
Figure 43. Sample signal: Zoom on the 200 first samples



4.6.2. Integral Non Linearity

On a second window we can see the INL of the signal.

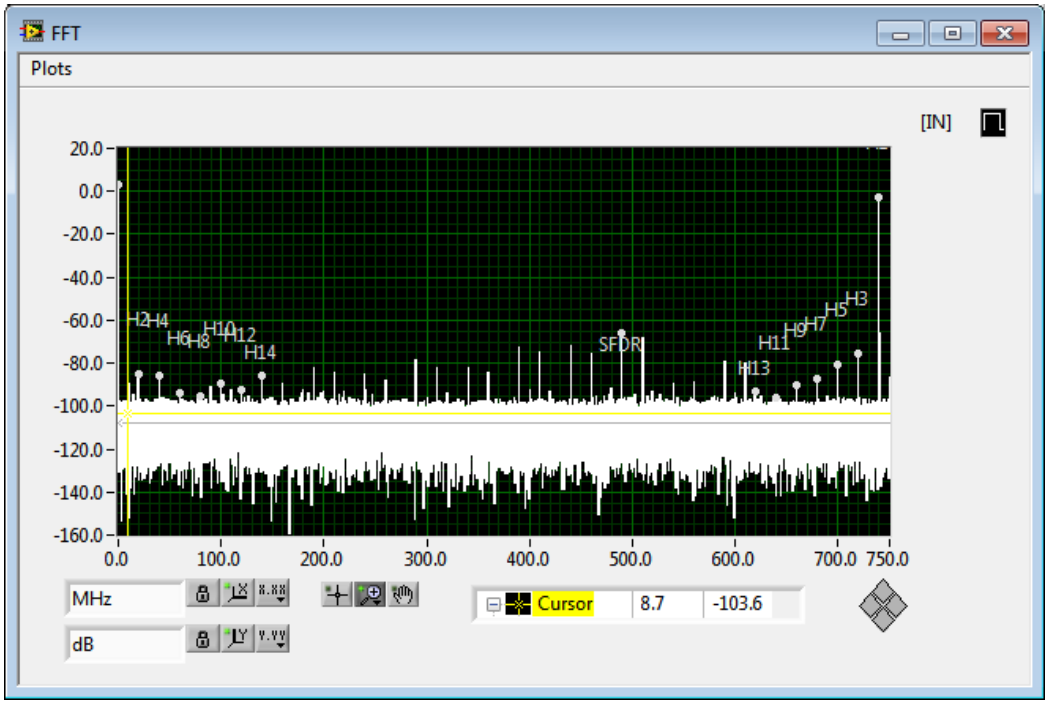
Figure 44. INL: Example of the 740 MHz signal



4.6.3. Fast Fourier Transform

A third window displays the FFT of the signal.

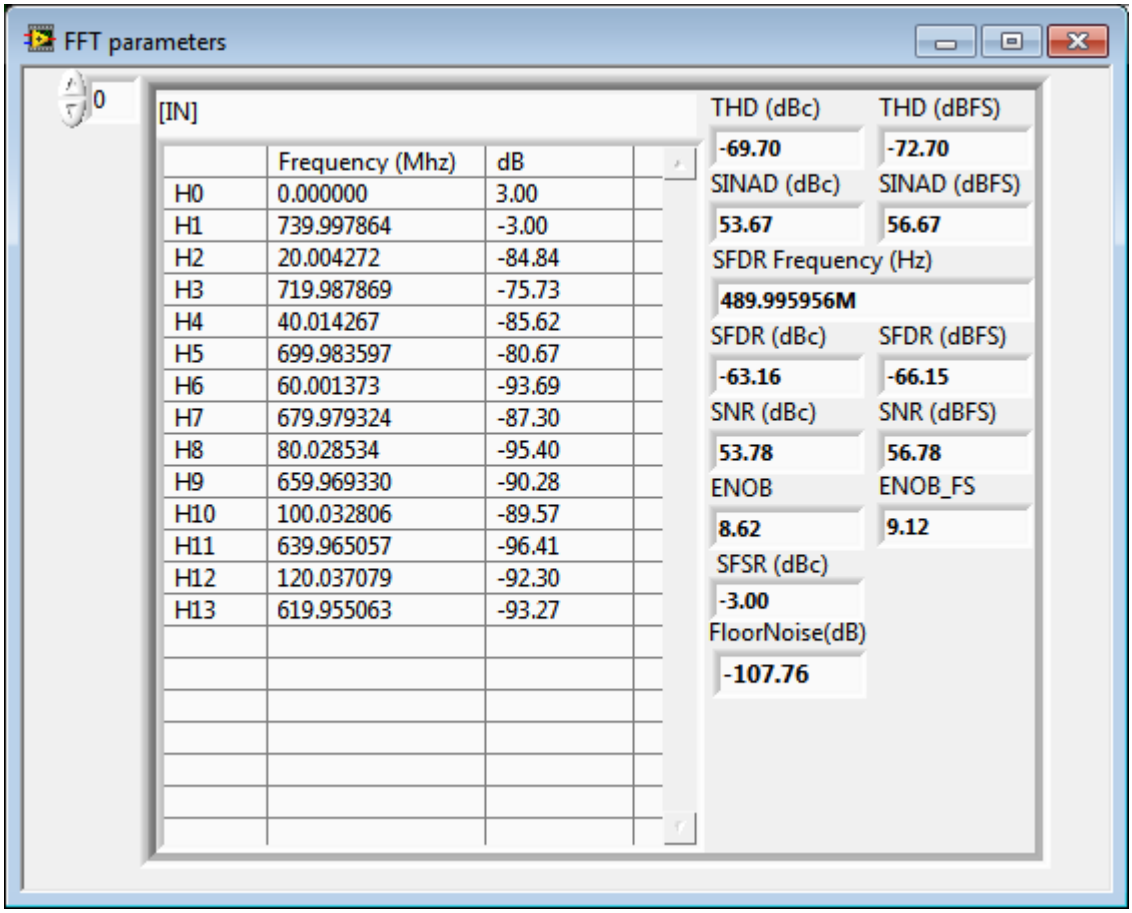
Figure 45. FFT spectrum: 740MHz FFT



4.6.4. FFT parameters

Finally the FFT parameters are synthesized on a fourth window.

Figure 46. FFT parameters: Synthesis of the sampled 740MHz signal FFT



The FFT is processed as follows:

For future calculations, we define:

Sig = Signal power level = $\sum_{0}^{N} spectrum_i^2$

Ho = Power of the continuous component = $\sum_{0}^{setup.PeakWidth} spectrum_i^2$

H1 = Power of the fundamental = $\sum_{j}^{setup.PeakWidth} spectrum_i^2$

Hi = Power of the harmonics= $\sum_{Harmonics}^{setup.cal..NbrOfHarmonics} \sum_{j}^{setup.PeakWidth} spectrum_i^2$

with setup_PeakWidth = 1 = width of one spur given in number of points;
setup_cal_NbrOfHarmonics = 5 or 10 = number of harmonics used for the spectral calculations
PmaxSpur =Power of the highest spur excluding the continuous component and the fundamental

$= \sum_{j}^{setup.PeakWidth} spectrum_i^2$

$$SFSR_{dBc} = H1_{dB}$$

$$AverageNoise_{rms} = \sqrt{\frac{Sig - H0 - H1}{N_{sig} - N_{H0} - N_{H1}}} \quad N = number, point s$$

$$THD_{dBc} = 10\log\frac{H1i}{H1}$$

$$SNR_{dBc} = 10\log\frac{H1}{Sig - H0 - H1 - H1i}$$

$$SFDR_{dBc} = 20\log\frac{Harmonic_{rms}}{fundamental_{rms}}$$

$$SINAD_{dBc} = 10\log\frac{Sig - H0 - AverageNoise_{rms}^2}{Sig - H0 - H1}$$

$$ENOB = \frac{SINAD_{dB} - 10\log 1.5}{6.02}$$

$$THD_{dBFS} = THD_{dBc} + SFSR_{dBc}$$

$$SNR_{dBFS} = SNR_{dBc} - SFSR_{dBc}$$

$$SFDR_{dBFS} = SFDR_{dBc} + SFSR_{dBc}$$

$$SINAD_{dBFS} = -10\log(10^{(-SNR_{dBFS}/10)} + 10^{(THD_{dBFS}/10)})$$

$$ENOB_{dBFS} = \frac{SINAD_{dBFS} - 10\log 1.5}{6.02}$$

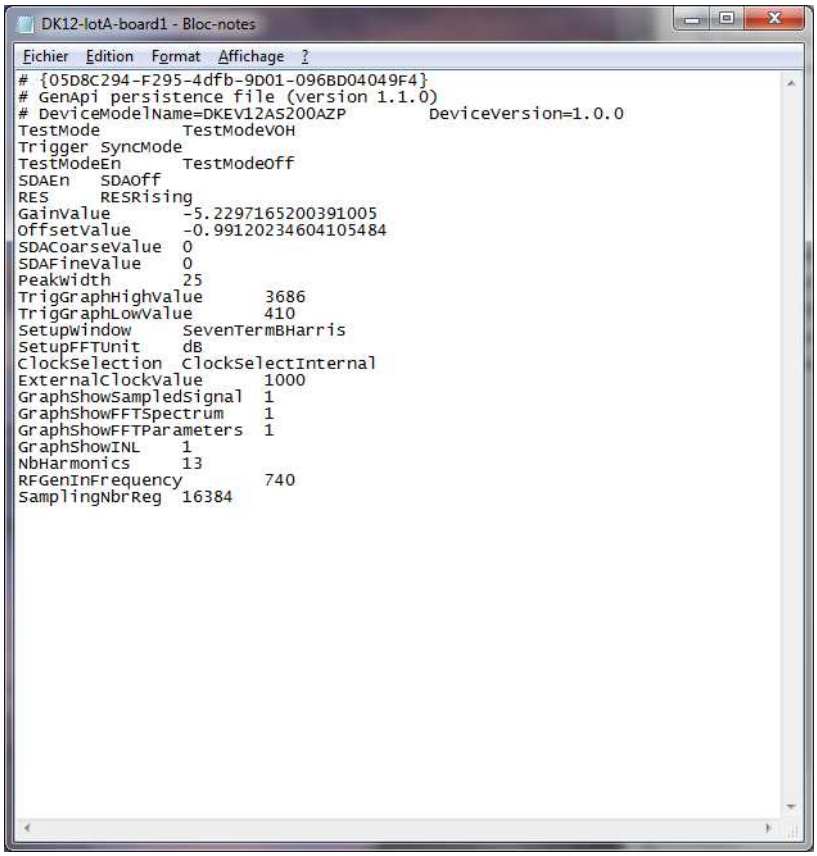
The parameters with the _FS prefix correspond to the same parameters but in dBFS (from full scale).

4.6.5. Demo Kit configuration file

In order to save time, it is possible to save the context (settings and configurations) of the Demo Kit via the File\Save Context As…\ menu.

The context is then saved as text file with a .ctx extension and can be reloaded via the File\Load Context\ menu.

Figure 47. Example of EV12AS200A-DK file

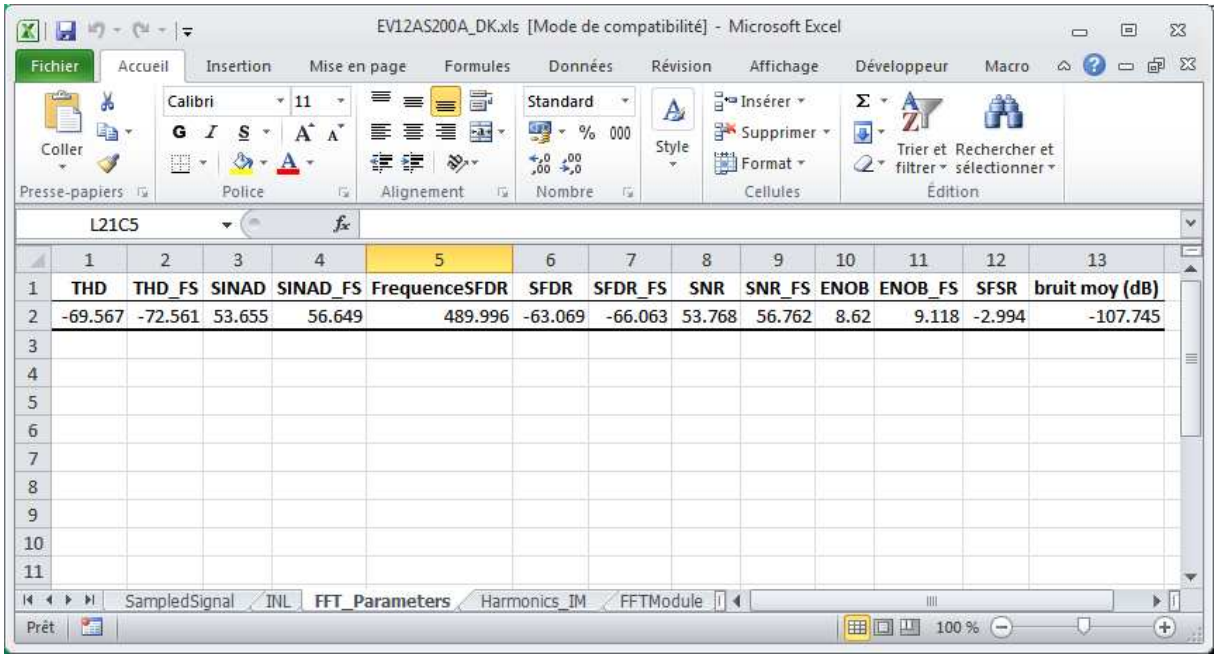


4.6.6. Data save file

It is also possible to save the data of your acquisition (saving of all FFT results). This data is stored into an Excel file with different sheet:

- INL curve in column
- FTT parameters (SFDR, THD, SNR, SINAD, ENOB) in line
- Harmonic level in columns
- FFT Module and FFT frequency in columns

Figure 48. example of Excel file



	1	2	3	4	5	6	7	8	9	10	11	12	13
1	THD	THD_FS	SINAD	SINAD_FS	FrequenceSFDR	SFDR	SFDR_FS	SNR	SNR_FS	ENOB	ENOB_FS	SFSR	bruit moy (dB)
2	-69.567	-72.561	53.655	56.649	489.996	-63.069	-66.063	53.768	56.762	8.62	9.118	-2.994	-107.745

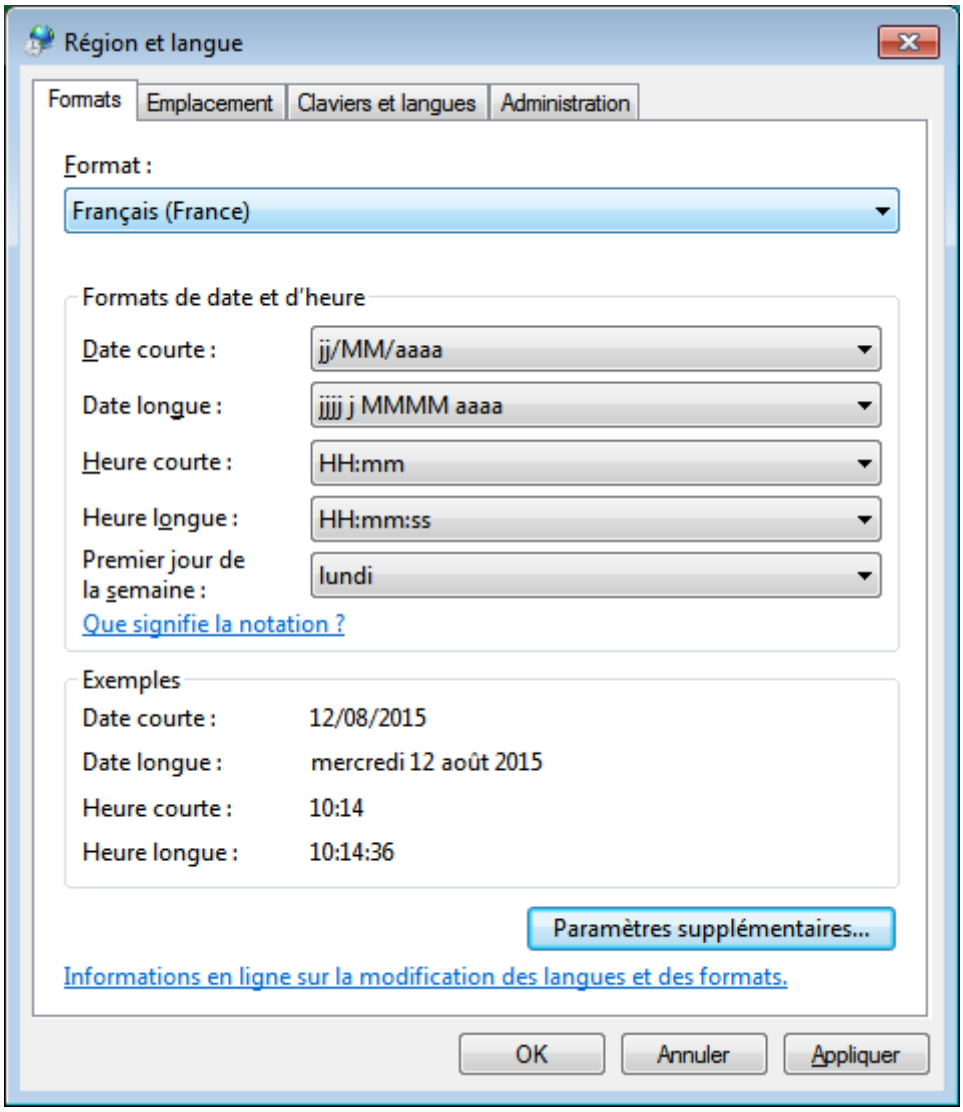
Warning: before use, your PC needs to be configured. The decimal separator must be a dot «.» instead of comma «,» like in the French version.

Use a control Regional Setting to check if decimal separator is configured with a dot «.».

4.6.7. Regional and Language Options

Use a control Regional Setting to check if decimal separator is configured with a dot «.».

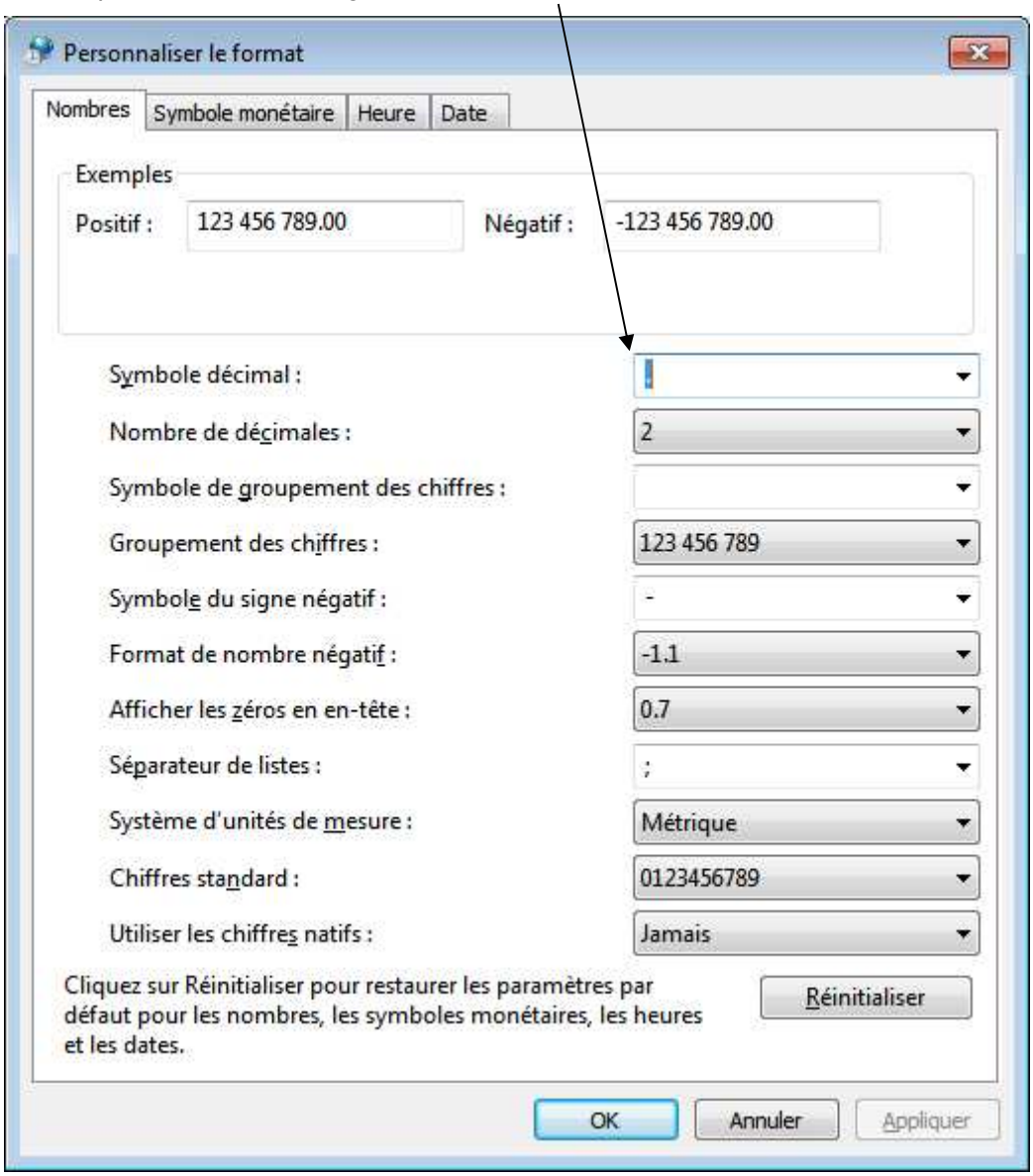
Figure 49. Regional and Language Options



Selection: Paramètres supplémentaires.

Figure 50. Customize regional Options

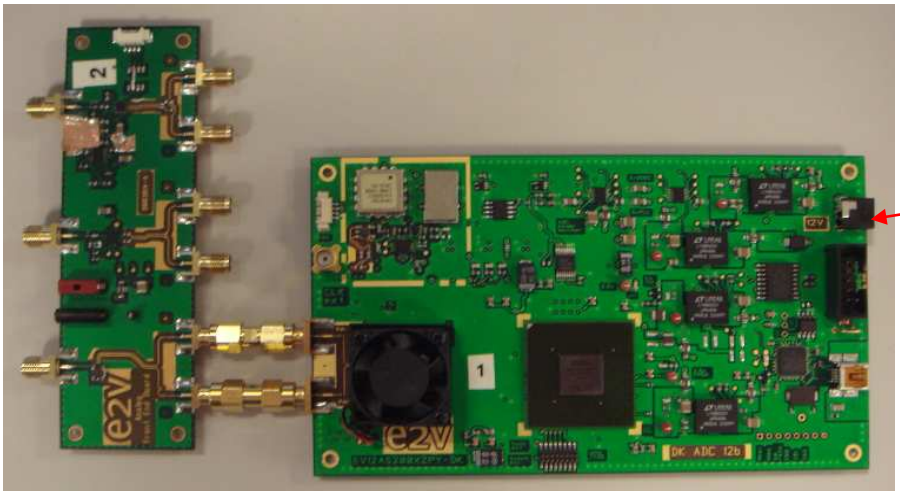
The decimal separator must be configured with a dot «.»



5 FPGA CODE

The FPGA code has been designed to be used with the onboard Altera Arria-II GX.

Figure 51. EV12AS200A Evaluation Board



5.1. FPGA binary file

A binary file is provided on the CDROM included with the Demo Kit:

5_ FPGA bin\FPGA-v1.15\bin\ adc12_top.pof

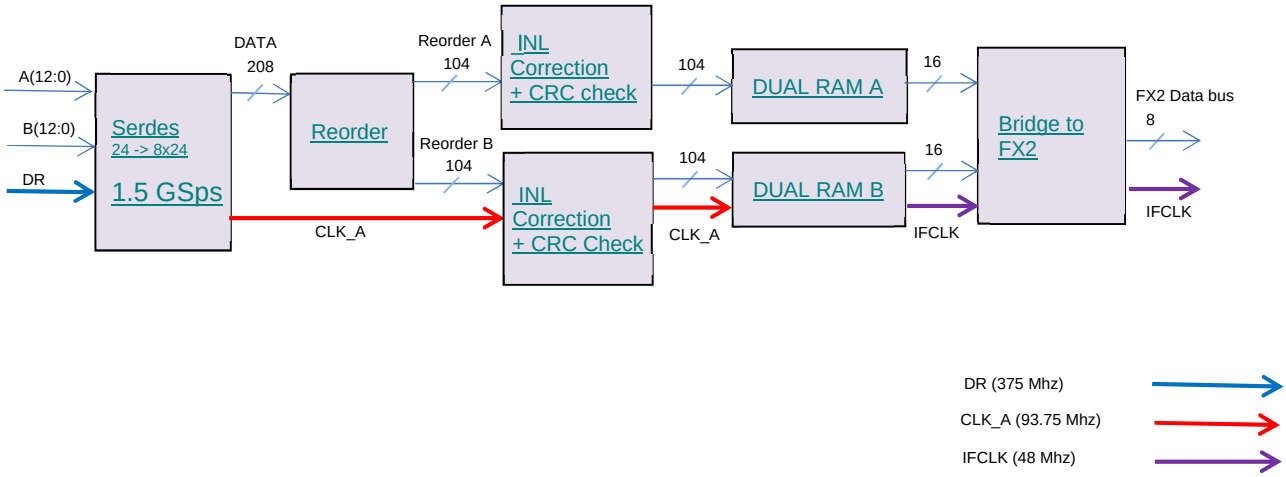
5.2. FPGA programming

1. Connect the ByteBlaster to the DK ADC 12 turn on the power supply
2. Launch the Altera programming software and select the programming method AS (Active Serial)
3. Click on «Add file» and select the file ”adc12_top.pof”
4. Select «programming», «verify»
5. Start the programming sequence
6. At the end of the sequence, disconnect the supply and then the Byte Blaster.

5.3. VHDL CODE

A documentation of VHDL architecture is provided with the Demo Kit

Figure 52. FPGA Top level simplified block diagram



6 Demo kit Hardware configuration

The Demo Kit could be hardware configured by changing manually some capacitor or resistance.

This chapter describes all user settable hardware configurations.

6.1. Clock selection

The ADC clock is generated by a PLL, but an external clock can be used (for frequency different than PLL). The selection between the two clocks is done manually with resistors.

Remove R15 and R37 resistors and solder R36 and R50 with a 0Ω.

Figure 53. ADC Clock selection schematic

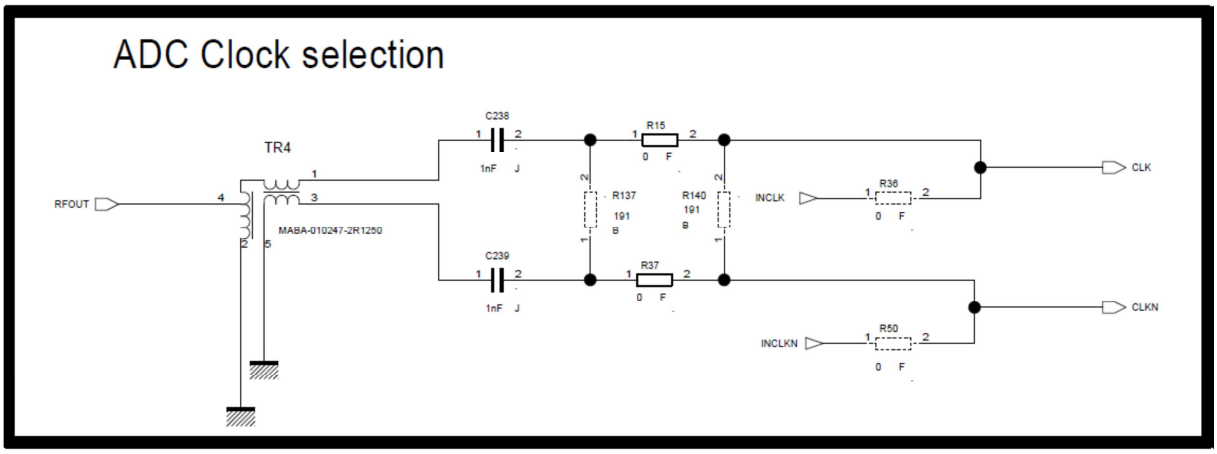
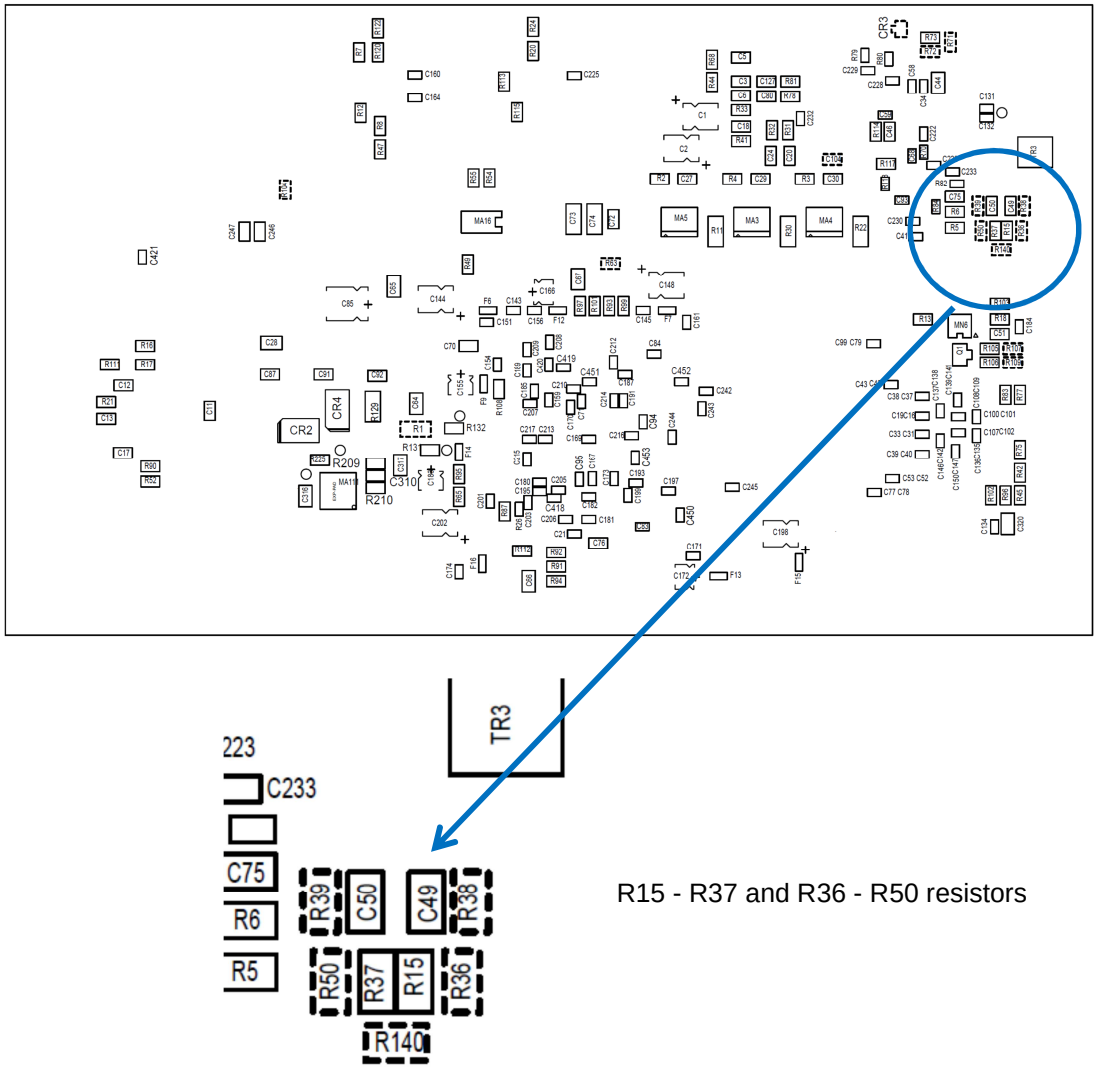


Figure 54. Implantation of resistors



R15 - R37 and R36 - R50 resistors

6.2. YNC signal

The SYNC signal is controlled by the FPGA. But it can also be controlled by an external signal on J1.1 and J1.2 pins of the GPIO JTAG connector.

The selection between the two signals is done manually with a resistor.

Remove R105 and R106 resistors and solder R107 and R109 with a 0Ω.

Figure 55. SYNC schematic (folio 6/11)

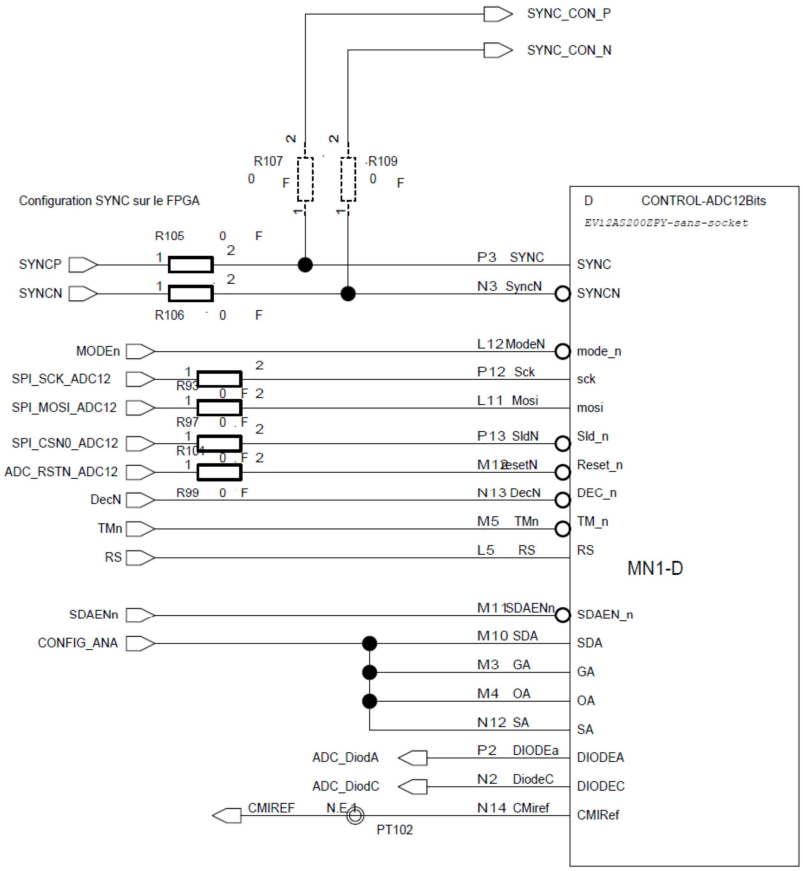
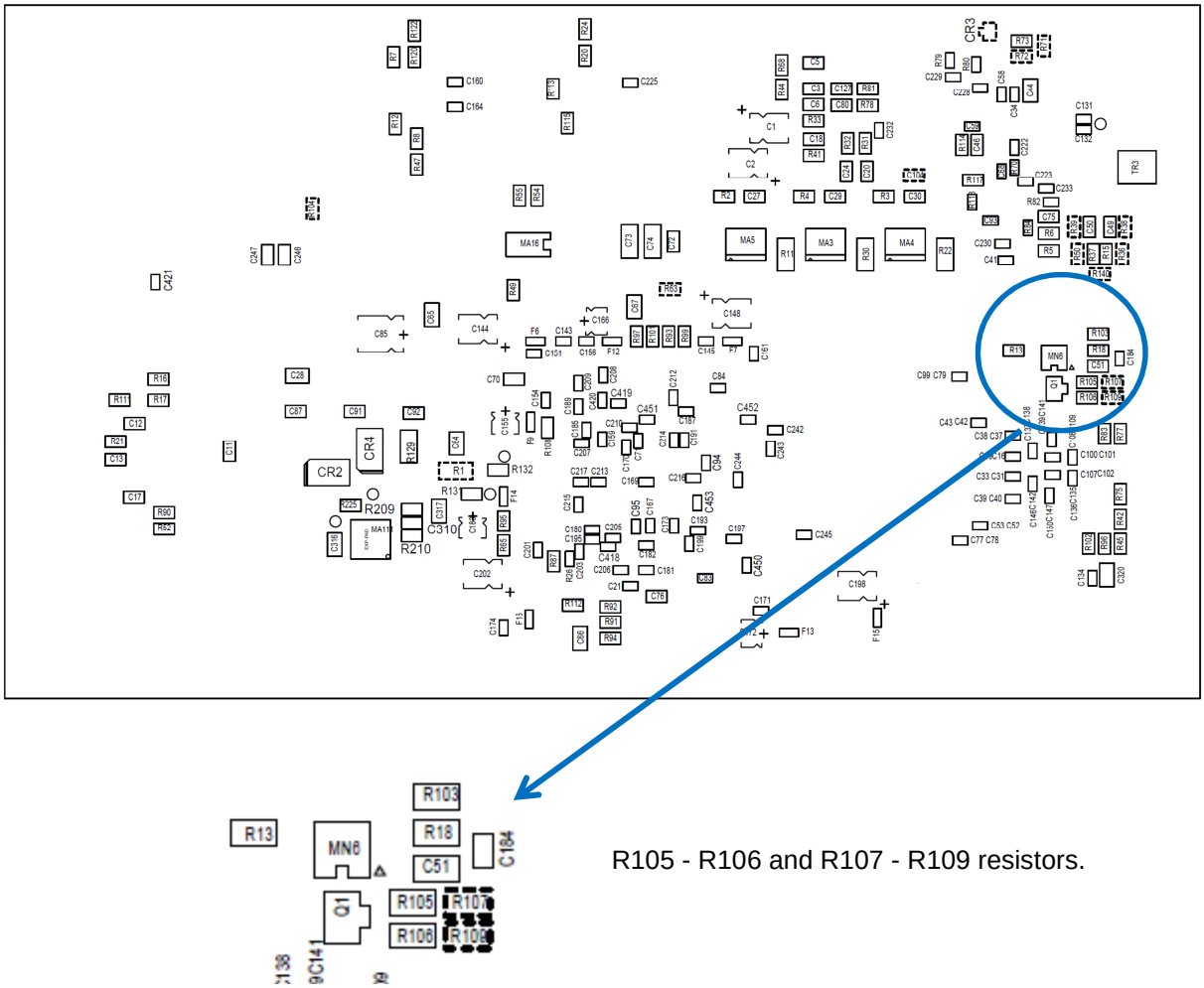


Figure 56. Implantation of resistors



R105 - R106 and R107 - R109 resistors.

7 Board Schematics

For BDC support about Board Schematics, please contact Hotline-BDC@e2v.com

8 Layout information

For BDC support about Layout information, please contact Hotline-BDC@e2v.com

9 Mechanical dimensions

The Demo Kit board with 12-bit ADC dimension is 141mm x 87mm

The analog front board with 3 inputs dimension is 118mm x 37 mm

The two boards weigh 150g

10 Electrical Specification

Power Supply 12V +/- 5% 1A max

Analog Input Full Scale 500mVpp : Max Value 4Vpp (13dBm into 100Ohm)

Clock Input (Optional) Max Value 3Vppp

11 Ordering Information

Table 1. Ordering information

Part Number	Temperature	Comments
EV12AS200AZPY-DK	Ambient	ROHS compliant

EV12AS200A-DK

Table of contents