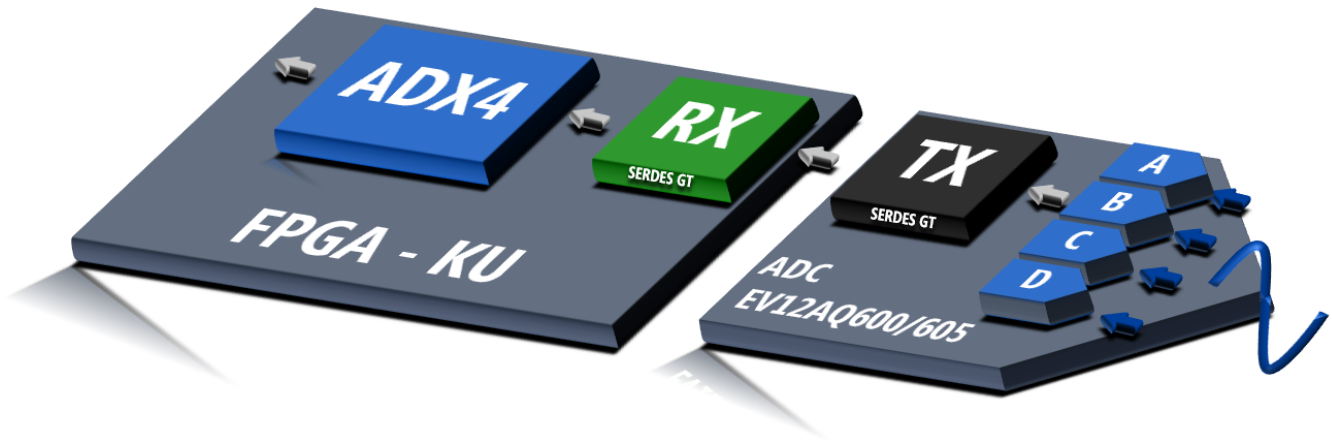
ADX4 IP

EV12AQ600-ADX-EVM

Design example User Guide



1 Summary

2 Introduction

2.1 ADX4 IP

Teledyne e2v provides the ADX4 IP and a vhdl wrapper to reduce EV12AQ600/605 ADC time interleaving spurious effects (fc/4-fin, fc/4, fc/4+fin and fc/2-fin) when the ADC is configured in 1 channel mode (4 ADC cores are interleaved). When the ADC is configured in 2 channels mode, the ADX2 IP must be used to reduce time interleaving spurious effects (fc/2-fin).

When the ADC is configured in 4 channels mode, all cores are independent and no ADX IP is required. No time interleaving spur to remove in 4 channels mode.
The ADX4 IP allows to cancel time interleaving gain, phase and DC-offset mismatch effects by real time post processing treatment without implementing a complex and time-consuming calibration process.
The ADX4 IP must be implemented on a Xilinx Kintex Ultrascale FPGA.
For another FPGA reference, please contact your local FAE or send an email at GRE-HOTLINE-BDC@Teledyne.com.

To learn more on how the ADX IP and time-interleaved ADC error correction work, Teledyne SP Devices provides technical details in a webinar and a white paper available here: https://www.spdevices.com/technology/interleaving.

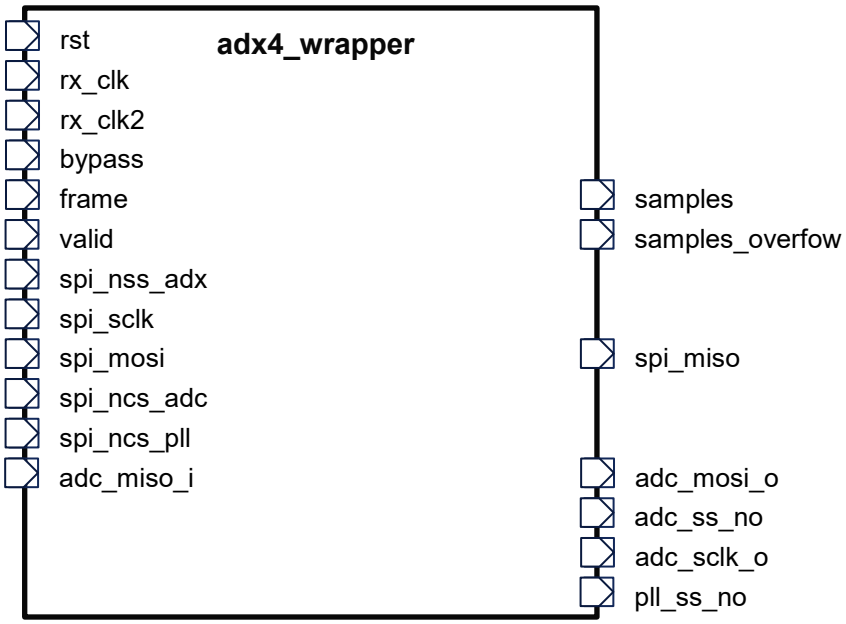


Figure 1 – ADX4 IP VHDL wrapper overview.

2.2 Evaluate the ADX4 IP

The EV12AQ600-ADX-EVM demonstration kit is available to start evaluating the ADX4 IP and ADX2 IP. EV12AQ600-ADX-EVM user guide available here.

To order the demonstration kit, please contact your local FAE or send an email at GRE-HOTLINE-BDC@Teledyne.com.

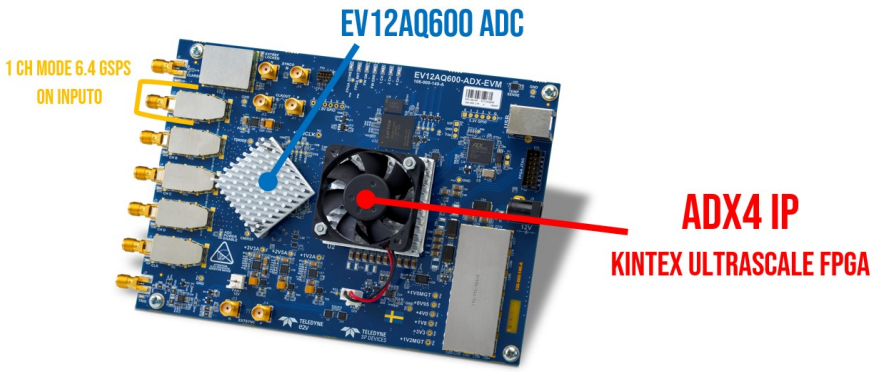


Figure 2 – EV12AQ600-ADX-EVM Demonstration Kit

2.3 ADX4 design example

To facilitate the ADX4 IP integration in the application design, a design example is provided with ADX4 IP.
The design example is based on EV12AQ600-ADX-EVM demonstration kit.

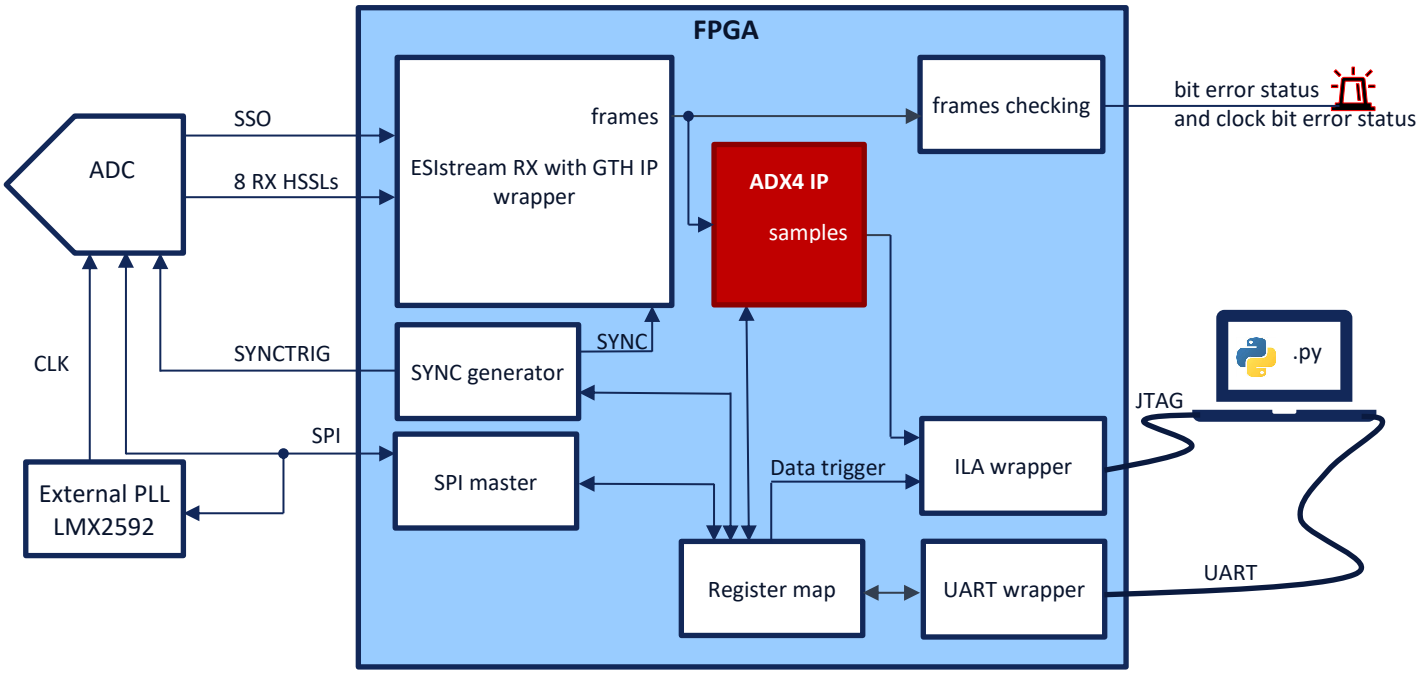


Figure 3 – design example overview

A UART interface (8-bit, 115200) allows to read and write FPGA registers from a python Graphical User Interface (GUI). A frames layer protocol has been defined to communicate with the register map using UART.
The GUI also allows to display the samples in both time and frequency domain.
Samples are acquired using Vivado Integrated Logic Analyser (ILA) and JTAG.
The register map contains registers to control all FPGA modules of the design example like ESIstream receiver (RX), SPI Master, SYNC generator and ADX4 IP.

The frames checking module allows to check the ESIstream decoded frames that contain samples when the ADC is configured in ramp test mode. If a bit error is detected in one of the frame transmitted between the ADC and the FPGA then flag is raised, and a LED turns ON (red).
Note: When the ADC is configured in normal mode, after a SYNC the LED always turns ON (red).

3 Hardware

3.1 List of materials

- EV12AQ600-ADX-EVM board and +12V/5A power supply: User guide
- Xilinx programmer: HW-USB-II-G
- USB to UART FTDI cable: FTDI TTL-232RG-VREG1V8-WE
- SMB100A signal generator
- SMA cable
- Low Pass Filter (LPF) or Band Pass Filter (BPF) to filter harmonics of the signal generator.

3.2 Setup

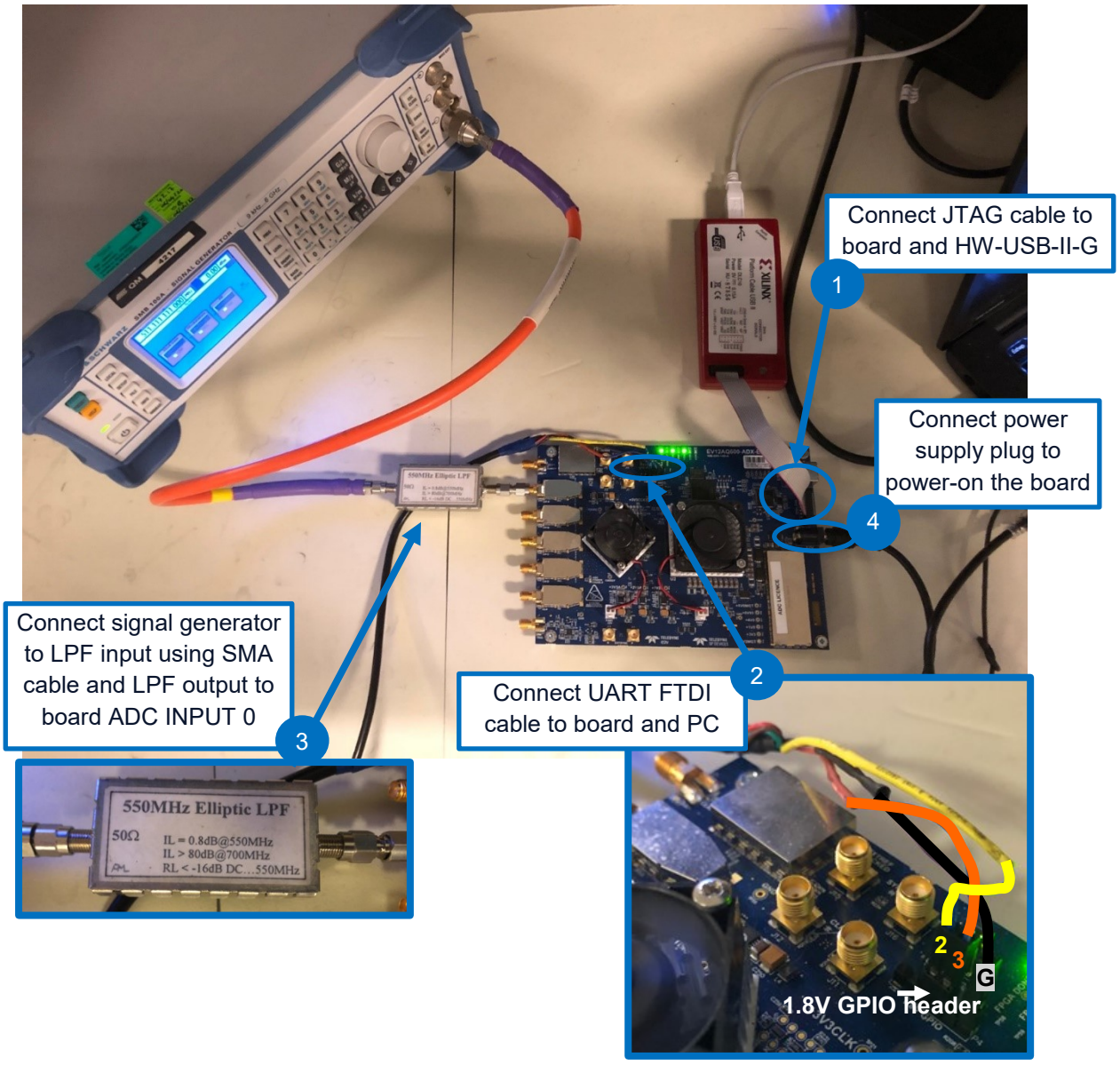
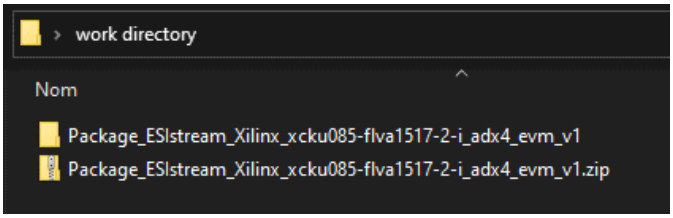


Figure 4 – Hardware setup overview

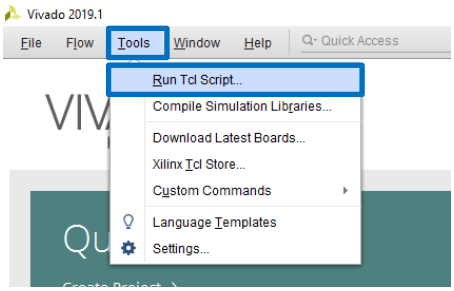
Note: USB3 connector is not used with the design example and can be left unconnected.

4 Generate Vivado project

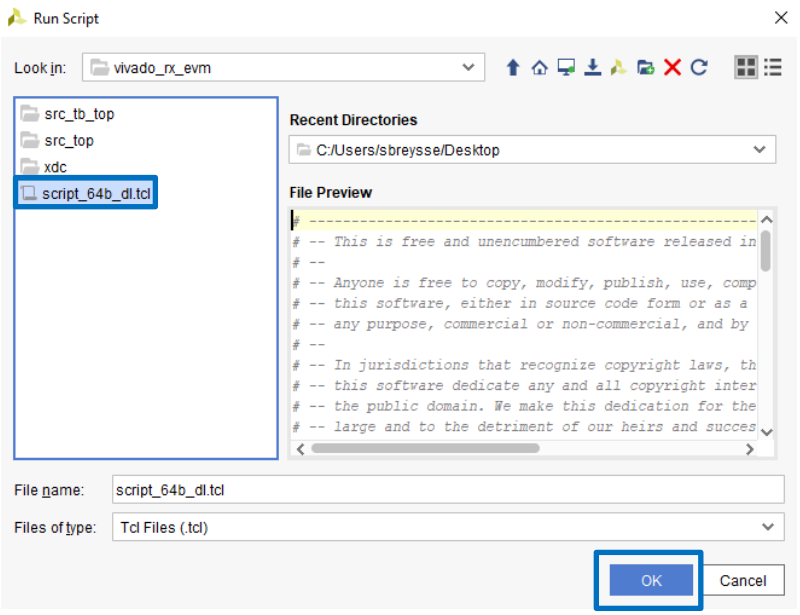
Copy and ***unzip*** the latest version of the vhdl design example ***package in your work directory***:
Package_ESIstream_Xilinx_xcku085-flva1517-2-i_adx4_evm_v1



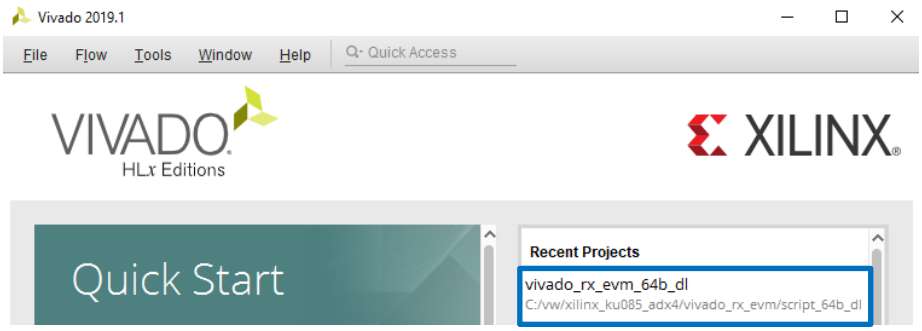
Open vivado 2019.1 and click on ***Tools*** and then on ***Run TCL script…***



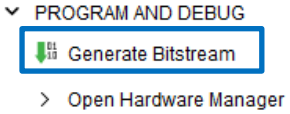
Browse and ***select*** the TCL script, ***script_64b_dl.tcl***, located in:
\work directory\Package_ESIstream_Xilinx_xcku085-flva1517-2-i_adx4_evm_v1\vivado_rx_evm
Click ***OK*** and the project generates automatically.
It takes few minutes to complete.



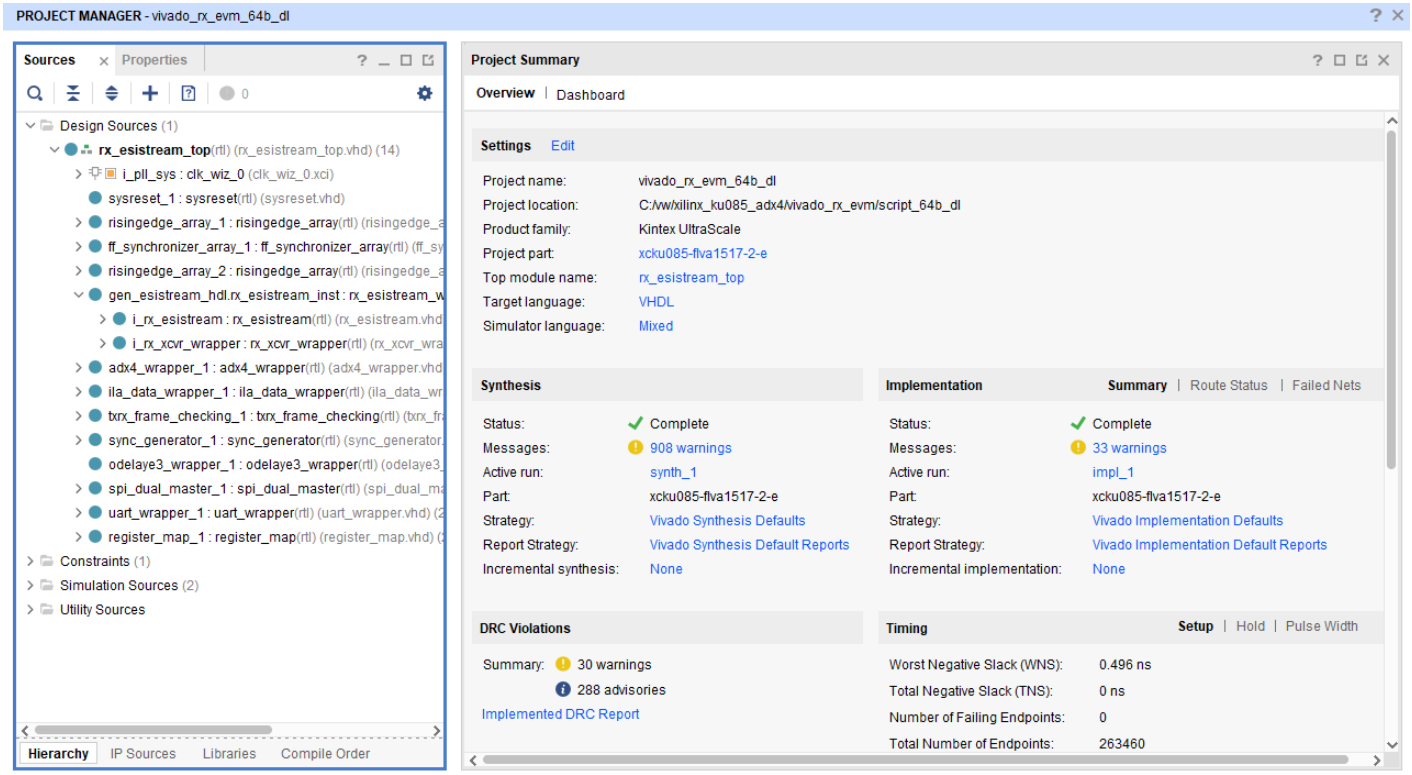
At the end of the project generation, the project closes.
Click on the ***project*** in the ***Recent projects*** view to open it.



Click on ***Generate Bistream***.
It takes one hour and a half to generate the bitstream.

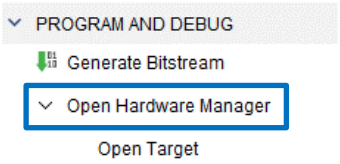


At the end of the project generation the ***Project Manager*** should look as shown below:

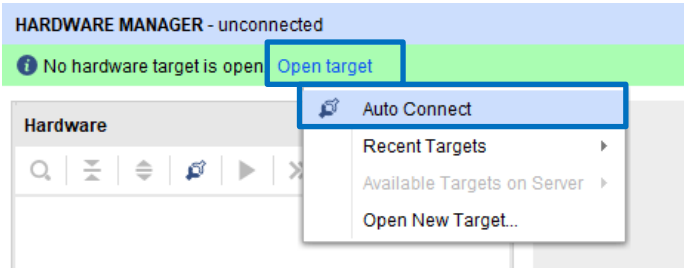


5 Program the FPGA

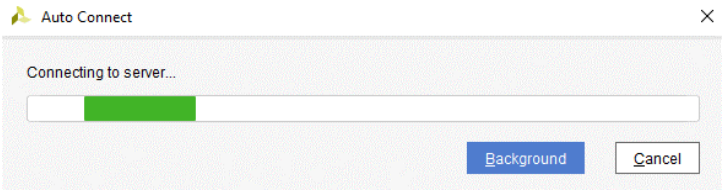
Click on ***Open Hardware Manager***



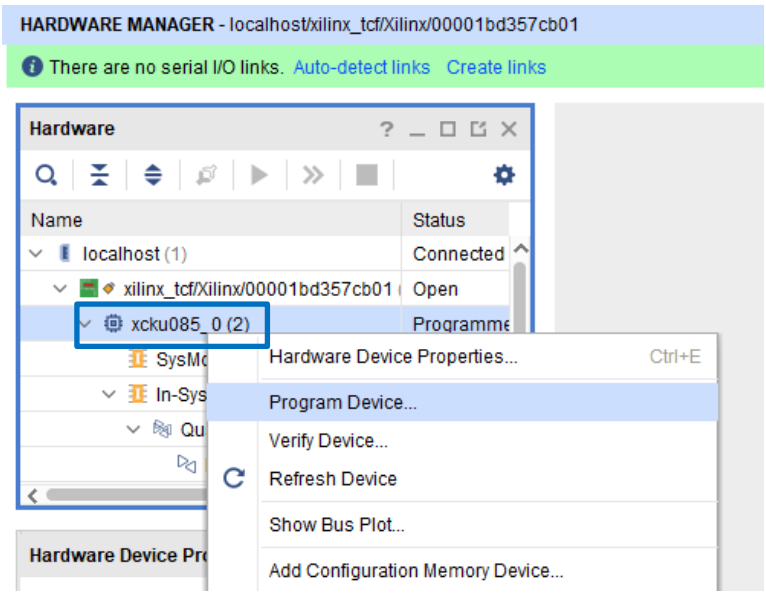
Click on ***Open target*** and then on ***Auto Connect***



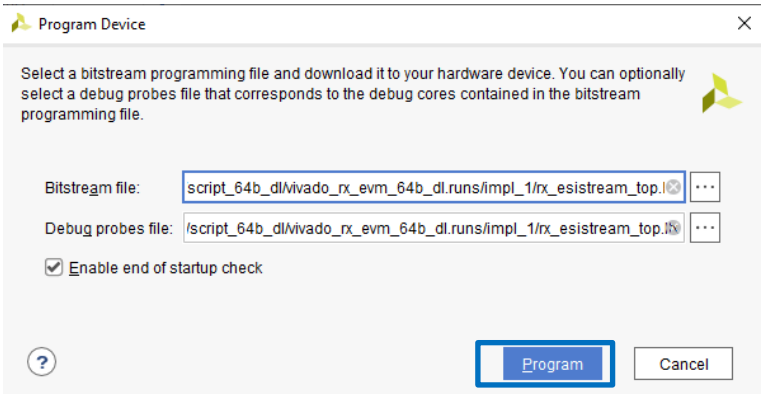
Wait…



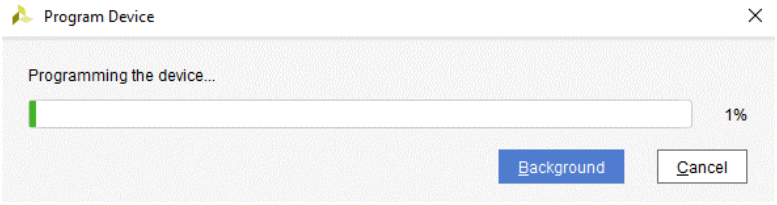
Right-click on ***FPGA reference (xcku085)*** and then click on ***Program Device…***



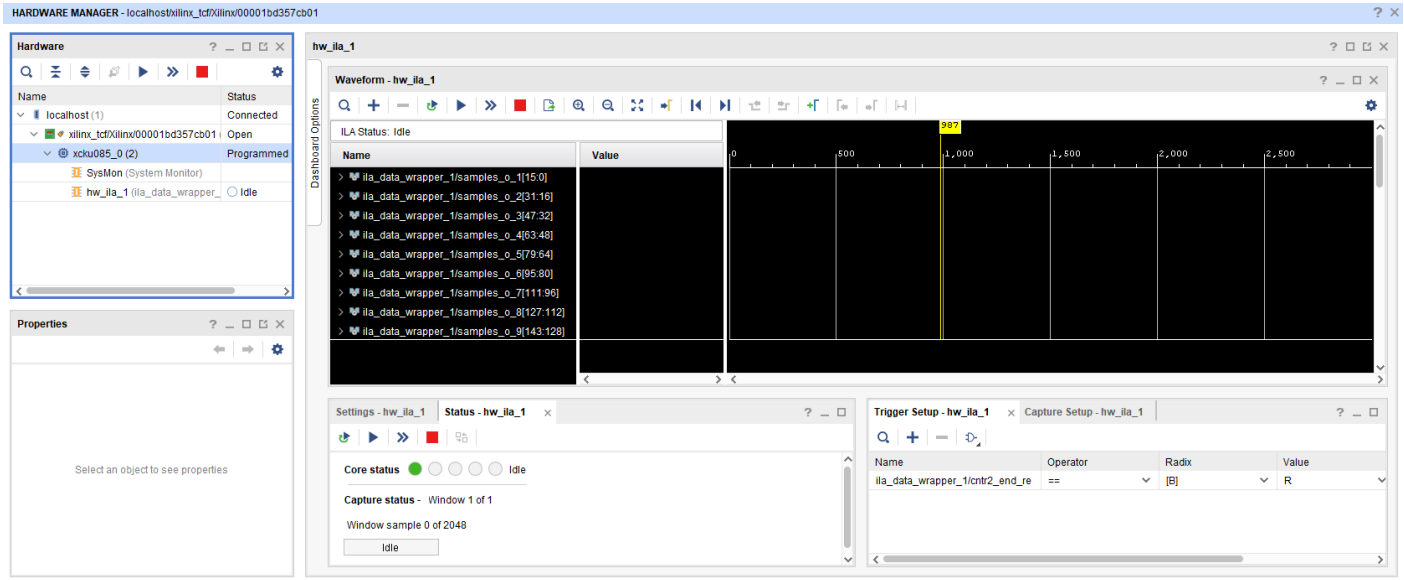
Click on ***Program***



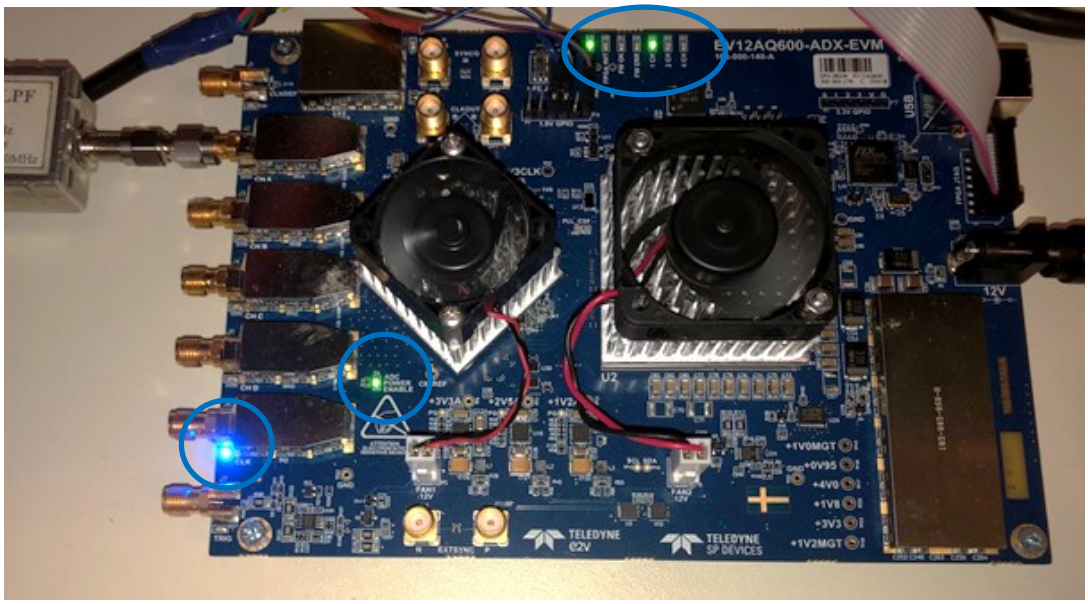
Wait end of programming…



At the end of programming, the ***Hardware Manager*** should look as shown below:



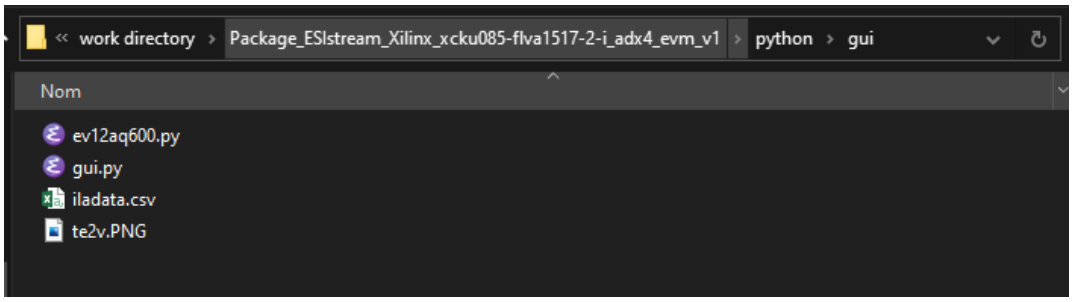
At the end of programming, the **board leds state** should look as shown below:



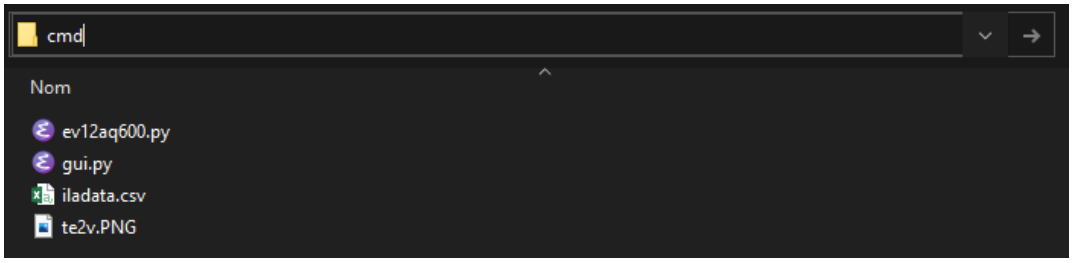
6 GUI

6.1 Open the GUI

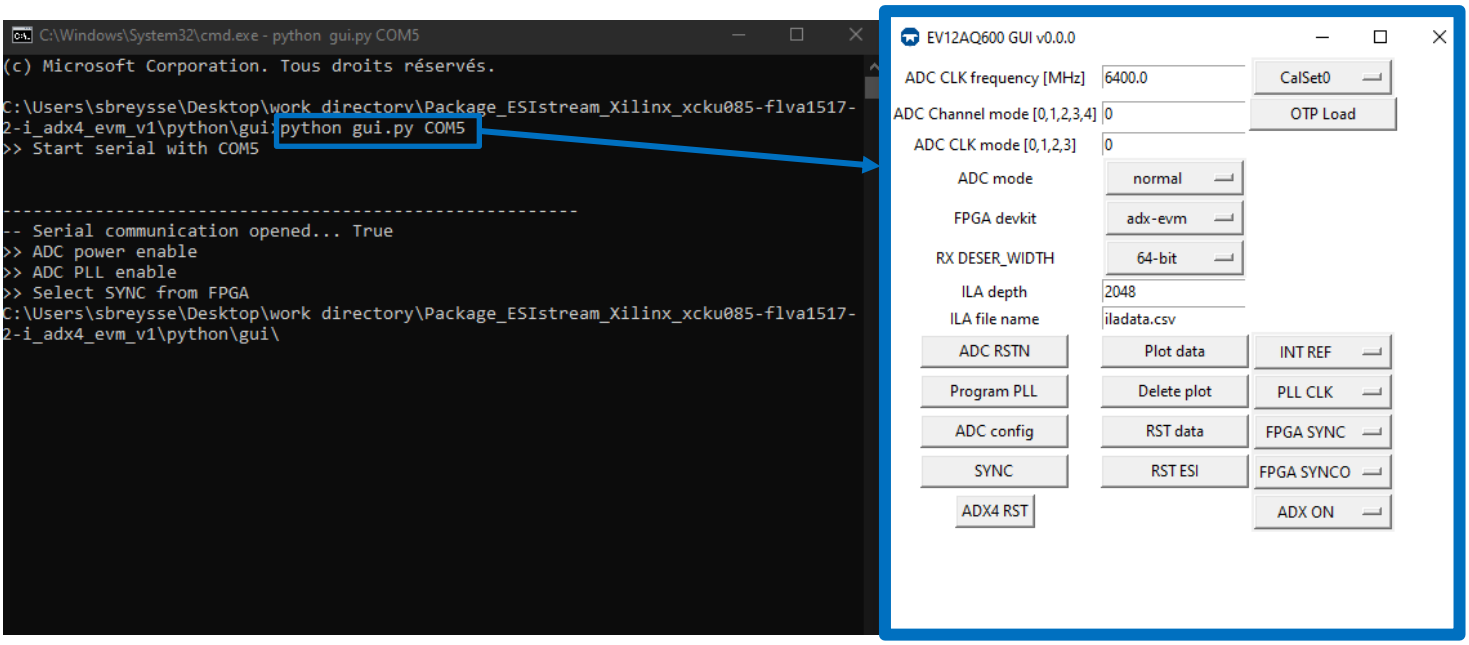
Go to package ***gui*** directory located in:
\work directory\Package_ESIstream_Xilinx_xcku085-flva1517-2-i_adx4_evm_v1\python\gui



Type ***cmd*** in file explorer and press ***enter*** to open a cmd window.



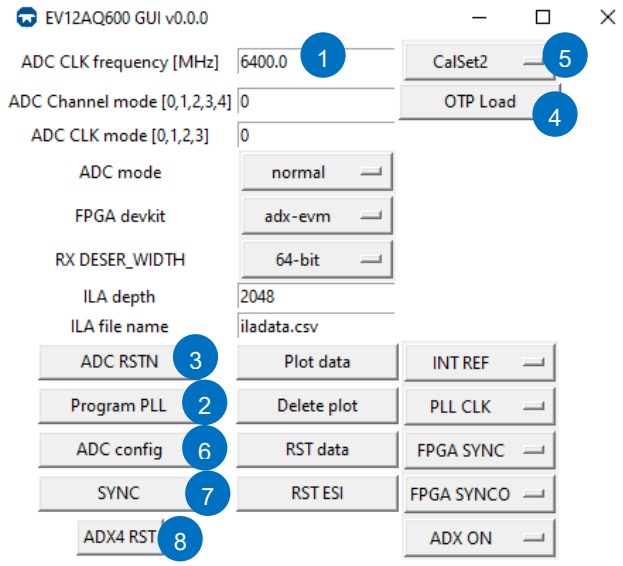
Type ***python gui.py COM5*** in the cmd window and press **enter** to open the GUI.
The COM id can change. Check the device manager to get the right COM id.



6.1 Configure the ADC and activate the ADX4 IP license

In the GUI:

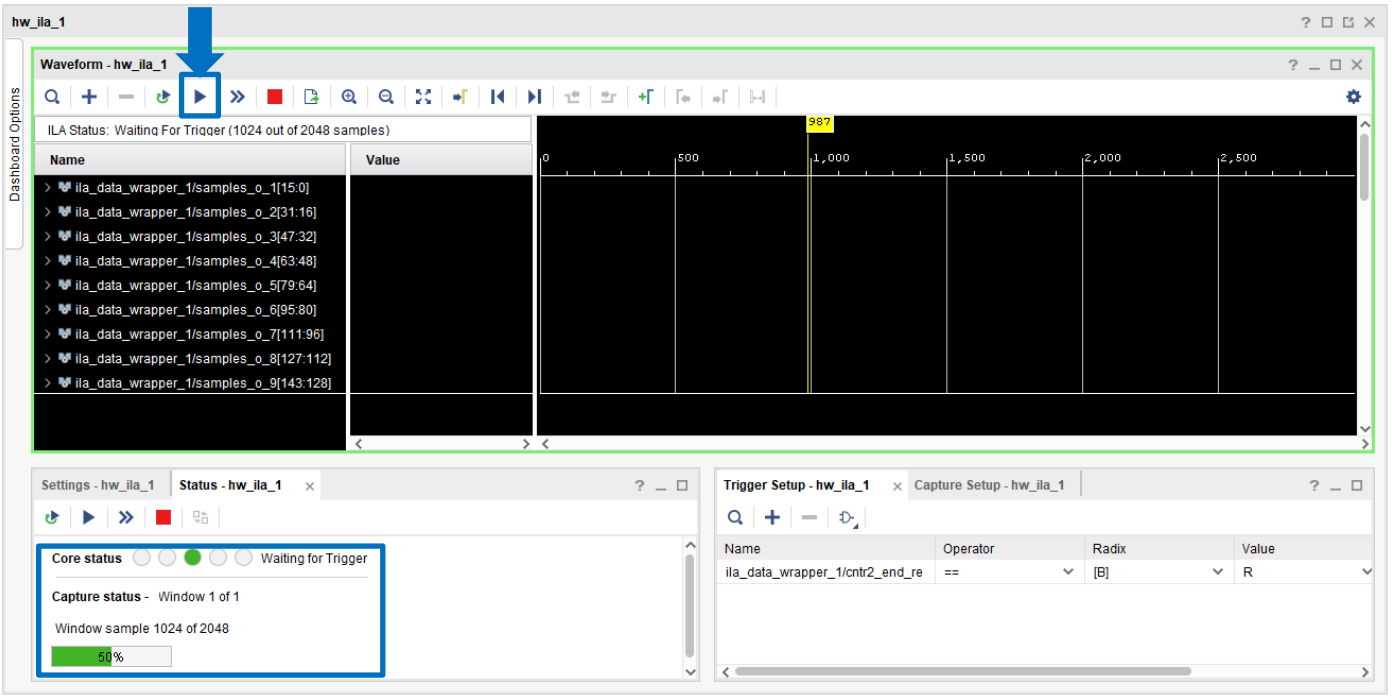
1) Select ADC CLK frequency (6400 MHz, 6250 MHz, 5000 MHz or 4900 MHz).
   - For another f_{ADC_CLK}, contact support, mailto:GRE-HOTLINE-BDC@Teledyne.com
2) Click on **Program PLL**
3) Click on **ADC RSTN**
4) Click on **OPT Load**
5) Select the right calibration set according to your input frequency and temperature range.
6) Click on **ADC config**
7) Click on **SYNC**
8) Click on **ADX4 RST** to activate the ADX4 IP



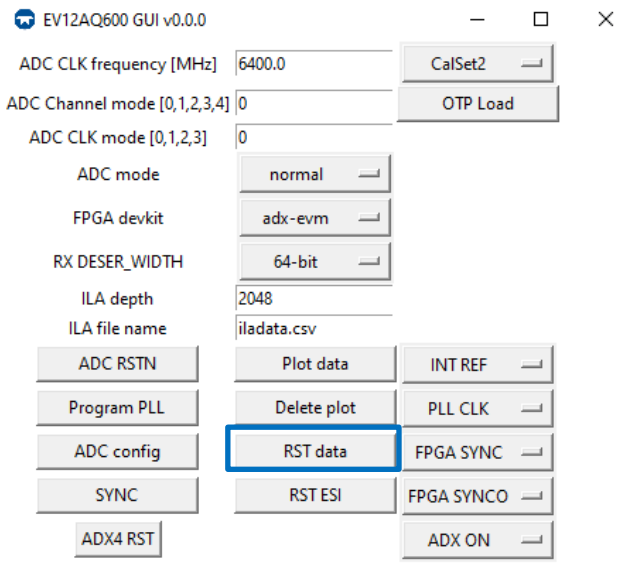
6.2 Acquire samples using Vivado ILA hardware manager and the GUI

In vivado hardware manager ILA, click on the ***play button*** to launch an acquisition.

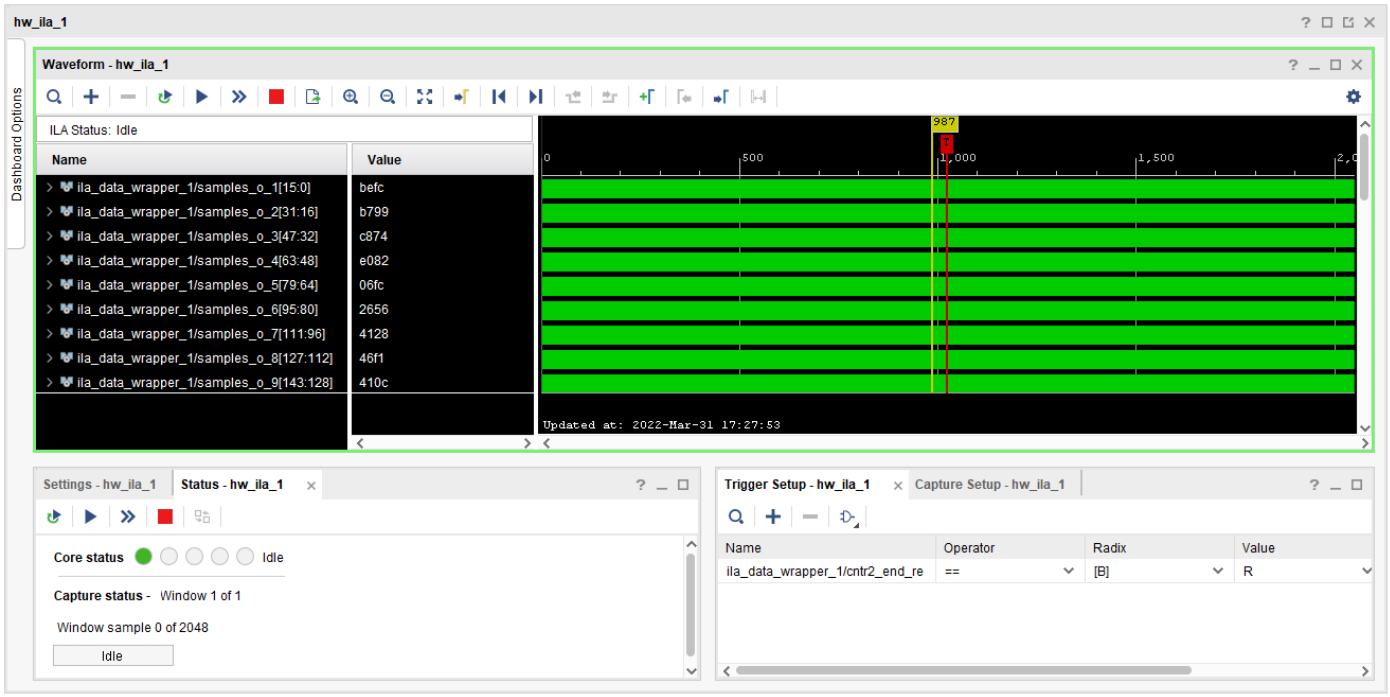
Then vivado ILA is waiting for Trigger.



Generate the data trigger in the GUI clicking on **RST data**:



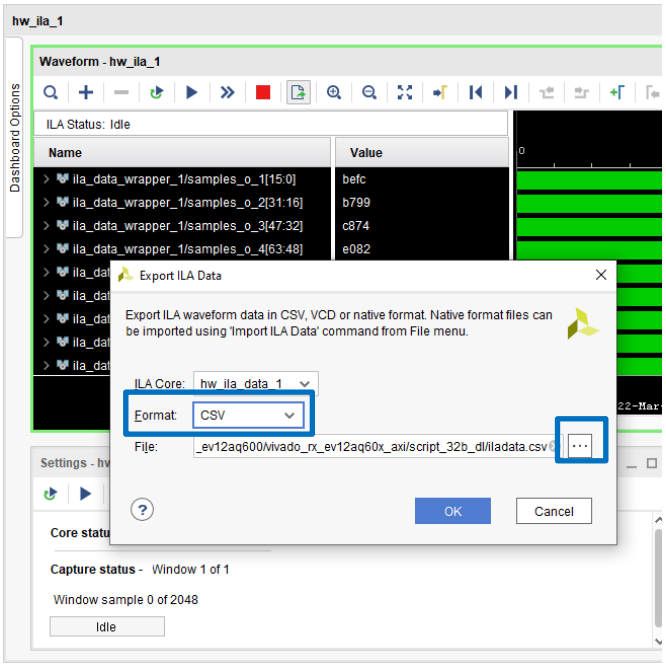
Samples are acquired in Vivado ILA hardware manager.



Click on ***Export ILA Data*** button:

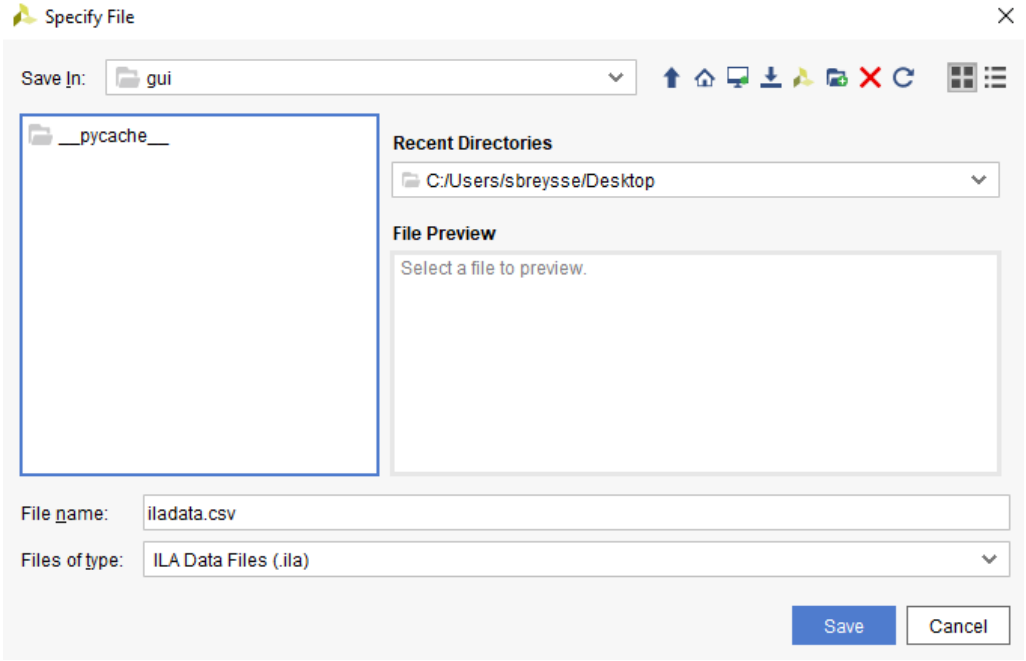
Select **CSV** format.

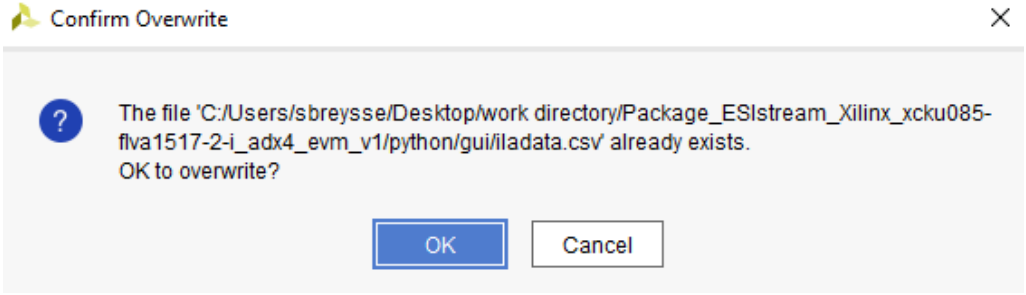
And **browse** to select the output directory.



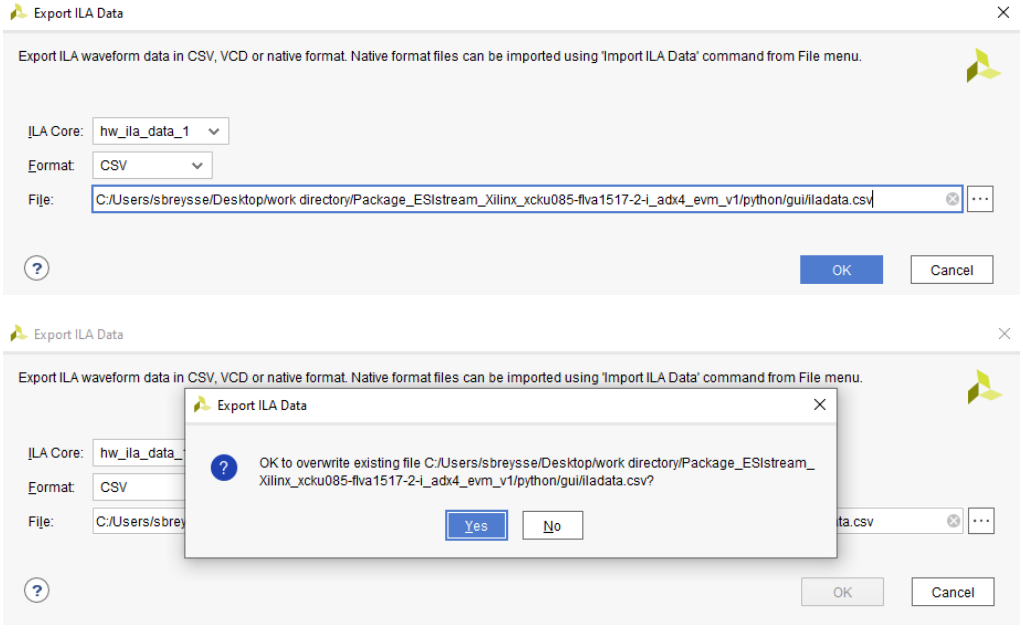
Select the output directory:
\work directory\Package_ESIstream_Xilinx_xcku085-flva1517-2-i_adx4_evm_v1\python\gui

Click on ***Save*** and confirm overwrite clicking on ***OK***.



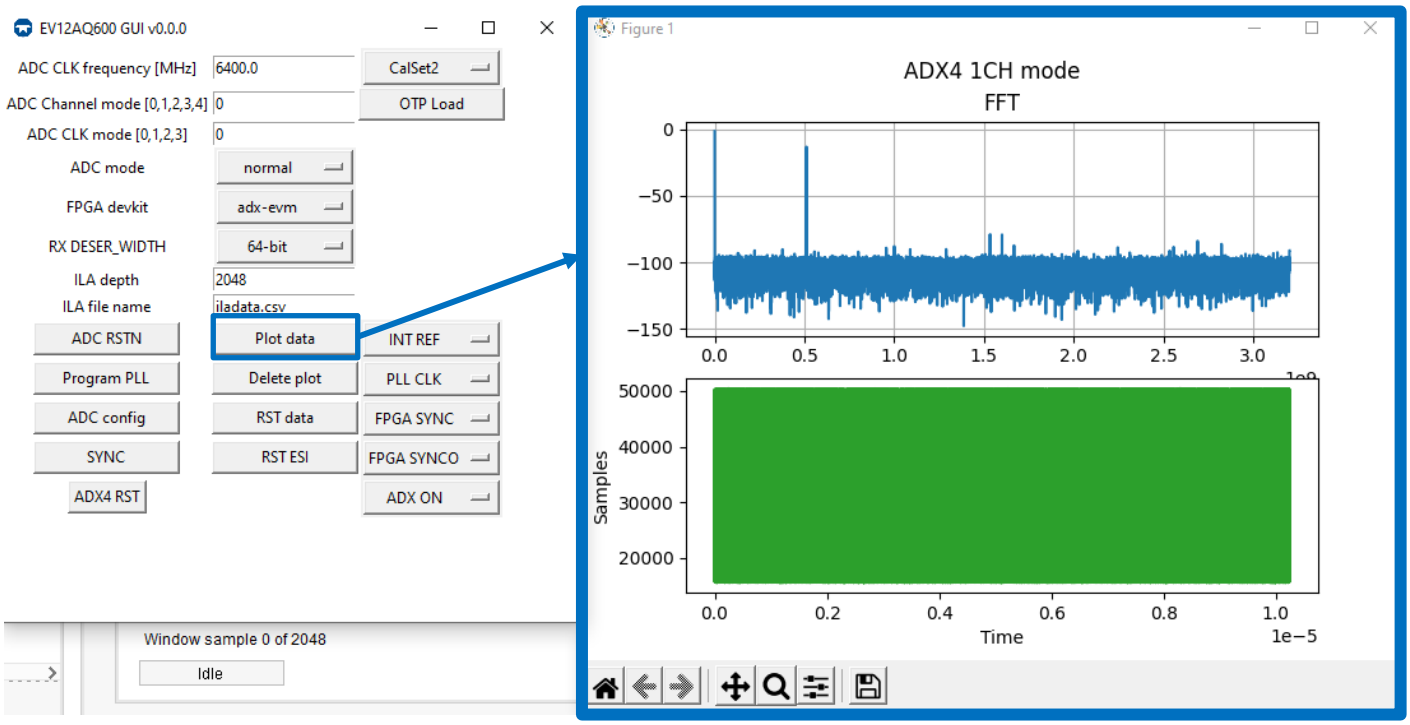


Click ***OK*** again to Export ILA Data in the csv file iladata.csv and on ***Yes*** to confirm overwrite again.



6.3 Display data in the GUI

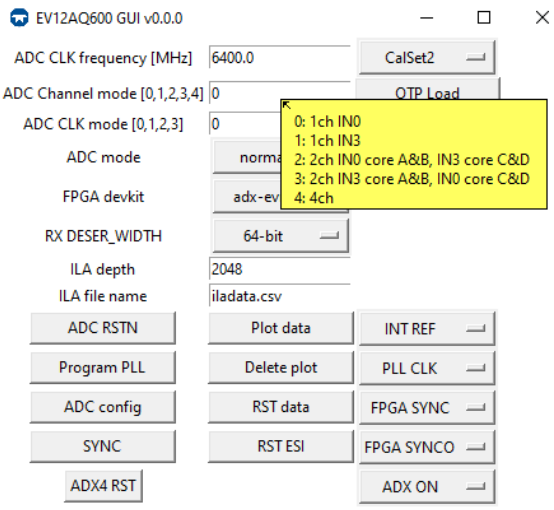
Click on ***Plot data***.

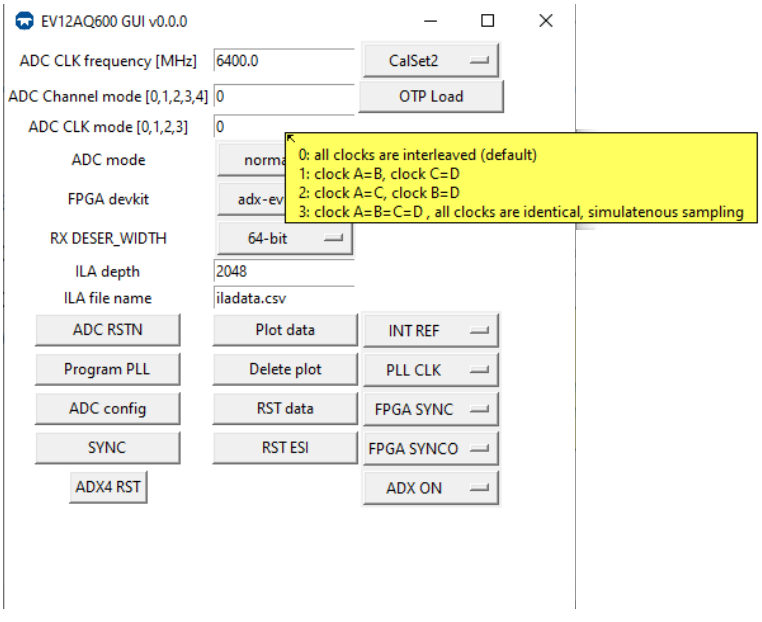


6.4 Configure the ADC in 1ch mode.

The ADX4 IP can be used when the ADC is configured in 1 channel mode.
This is the default configuration when opening the GUI:

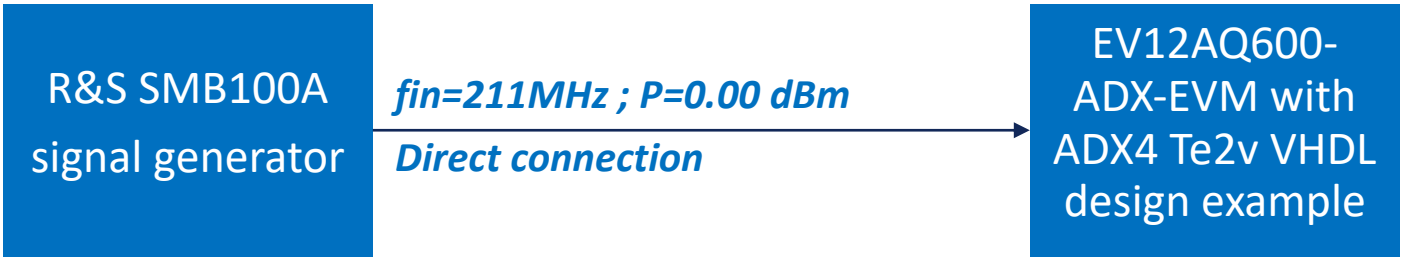
- ***0*** in the field ***ADC Channel mode***: 1ch with signal to acquire on INPUT0
- ***0*** in the field ***ADC CLK mode***: all clocks are interleaved.





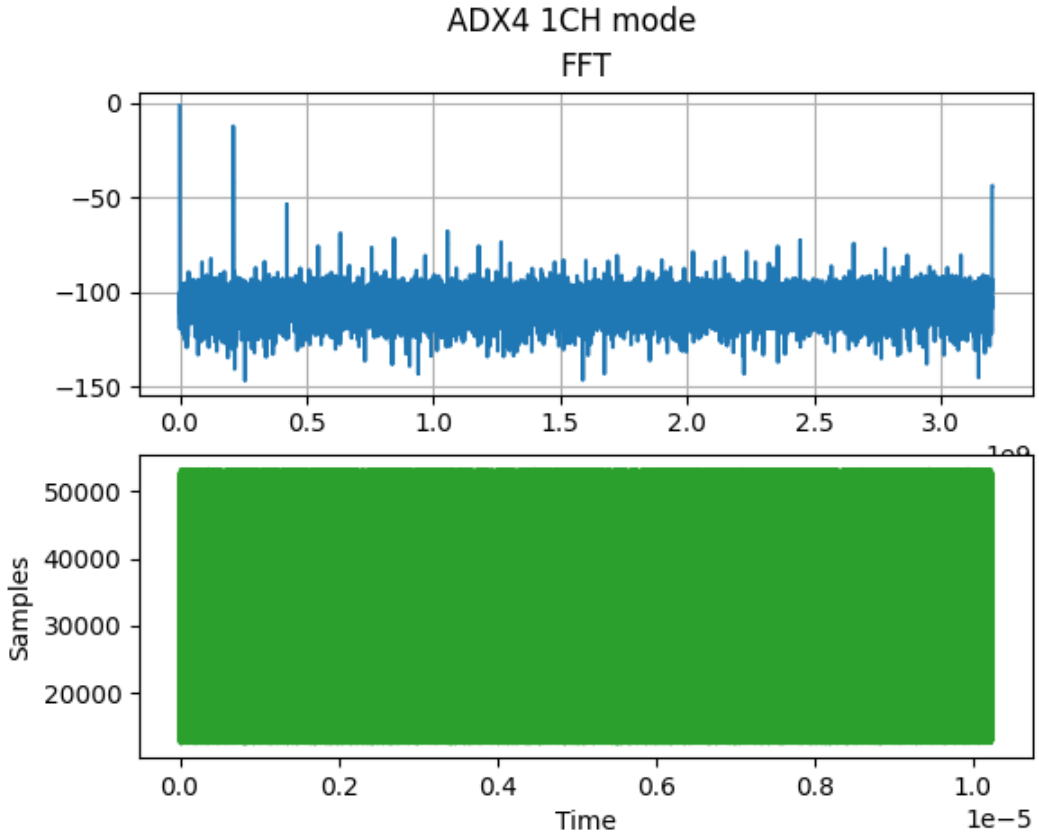
7 Understand the effects of ADC internal calibration and ADX4 IP on ADC performance.

7.1 Setup 1, no filter, fin = 211.000000MHz - overview:



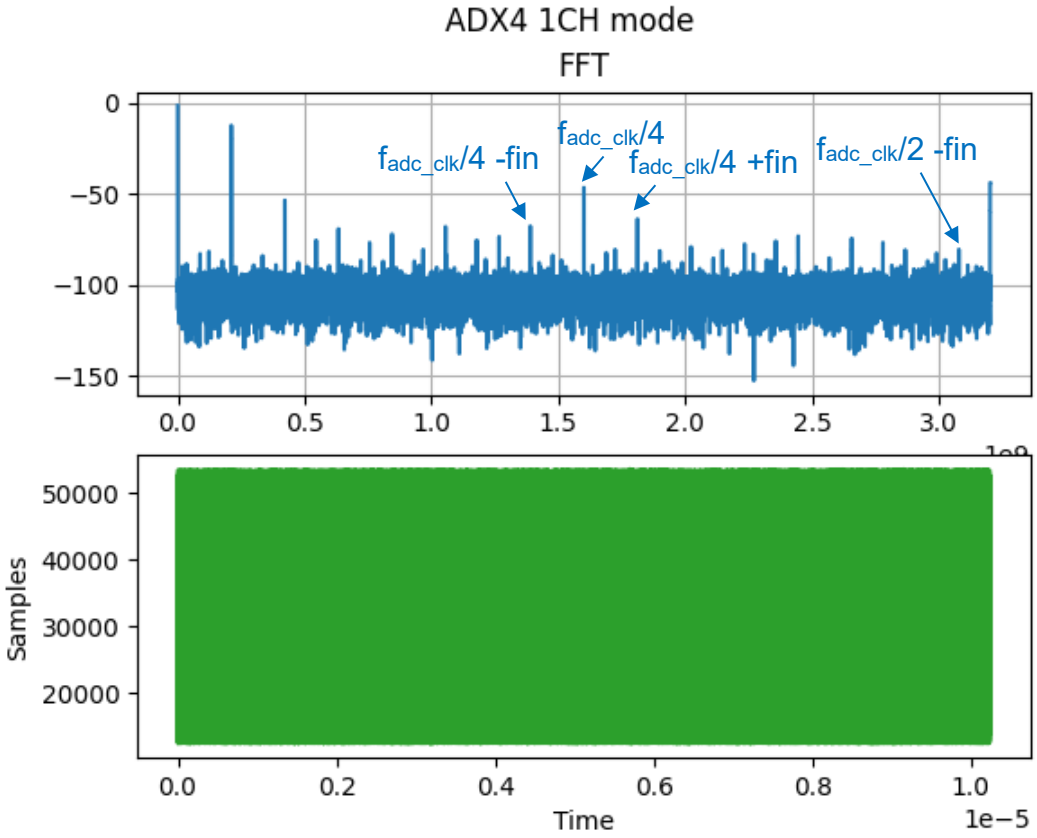
7.2 Setup 1 - ADX ON without OTP LOAD

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet[0:3] depending on input frequency and temperature, are **not loaded**.



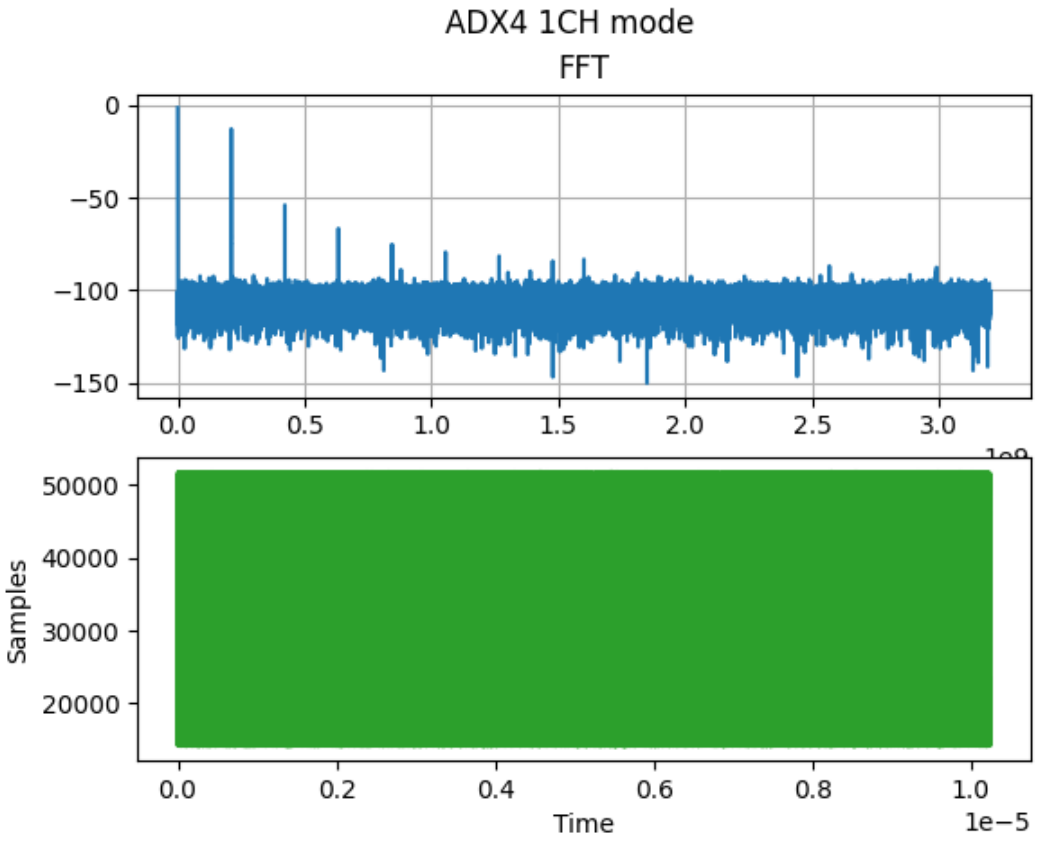
7.3 Setup 1 - ADX BYPASS without OTP LOAD

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet[0:3] depending on input frequency and temperature, are **not loaded**.



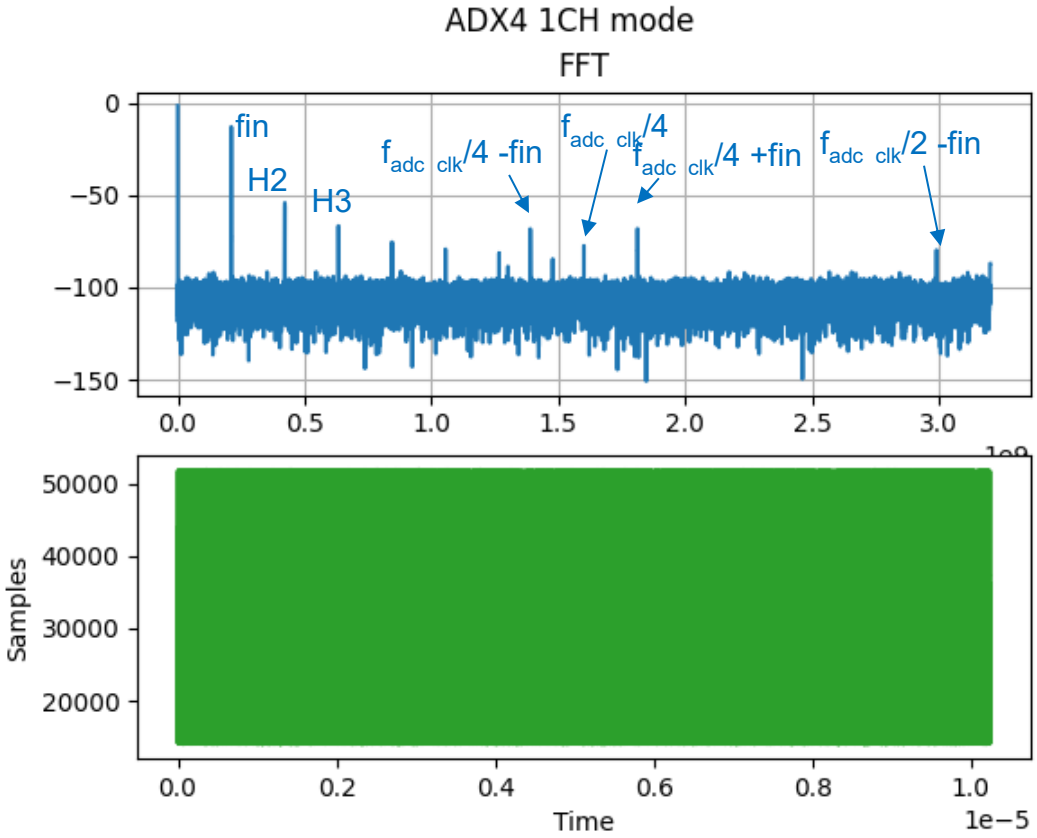
7.4 Setup 1 - ADX ON with OTP LOAD CalSet2

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet2, is **loaded**.

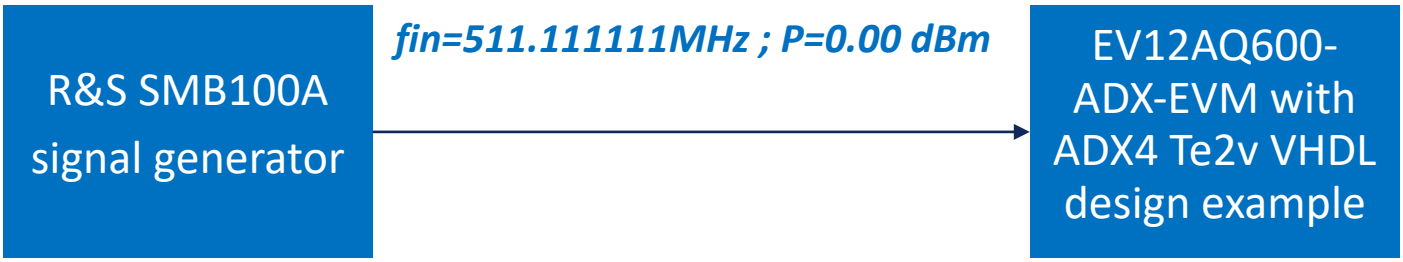


7.5 Setup 1 - ADX BYPASS with OTP LOAD CalSet2

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet2, is **loaded**.

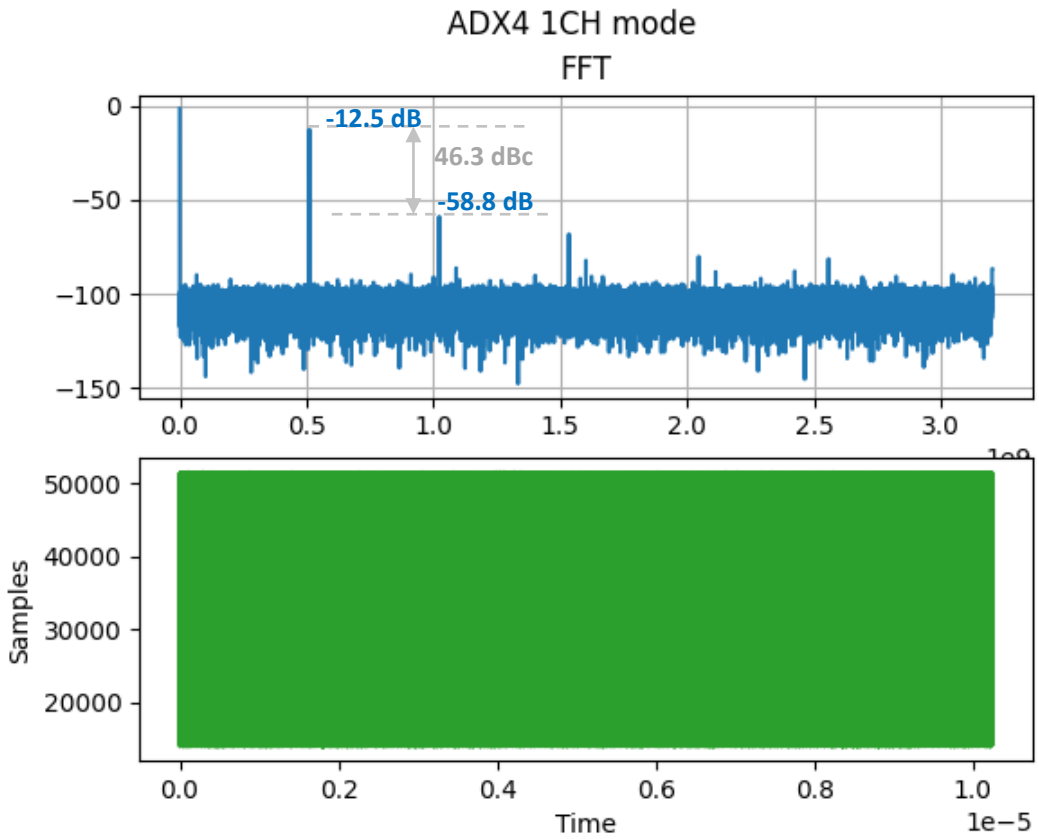


7.6 Setup 2, no filter, fin = 511.111111MHz - overview:

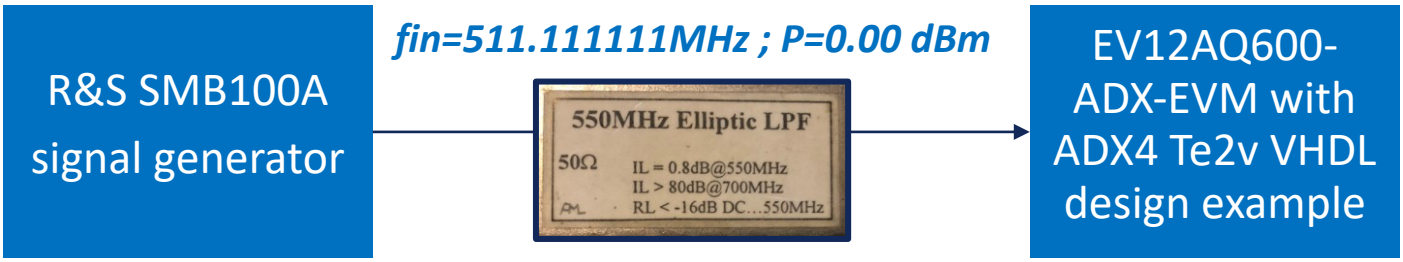


7.7 Setup 2, ADX ON with OTP LOAD

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet2 (fin <800MHz & T~60°C), is **loaded**.

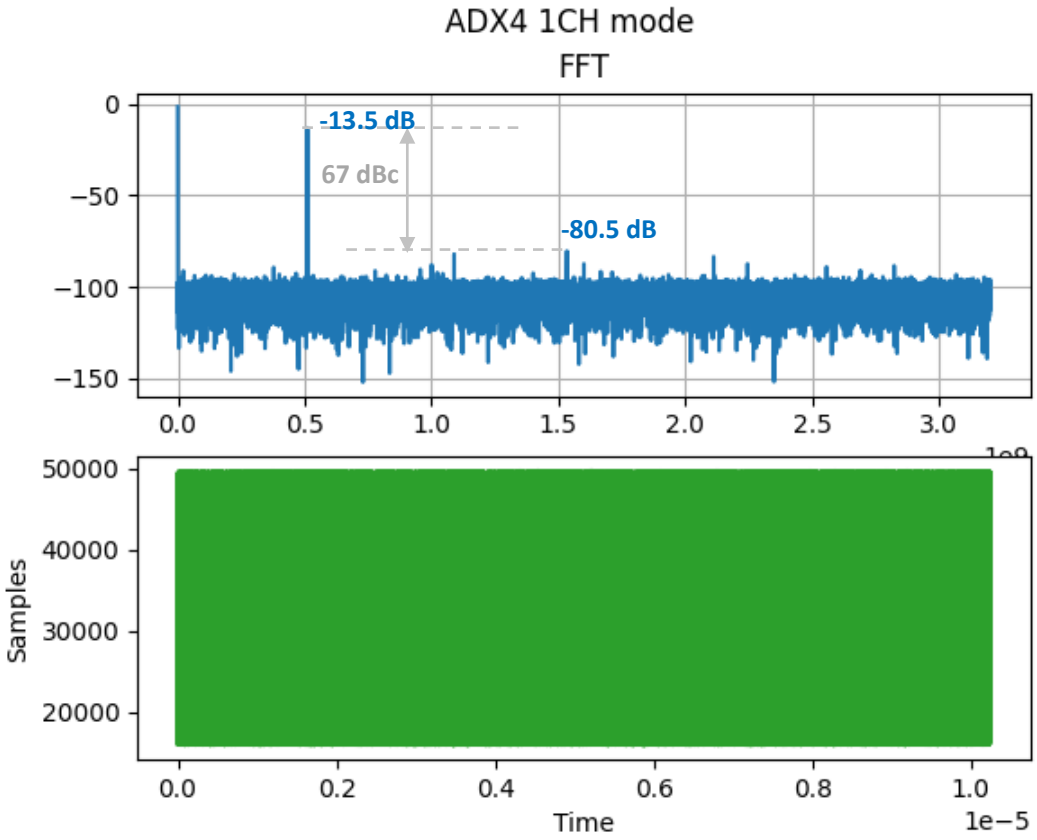


7.8 Setup 3, LPF, fin = 511.111111MHz - overview:



7.9 Setup 3 - ADX ON withOTP LOAD

ADC INL calibration and Gain-Phase-Offset calibration set, CalSet2 (fin <800MHz & T~60°C), is **loaded**.



Conclusion: Hamonics (H2, H3, …) are generated by SMB100A signal generator.