AT84CS001-EB Evaluation Board

User Guide

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Section 1
Introduction

1.1 Scope

The AT84CS001-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the AT84CS001 1:2/4 10-bit 2.2 GHz DMUX up to 2.2 GHz.

The AT84CS001-EB Evaluation Kit includes

- The 1:2/4 10-bit 2.2 GHz DMUX Evaluation Board
- Five SMA caps for DAI, DAIN, DAO, DAON and ASYNCRST signals
- Seven jumpers for the DMUX function settings (RS, BIST, CLKTYPE, DRTYPE, SLEEP, STAGG, DAEN)

This user guide uses the AT84CS001-EB evaluation Kit as an evaluation and demonstration platform and provides guidelines for its correct use.

1.2 Description

The AT84CS001-EB evaluation board is very straightforward as it only implements the AT84CS001 1:2/4 10-bit 2.2 GHz DMUX device, SMA connectors for the standalone delay cell inputs and outputs and for the reset input accesses and 2.54 mm pitch connectors compatible with high-speed acquisition system probes.

This evaluation board is fully compatible with e2v high-speed ADC boards (TSEV830500GL, TSEV8388BGL/GLZA2/F/FZA2, TSEV83102G0BGL and AT84AS008GL-EB).

To achieve optimal performance, the AT84CS001-EB evaluation board was designed in a 4-metal-layer board with RO4003 200 and FR4 HTG dielectric layers. The board implements the following devices:

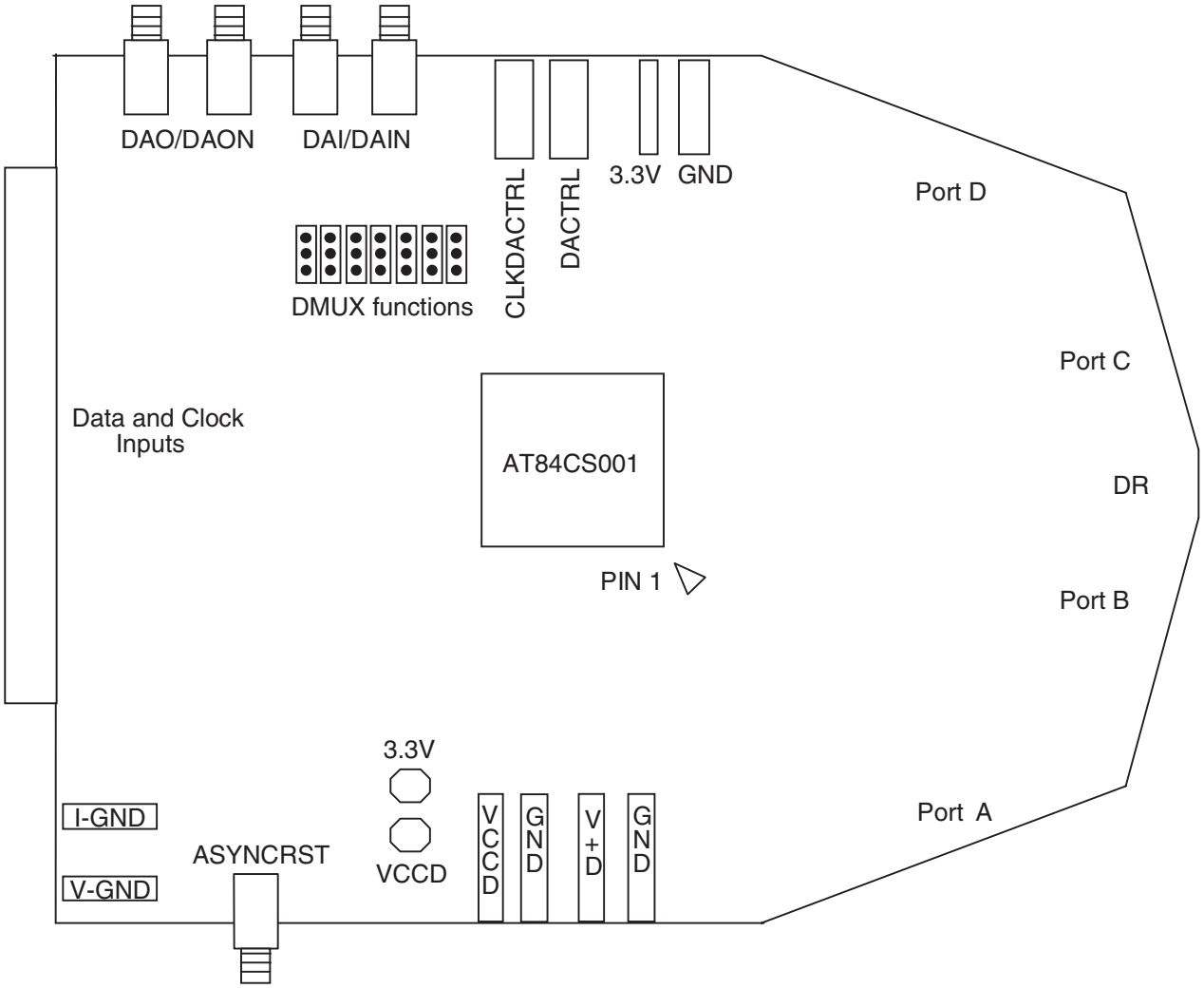
- The 1:2/4 10-bit 2.2 GHz DMUX Evaluation board
- Five SMA caps for DAI, DAIN, DAO, DAON and ASYNCRST signals
- Seven jumpers for the DMUX function settings (RS, BIST, CLKTYPE, DRTYPE, SLEEP, STAGG, DAEN)
- 2.54 mm pitch connectors for the digital inputs and outputs, compatible with high-speed acquisition system probes
- Banana jacks for the power supply accesses
- Potentiometers for the DMUX control functions

The board is comprised of four metal layers for signal traces, ground and power supply layers, and three dielectric layers featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain.

The board dimensions are 220 mm x 230 mm.

The board comes fully assembled and tested, with the AT84CS001 installed.

Figure 1-1. Simplified Schematics of the AT84CS001-EB Evaluation Board



As shown in Figure 1-1, different power supplies are required:

- V_{CCD} = 3.3V digital positive power supply
- V_{PLUSD} = 2.5V digital output power supply
- 3.3V used for the DMUX functions

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Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full-speed operation of the AT84CS001 1:2/4 10-bit 2.2 GHz DMUX, a multi-layer board structure was retained for the evaluation board. Four copper layers are used, respectively dedicated to the signal traces, ground planes and power supply planes.

The board is made in RO4003 200 µm and FR4 HTG epoxy dielectric materials.

The following table gives a detailed description of the board's structure.

Table 2-1. Board Structure

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 µm Input and output signals traces = 50Ω microstrip lines
Layer 2 RO4003 dielectric layer (Hydrocarbon/wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz - 0.044 dB/inch insertion loss at 2.5 GHz - 0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper ground plane = reference plane
Layer 4 FR4 HTG/dielectric layer	Layer thickness = 1050 µm
Layer 5 Copper layer	Copper thickness = 35 µm Power planes = 3.3V, V_{CCD} and V_{PLUSD}
Layer 6 FR4 HTG/dielectric layer	Layer thickness = 200 µm
Layer 7 Copper layer	Copper thickness = 40 µm Lower ground plane = reference plane

The board is 1.6 mm thick.

The digital data input, output and reset signals are located on the top metal layer.

The function signals are located on the top metal layer and layer 7.

The ground planes are located on layer 3 and 7.

Layer 5 is dedicated to the power supplies (3.3V, V_{CCD} and V_{PLUSD}).

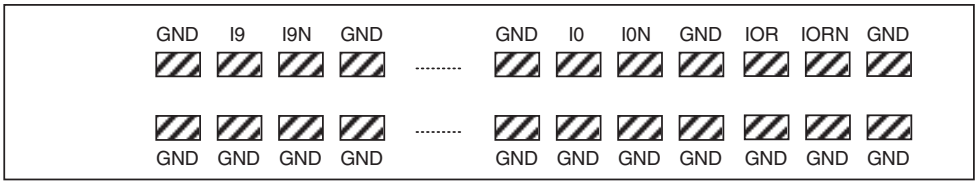
2.2 Data and Clock Input Accesses

Access to the digital data and clock inputs is provided by one female 2.54 mm pitch connector (points) via 50Ω microstrip lines.

The connector is made of two rows:

- The upper row is dedicated to the data and clock signals
- The lower row is connected to ground
- Each differential signal pair is separated by a connection to ground, as illustrated in Figure 2-1

Figure 2-1. Input Data Connector



The input lines are matched (in length) within ±1 mm.
Note: 100Ω termination is provided on-chip.

2.3 Digital Output

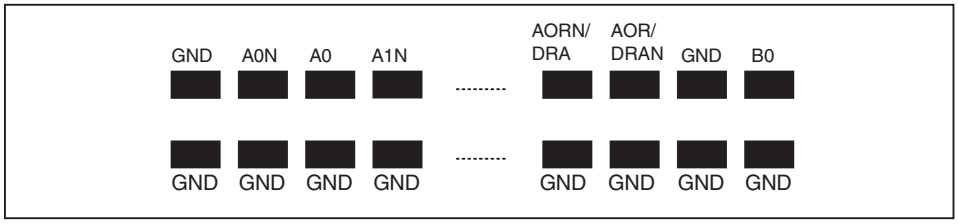
Access to the digital data and clock outputs is provided by four male 2.54 mm pitch connectors (points) via 50Ω microstrip lines.

The connector is made of two rows:

- The upper row is dedicated to the data and clock signals
- The lower row is connected to ground

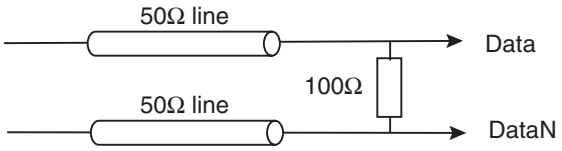
Each output port is separated by a connection to ground, as illustrated in Figure 2-2 on page 2-3.

Figure 2-2. Output Data Connector



The digital outputs are compatible with LVDS standard. They are on-board 100Ω differentially terminated as described in Figure 2-3.

Figure 2-3. Differential Digital Outputs Implementation



The output lines are matched (in length) within ± 5 mm.

2.4 ASYNCRST

Access to the asynchronous reset is provided by both an SMA connector and a push button.

2.5 Standalone Delay Cell

Access to the standalone delay cell inputs (DAI/DAIN) and outputs (DAO/DAON) is provided by SMA connectors via 50Ω microstrip lines.

Note: The 100Ω termination for the DAI/DAIN inputs is provided on-chip, the DAO/DAON outputs are floating (must be terminated by 100Ω termination).

2.6 DMUX Functions

Two potentiometers are provided for the DMUX input clock delay control (CLKDACTRL) and the standalone delay cell control (DACTRL).

Seven jumpers are provided for the RS, BIST, DAEN, SLEEP, STAGG, CLKTYPE and DRTYPE functions (jumper on board = logic 0).

2.7 Power Supplies

Layer 5 is dedicated to power supply planes (3.3V, V_{CCD} and V_{PLUSD}).

The supply traces are low impedance and are surrounded by two ground planes (layers 3 and 7).

V_{CCD} and 3.3V have separated planes but can be short-circuited on the board. The 3.3V supply was separated from V_{CCD} for device power consumption testing purposes.

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply is decoupled as close as possible to the AT84CS001 device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

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Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the AT84CS001 1:2/4 10-bit 2.2 GHz DMUX.

3.2 Operating Procedure

The procedure described below helps you operate the evaluation board for the first time.

It described the steps to accomplish a BIST in order to verify whether the board is functional or not. At the end of the procedure, the DMUX is in the following configuration: BIST, 1:4 ratio, CLKTYPE = CLK/2, DRTYPE = DR/2, simultaneous mode, no SLEEP.

Note: Do not switch the power supplies until all power connections on the evaluation board are established.

1. Connect the power supplies and ground accesses through the dedicated banana jacks. V_{CCD} = 3.3V, V_{PLUSD} = 2.5V and 3.3V.
2. Connect the clock input signals (CLK, CLKN). This clock may be single-ended or differential. Use a low-phase noise high frequency generator. You should use an LVDS signal to drive the input clock.
   In single-ended mode, CLK must have a common mode voltage equal to 1.25V and CLKN should be connected to a constant value equal to 1.25V. For a differential signal use an LVDS buffer. The clock frequency can range from 1 MHz up to 1.1 GHz (CLK/2 mode) or 2.2 GHz (CLK mode).
3. Remove the jumpers on CLKTYPE, DRTYPE, RS, DAEN, SLEEP and STAGG. The only remaining jumper is on BIST.
4. Connect the high-speed acquisition system probes to the output connectors.

The digital data are differentially terminated on-board (100Ω) but, they can be probed either in differential or in single-ended mode.

All instrumentation and connectors are now connected.

5. Switch on the power supplies (recommended power up sequence: simultaneous or in the following order: V_{CCD} = 3.3V, V_{PLUSD} = 2.5V and 3.3V).

6. Turn on the RF clock generator
7. Perform an asynchronous reset (ASYNCRST push button) on the device.

The AT84CS001-EB evaluation board is now ready for operation in BIST mode.

Note: The BIST comprises a 10-bit sequence available on all four ports of the device (sets the AT84CS001 in 1:4 mode).

The sequence is as follows:

Cycle 0:
Port A = 1010101010
Port B = 1010101010
Port C = 0101010101
Port D = 1010101010

Cycle 1:
Port A = 0101010101
Port B = 0101010101
Port C = 1010101010
Port D = 0101010101

3.3 Electrical Characteristics

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Digital power supply	V_{CCD}	3.6	V
Output power supply	V_{PLUSD}	3.6	V
Data input	I0, I0N…I9, I9N IOR,IORN DAI, DAIN	-0.3 to V_{CCD} + 0.3	V
Clock input	VCLK,VCLKN	-0.3 to V_{CCD} + 0.3	V
Control inputs	SLEEP, STAGG, ASYNCRST, BIST, RS, DAEN, CLKTYPE, DRTYPE, CLKDACTRL, DACTRL	-0.3 to V_{CCD} + 0.3	V
Maximum junction temperature	TJ	125	°C
Storage temperature	Tstg	-65 to 150	°C
Ball temperature	Tballs	300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended	Unit
Positive supply voltage	V_{CCD}		3.3	V
Positive digital supply voltage	V_{PLUSD}		2.5	V
DMUX Control Voltage		CLKDACTRL, DACTRL	$V_{CCD}/3$ to $2 \times V_{CCD}/3$	V
Operating Temperature Range		Industrial “V” grade	-40°C < T_C; T_J < 110°C	°C

Table 3-3. Electrical Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Resolution		10-bit with additional 11th bit			Bit
Power Requirements					
Digital power supply voltage	V_{CCD}	3.15	3.3	3.45	V
Output power supply voltage	V_{PLUSD}	2.375	2.5	2.625	V
Digital power supply current - 1:2 mode - 1:4 mode - SLEEP mode - Additional current with SDA enabled - Additional current with BIST enabled	I_{VCCD}		 520 580 170 25 40	 610(3) 680(3) 200(3)	mA
Output power supply current - 1:2 mode - 1:4 mode	I_{VPLUSD}		 250 280	 350(3) 380(3)	mA
Power dissipation - 1:2 mode - 1:4 mode - SLEEP mode (1:4) - All active (1:4, BIST & SDA enabled)	P_D		 2.4 2.6 1.3 2.8	 3.0(3) 3.3(3) 3.5(3)	W
LVDS Data/Clock Inputs and Outputs					
Logic Compatibility		LVDS			
Input Common Mode(1)	V_{ICM}	1	1.25	1.6	V
Output Common Mode(2)	V_{OCM}	1.125	1.25	1.375	V
Differential input(1)	V_{IDIFF}	100	350	-	mV
Differential output	V_{ODIFF}	250	350	500	mV
Output level "High"	V_{OH}	1.25	1.425	-	V
Output level "Low"	V_{OL}	-	1.075	1.25	V

Table 3-3. Electrical Operating Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Static Inputs (SLEEP, STAGG, BIST, RS, DAEN, CLKTYPE, DRTYPE)					
Control Input Voltages : - Logic low - Logic high	 R_{IL} V_{IL} R_{IH} V_{IL}	 0 10k 2.0V		 10 0.5V Infinite	 Ω
Static Inputs (CLKDACTRL, DACTRL)					
Control input voltages		$V_{CCD}/3$		$2 \times V_{CCD}/3$	V
Reset input (ASYNCRST)					
Logic compatibility			LVCMOS/CMOS		
Control input voltages: - Logic low - Logic high - Common mode	 V_{IL} V_{IH} V_{ICM}	 0 1.5	 1.4	 1.2 3.3	V

Notes: 1. Given for a differential input
2. Given for a 100Ω termination across true/false signals
3. Worst case value obtained with maximum supply voltages over full temperature range

Table 3-4. Switching Performance and Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Clock					
Maximum clock frequency	Fs max	1		1500	MHz
Minimum clock pulse width (high)	TC1	0.3	0.333	500	ns
Minimum clock pulse width (low)	TC2	0.3	0.333	500	ns
Output rise/fall time for data (20% - 80%)	TR/TF			400	ps
Output rise/fall time for Data Ready (20% - 80%)	TR/TF			400	ps
Data output delay	TOD		400		ps
Data Ready output delay	TDR		400		ps
	|TOD - TDR|		0		ps

Table 3-4. Switching Performance and Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Output data to Data Ready propagation delay	TD1	0.3	0.333	500	ps
Data Ready to output data propagation delay	TD2	0.3	0.333	500	ps
Output data pipeline delay: - Synchronized 1:2 mode - Synchronized 1:4 mode - Staggered 1:2 mode - Staggered 1:4 mode	TPD		0.5 1.5 0 / 0.5 0 / 0.5 / 1 / 1.5		Clock cycles

Note: Please refer to the device datasheet entitled “AT84CS001”, reference 0809.

Section 4

Application Information

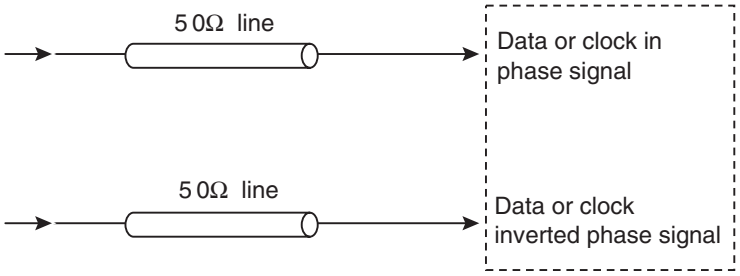
4.1 Introduction

For this section, please also refer to the “Main features” section in the”AT84CS001” reference 0809.

4.2 Input Data

The input data (I0, I0N…I9, I9N and IOR, IORN) and clock (CLK, CLKN) as well as the DAI, DAIN input data of the standalone delay cell are LVDS compatible (on-chip 100Ω).

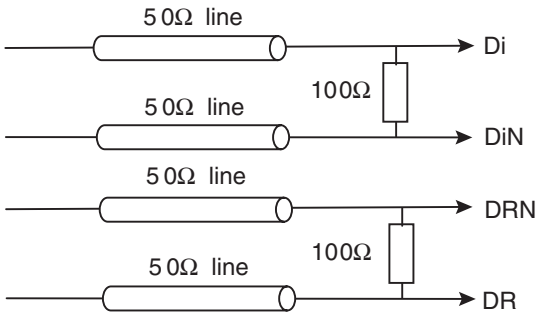
Figure 4-1. Input Data and Clock Signals



4.3 Digital Outputs

The digital outputs (data and Data Ready) are LVDS compatible. The 100Ω differential termination is provided on-board.

Figure 4-2. Implementation of Differential Digital Outputs



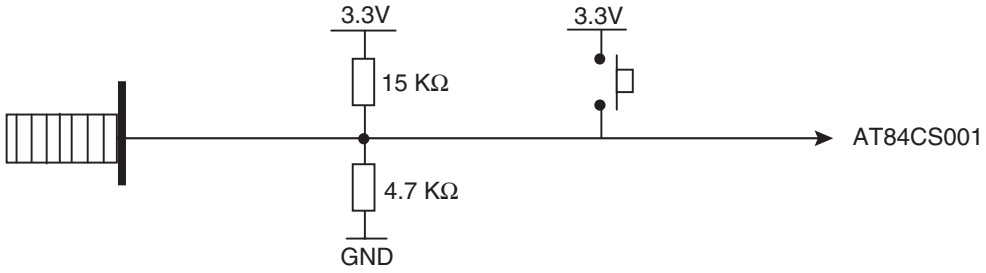
4.4 DMUX Functions

4.4.1 ASYNCRST

The asynchronous reset is mandatory to start the device properly. It must be applied after power up of the device and after any change of DMUX function.

A push button is provided to perform this reset and pull-up and pull-down resistors maintain the ASYNCRST signal in inactive mode.

Figure 4-3. ASYNCRST Function



If the DRRB reset is also used, we recommend to apply the asynchronous reset while the DRRB reset is active.

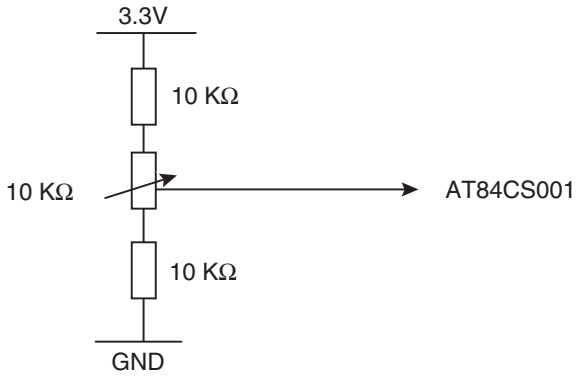
The first data is available at the device output after TOD + 7.5 cycles.

4.4.2 CLKDACTRL

A delay cell is provided to allow you to tune the delay between the clock and data at the DMUX input. The delay is controlled via the CLKDACTRL potentiometer.

This cell allows you to delay the internal DMUX clock by approximately 250 ps via the CLKDACTRL potentiometer (varying from $V_{CCD}/3$ to $(2 \times V_{CCD})/3$).

Figure 4-4. CLKDACTRL Function



4.4.3 DACTRL

A standalone delay cell is available (input = DAI/DAIN, output = DAO/DAON, control = DACTRL, enable = DAEN). This cell allows you to delay the incoming signal DAI/DAIN by approximately 250 ps via the DACTRL potentiometer (varying from $V_{CCD}/3$ to $(2 \times (V_{CCD})/3)$.

4.4.4 RS, DRTYPE, DAEN, BIST, CLKTYPE, SLEEP, STAGG

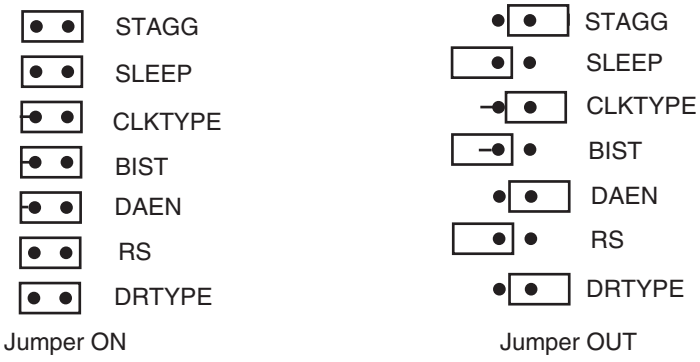
Seven jumpers are provided for the RS, DRTYPE, DAEN, BIST, CLKTYPE, SLEEP and STAGG functions. The following table describes each of these functions.

Table 4-1. Settings and Description of each DMUX Function

Function	Description	Jumper Settings
BIST	Built-In Self Test: - Active: checker-board pattern available at the device's output - Inactive: normal mode	BIST: jumper ON No BIST: jumper OUT
CLKTYPE	Input clock mode: - CLK= data valid on each rising edge of the CLK/CLKN signal - CLK/2 = data valid on both rising and falling edges of the CLK/CLKN signal	CLK: jumper ON CLK/2: jumper OUT
DAEN	Standalone Delay Cell Enable - DAEN active: DAI/DAIN delay can be controlled via DACTRL and output in DAO/DAON - DAEN inactive: the standalone delay cell cannot be used	DAEN active : jumper ON DAEN inactive: jumper OUT
DRTYPE	Output clock mode: - DR/2 = data valid on both rising and falling edges of the DR/DRN signal - DR = data valid on each rising edge of the DR/DRN signal	DR/2: jumper ON DR: jumper OUT
RS	Ratio selection: - 1:2 - 1:4	Jumper ON Jumper OUT
SLEEP	Sleep mode: - Active: the device is in a partial standby mode - Inactive: normal mode	SLEEP: jumper ON Inactive: jumper OUT
STAGG	Simultaneous or staggered output mode: - STAGG acitve: staggered output data - Inactive: simultaneous output data	STAGG: jumper ON Inactive: jumper OUT

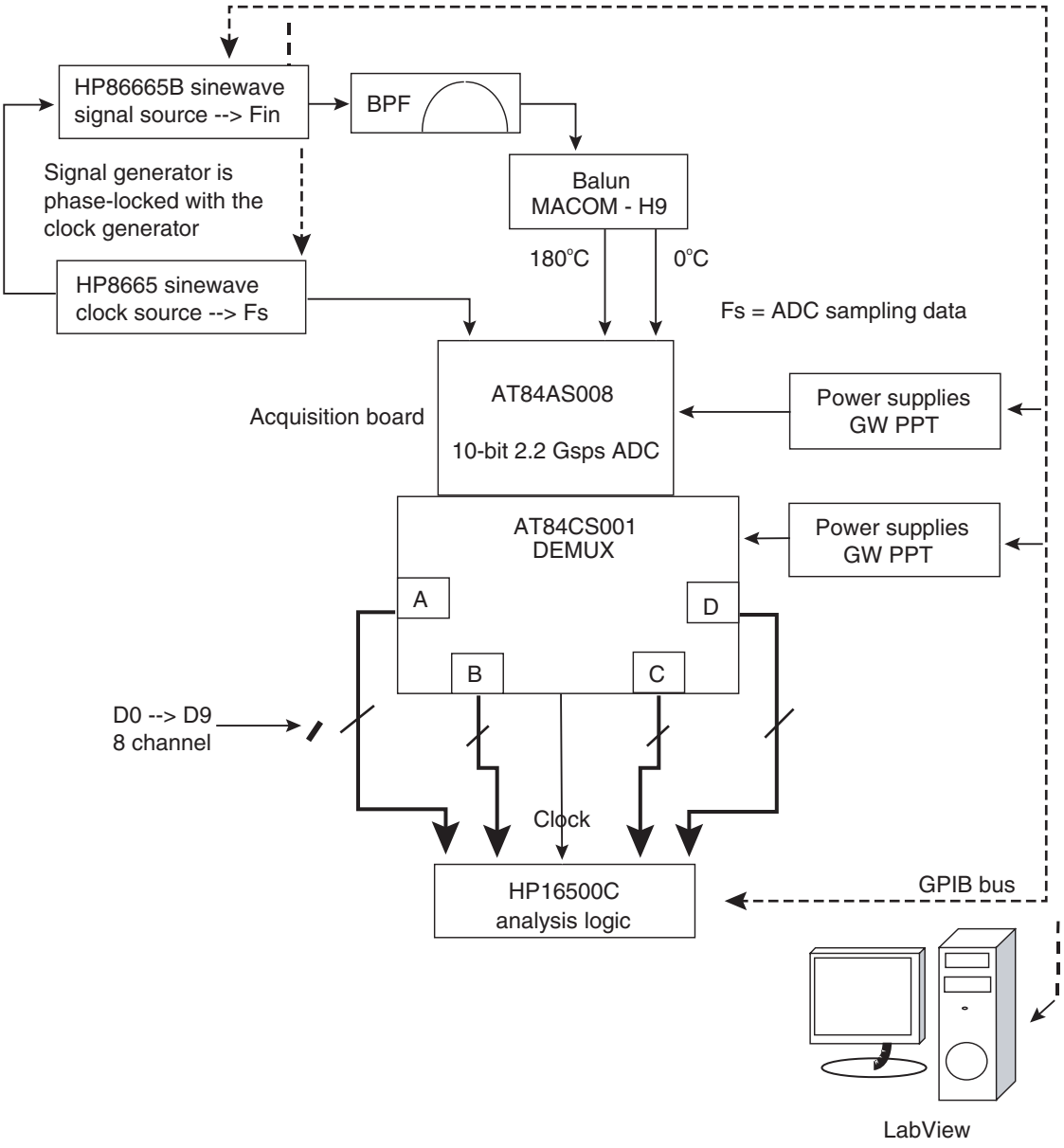
Note: The BIST is comprised of a 10-bit sequence available on all four ports of the device (sets the AT84CS001 in 1:4 mode). The sequence is as follows:
Cycle 0:
Port A = 1010101010
Port B = 1010101010
Port C = 0101010101
Port D = 1010101010
Cycle 1:
Port A = 0101010101
Port B = 0101010101
Port C = 1010101010
Port D = 0101010101

Figure 4-5. Jumper Positions of DMUX Functions



4.5 Test bench Description

Figure 4-6. Test Bench Schematics



Section 5

Package Information

5.1 AT84CS001 Pinout (Bottom View)

Figure 5-1. AT84CSO01 Pinout

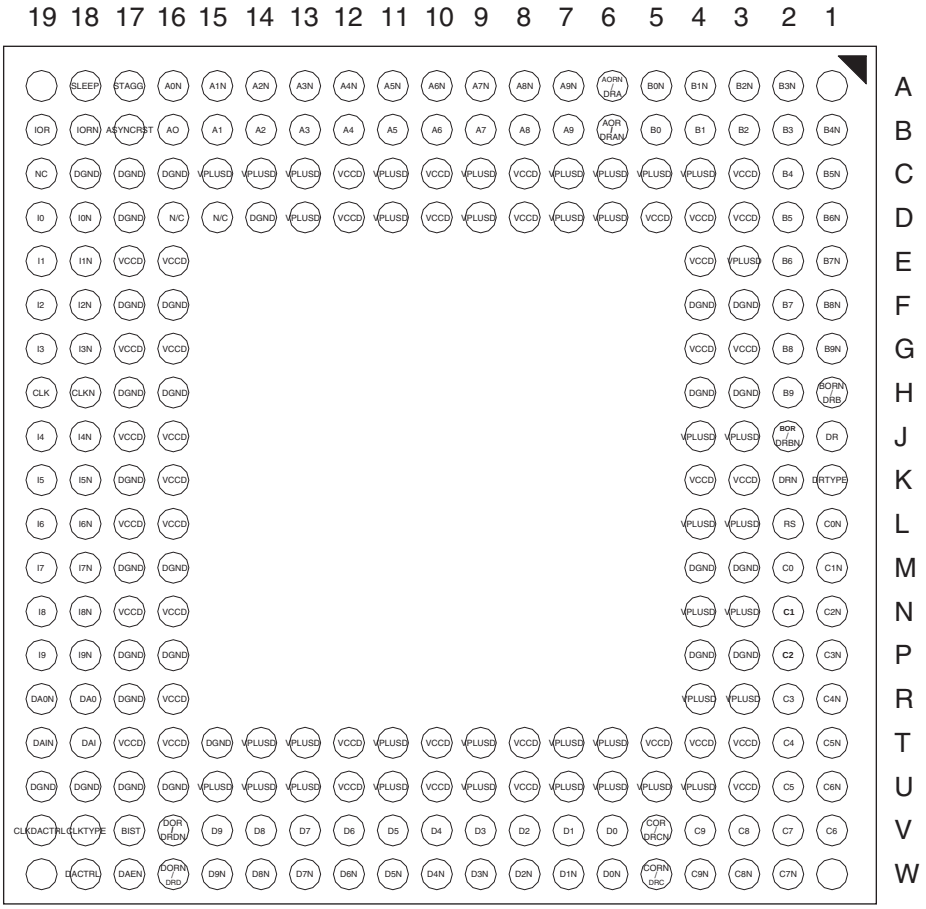


Table 5-1. ASTS8CSO01 Pinout Description

Symbol	Pin Number	Function
Power Supply		
V_{CCD}	C12, C10, C8, C3, D12, D10, D8, D5, D4, D3, E17, E16, E4, G17, G16, G4, G3, J17, J16, K16, K4, K3, L17, L16, N17, N16, R16, T17, T16, T12, T10, T8, T5, T4, T3, U12, U10, U8, U3	Digital 3.3V supply
V_{PLUSD}	C15, C14, C13, C11 C9, C7, C6, C5, C4, D13, D11, D9, D7, D6, E3, J4, J3, L4, L3, N4, N3, R4, R3, T14, T13, T11, T9, T7, T6, U15, U14, 13, U11, U9, U7, U6, U5, U4	Output 2.5V supply
DGND	C18, C17, C16, D17, D14, F17, F16, F4, F3, H17, H16, H4, H3, K17, M17, M16, M4, M3, P17, P16, P4, P3, R17, T15, U19, U18, U17, U16	Ground
Digital inputs		
I0, I1, I2, I3, I4, I5, I6, I7, I8, I9	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19	In-phase (+) digital input signal
I0N, I1N, I2N, I3N, I4N, I5N, I6N, I7N, I8N, I9N	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18	Inverted phase (-) digital input signal
IORN	B18	Inverted phase (-) digital input signal for additional bit
IOR	B19	In-phase (+) digital input signal additional bit
DAI	T18	In-phase (+) input signal for standalone delay cell
DAIN	T19	Inverted phase (-) input signal for standalone delay cell
Clock inputs		
CLK	H19	In-phase (+) clock input
CLKN	H18	Inverted phase (-) clock input
Digital inputs		
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-phase (+) digital outputs for port A A0 is the LSB, A9 is the MSB
A0N, A1N, A2N, A3N, A4N, A5N, A6N, A7N, A8N, A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted phase (-) digital outputs for port A
AOR/DRAN	B6	In-phase (+) additional bit output for port A or inverted phase (-) output clock for port A in staggered mode
AORN/DRA	A6	Inverted phase (-) additional bit output for port A or In-phase (+) output clock for port A in staggered mode
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-phase (+) digital outputs for port B B0 is the LSB, B9 is the MSB

Table 5-1. ASTS8CSO01 Pinout Description (Continued)

Symbol	Pin Number	Function
B0N, B1N, B2N, B3N, B4N, B5N, B6N, B7N, B8N, B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted phase (-) digital outputs for Port B
BOR/DRBN	J2	In-phase (+) additional bit output for port B or inverted phase (-) output clock for port B in staggered mode
BORN/DRB	H1	Inverted phase (-) additional bit output for port B or In-phase (+) output clock for port B in staggered mode
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9	M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	In-phase (+) digital outputs for port C C0 is the LSB, C9 is the MSB
C0N, C1N, C2N, C3N, C4N, C5N, C6N, C7N, C8N, C9N	L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	Inverted phase (-) digital outputs for Port C
COR/DRCN	V5	In-phase (+) additional bit output for port C or inverted phase (-) output clock for port C in staggered mode
CORN/DRC	W5	Inverted phase (-) additional bit output for port C or In-phase (+) output clock for port C in staggered mode
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-phase (+) digital outputs for port D D0 is the LSB, D9 is the MSB
D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted phase (-) digital outputs for Port D
DOR/DRDN	V16	In-phase (+) additional bit output for port D or inverted phase (-) output clock for port D in staggered mode
DORN/DRD	W16	Inverted phase (-) additional bit output for port D or In-phase (+) output clock for port D in staggered mode
DR	J1	In-phase (+) Data Ready signal output
DRN	K2	Inverted phase (-) Data Ready signal output
DAO	R18	In-phase (+) output signal for standalone delay cell
DAON	R19	Inverted phase (-) output signal for standalone delay cell
Additional Functions		
ASYNCRST	B17	Asynchronous reset signal
CLKTYPE	V18	Input clock type Selection signal
DRTYPE	K1	Output clock type Selection signal
CLKDACTRL	V19	Clock delay cell control signal
DACTRL	W18	Standalone delay cell control signal
DAEN	W17	Standalone delay cell enable signal
RS	L2	Ratio selection signal
SLEEP	A18	Sleep Mode Selection signal

Table 5-1. ASTS8CSO01 Pinout Description (Continued)

Symbol	Pin Number	Function
STAGG	A17	Staggered output mode selection signal
BIST	V17	Built-In Self Test selection signal
NC	C19	Leave floating

5.2 Package Outline

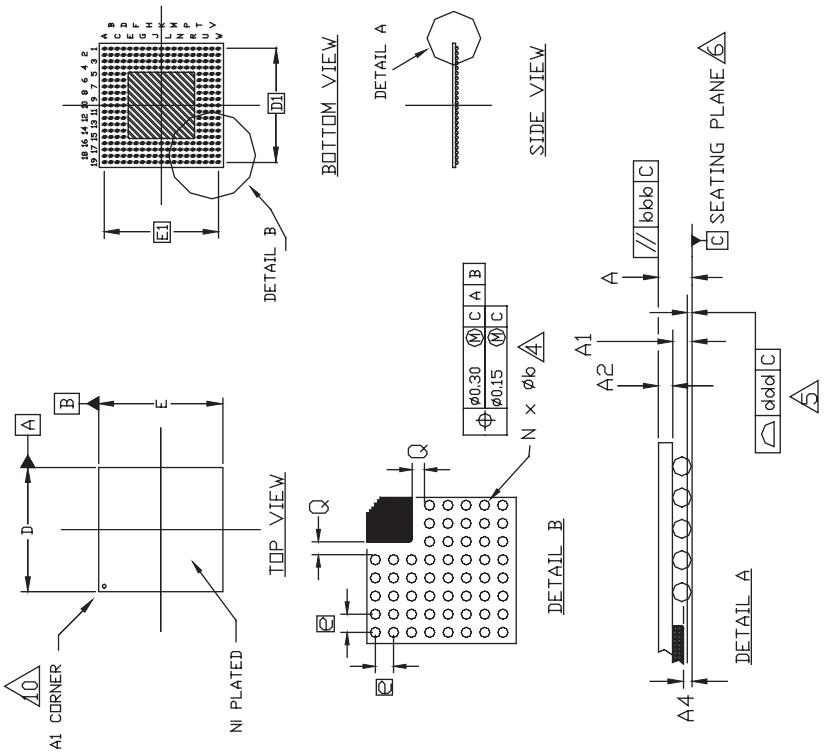
Figure 5-2. Package Outline Schematics

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	24.80	25.00	25.20
D1		22.86 (BSC.)	
E	24.80	25.00	25.20
E1		22.86 (BSC.)	
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M		19	
N		240	
bbb			0.25
ddd			0.20
e		1.27 TYP.	
A4	0.15		
Q	0.35		

REF: JEDEC MS-034B VARIATION BAK-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL 'N' IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
5. DIMENSION 'ddd' IS MEASURED PARALLEL TO PRIMARY DATUM C. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE NI PLATED.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. BLACK SPOT FOR PIN 1 IDENTIFICATION.
10. 'A4' IS MEASURED AT THE EDGE OF ENCAPSULANT TO THE INNER EDGE OF BALL PAD.
11. DIMENSIONING AND TOLERANCING PER ASME Y14.5 1994
12. THIS DRAWING IS FOR QUALIFICATION PURPOSE ONLY.



e2v

Section 6

Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84XCS001TP	EBGA 240	Ambient	Prototype	Please contact your local sales office
AT84CS001VTP	EBGA 240	Industrial "V" grade -40°C < T_C; T_J < 110°C	Standard	
AT84CS001VTPY	EBGA240 RoHS	Industrial “V” grade -40°C < T_C; T_J < 110°C	Standard	
AT84CS001TP-EB	EBGA 240	Ambient	Prototype	Evaluation Kit

Section 7

Appendix

7.1 AT84CS001-EB Electrical Schematics

Figure 7-1. Data I/O Electrical Schematic

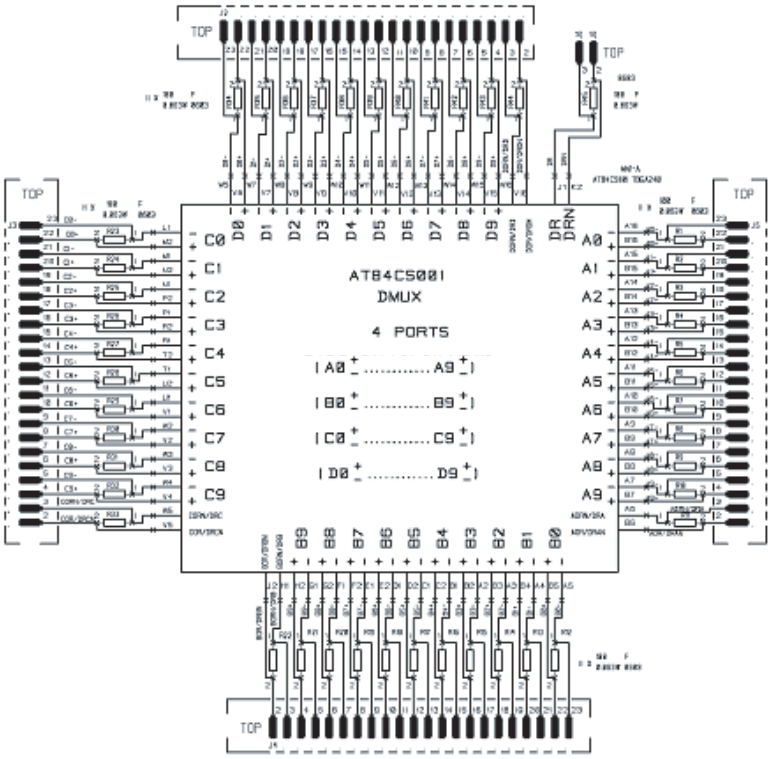


Figure 7-2. Data I/O Electrical Schematic [2]

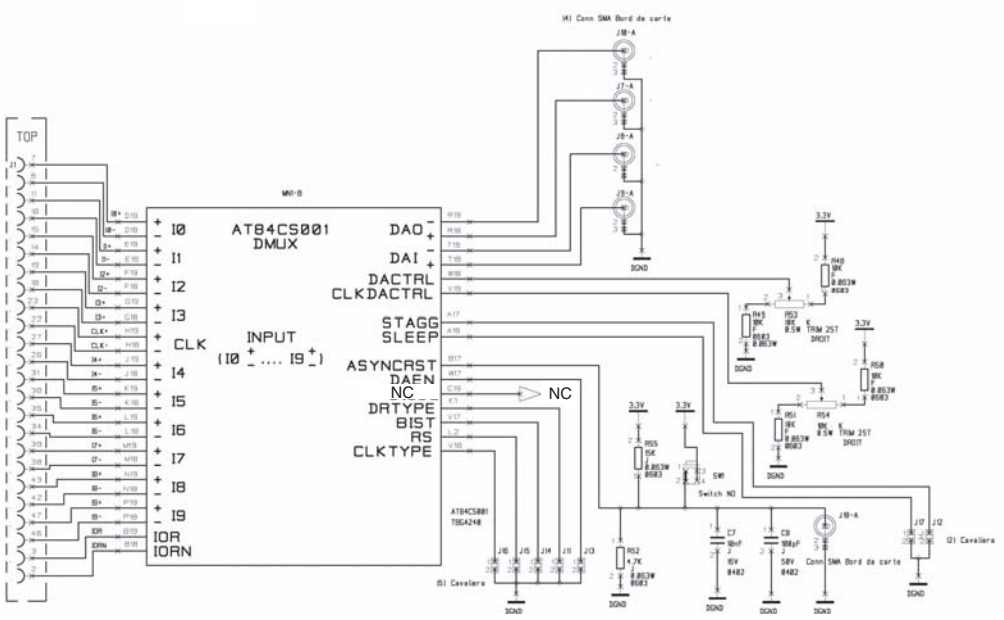


Figure 7-3. Electrical Schematic of Power Supplies [1]

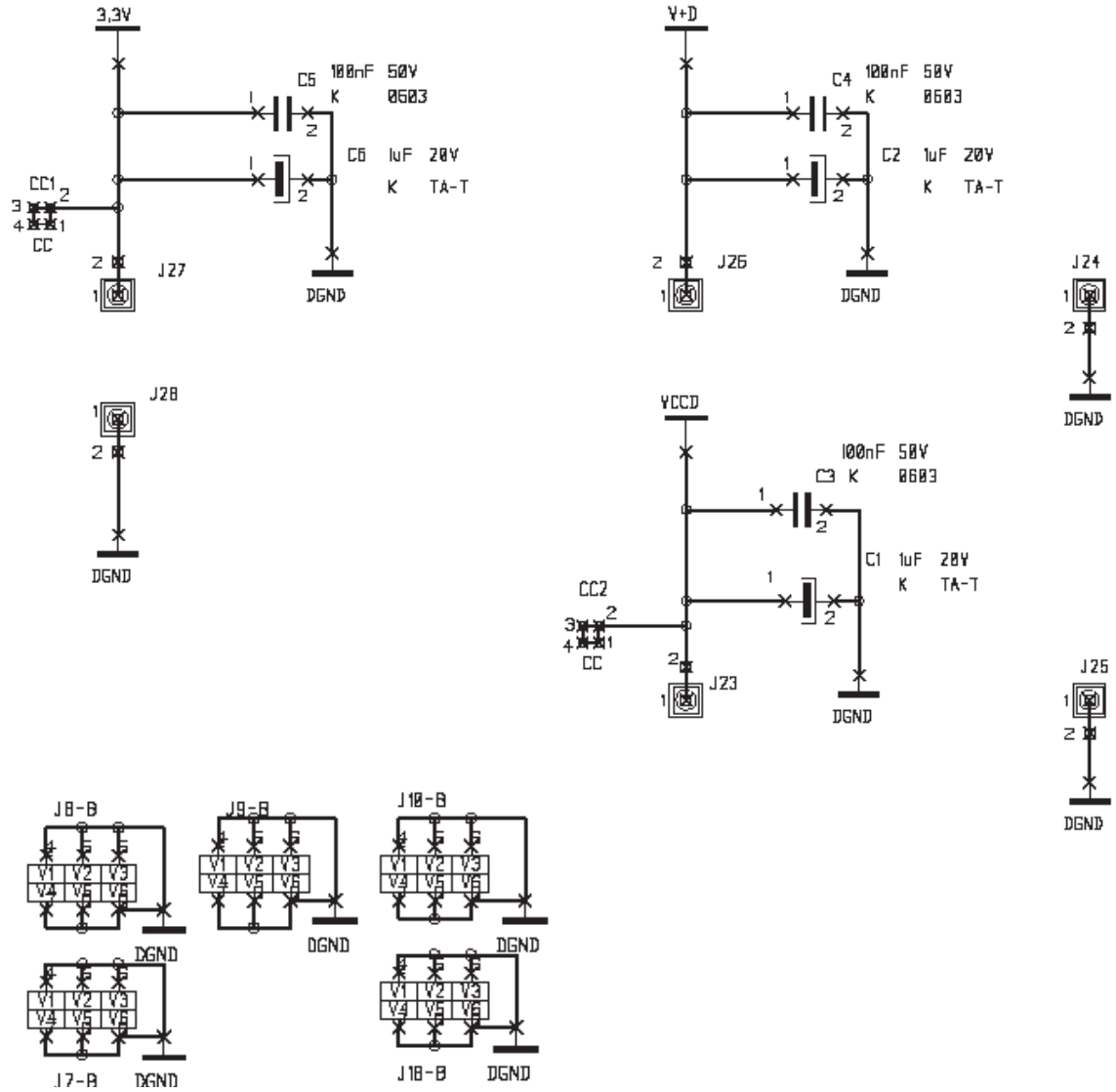


Figure 7-4. Electrical Schematic of Power Supplies [2]

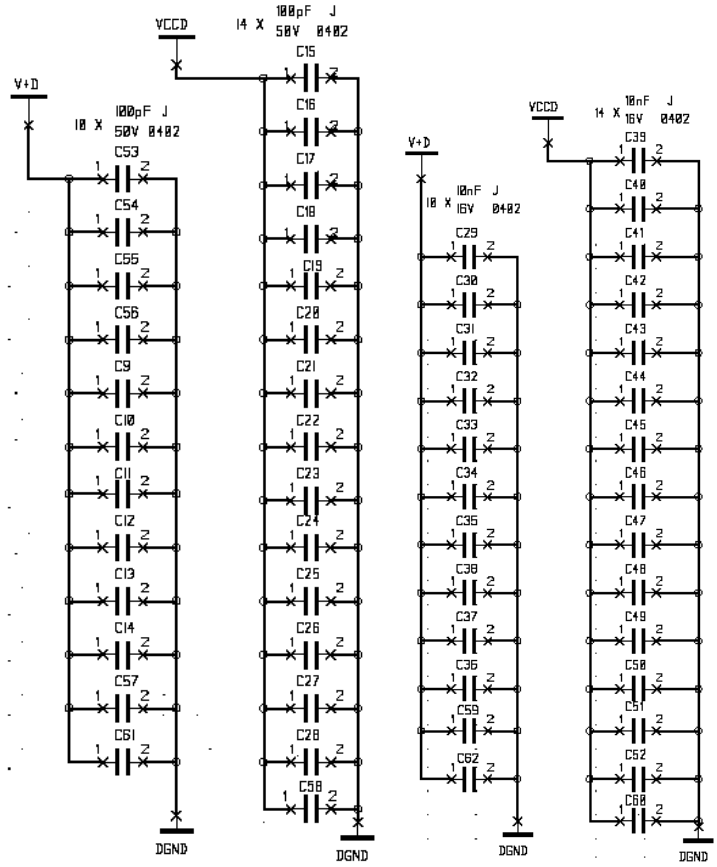
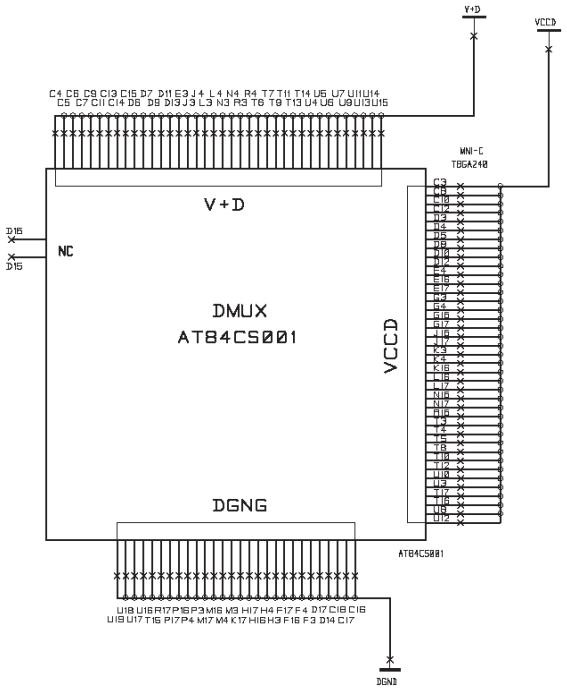


Figure 7-5. Electrical Schematic of Power Supplies [3]



7.2 AT84CS001-EB Board Layers

Figure 7-6. Top Layer

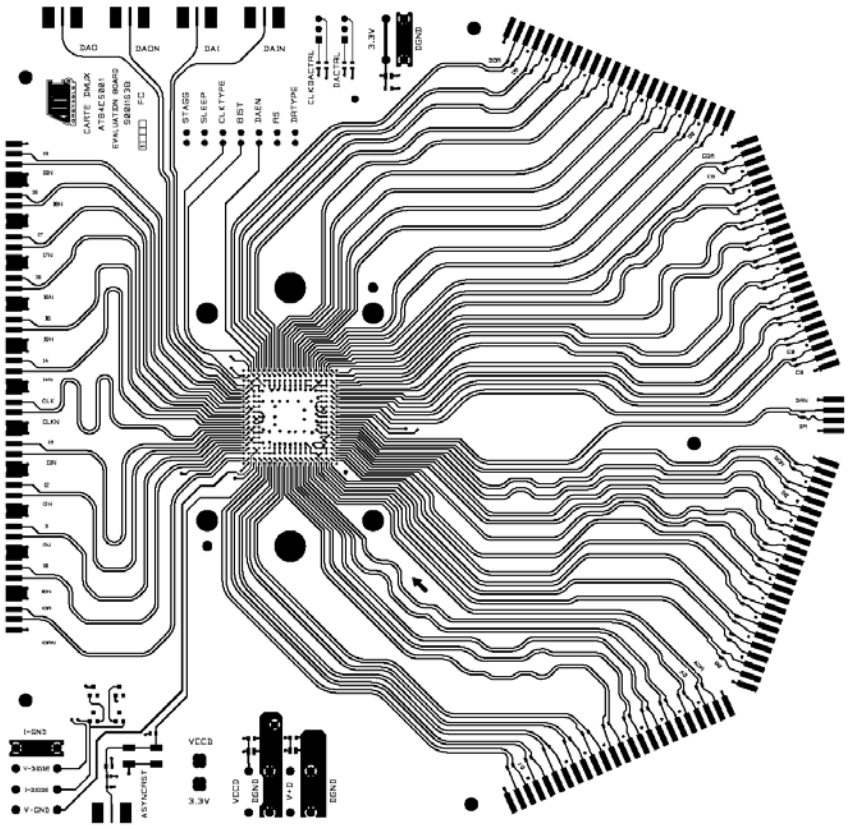


Figure 7-7. Bottom Layer

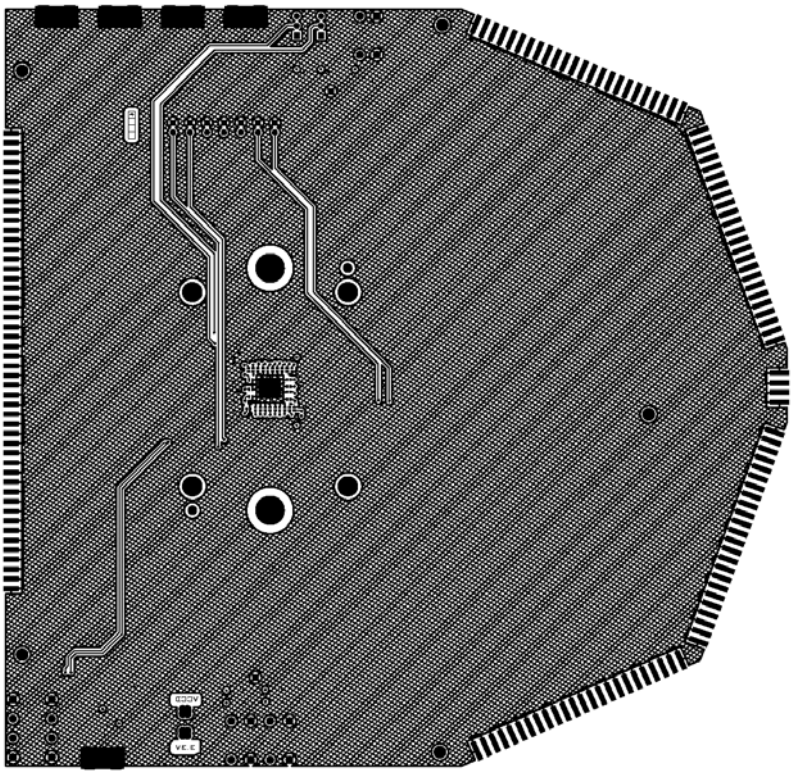


Figure 7-8. Equipped Board (Top)

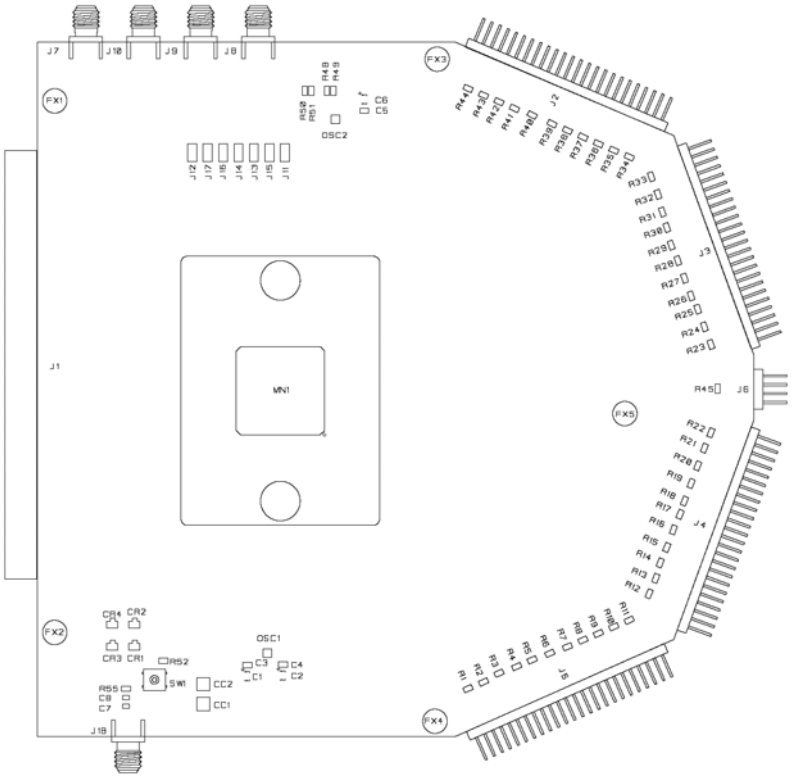
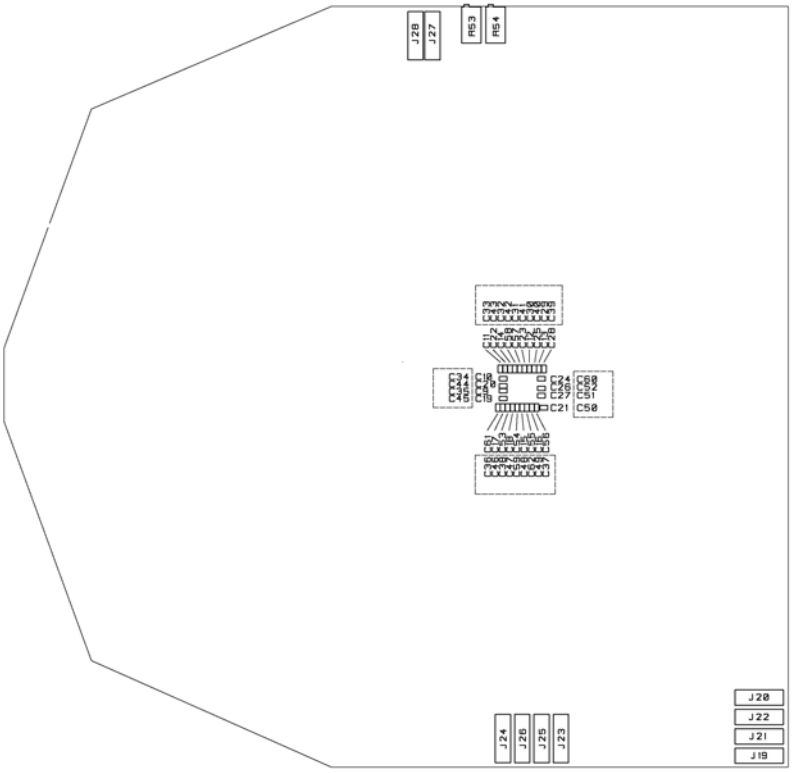


Figure 7-9. Equipped Board (Bottom)



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