Interleaving Two AT84CS001

Application Note

1. Introduction

e2v AT84CS001 10-bit DMUX is able to process data rates of up to 2.2 Gsps in 1:4 ratio, generating an output data rate of up to 550 Msps (both double or single data rate). In some applications, this rate might still be too fast to be processed. It is then necessary to slow down the data rate once more to relax the timing constraints on the processing circuit (ASIC, FPGA, memory).

The solution is to interleave two AT84CS001, thus, achieving a result of 1:8 ratio and leading to a maximum output rate of 275 Msps.

This application note details how it is possible to interleave two AT84CS001 devices. It provides timing and electrical guidelines as well as a practical example with e2v 10-bit 2.2 Gsps ADC AT84AS008.

2. Principle of Operation

It is possible to achieve a 1:8 ratio with two interleaved AT84CS001 DMUXes.

The principle of operation is as follows: each even 10-bit data coming out of the ADC is processed by one DMUX while all odd 10-bit data are processed by the second DMUX. Both DMUXes are set in 1:4 ratio, resulting in a data rate which is eight times slower than the initial sampling rate.

When the DMUX is fed with double data rate (or CLK/2 mode), where both edges of the input clock correspond to a data, which is the case when the DMUX is interfaced to all e2v High Speed ADCs (TS8388B, TS83102G0B, AT84AS008), the configuration is very straightforward as no conversion of the ADC output clock signal is necessary.

In the case of a single data rate (CLK mode) at the DMUX input, additional circuitry is required for the management of the ADC output clock.

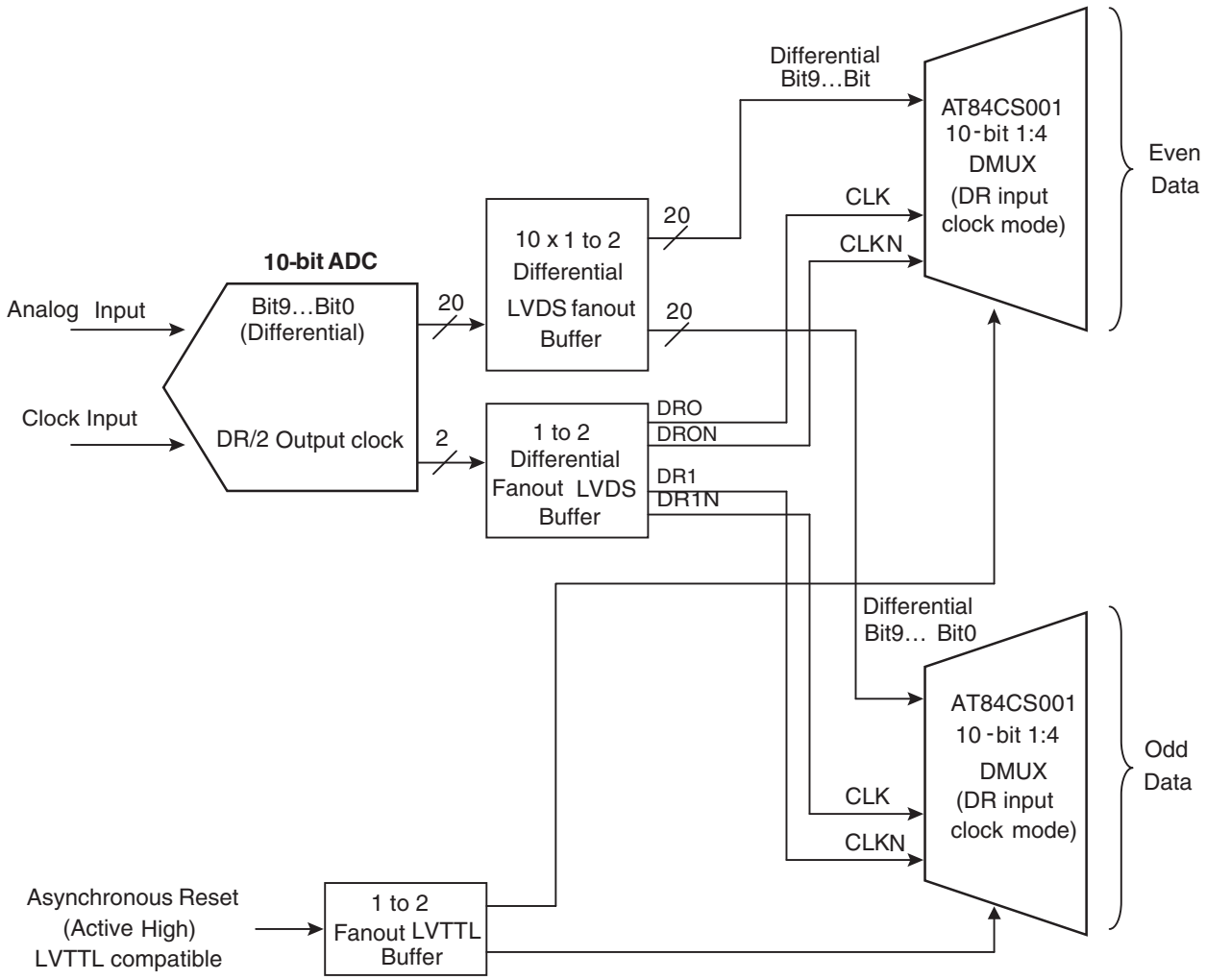
In the following sections, both options are explored and an example with e2v AT84AS008 10-bit 2.2 Gsps ADC is provided.

3. ADC in Double Data Rate

3.1 Block Diagram

The following simplified block diagram illustrates how to achieve a 1:8 demultiplexing ratio using two AT84CS001 LVDS DMUX interfaced with a 10-bit ADC (for example e2v AT84AS008 10-bit 2.2 Gsps ADC). The ADC operates in double data rate (DR/2 mode) but each DMUX operates in single input data rate. The output clock mode of the DMUXes can be either single or double data rate (DR or DR/2 modes).

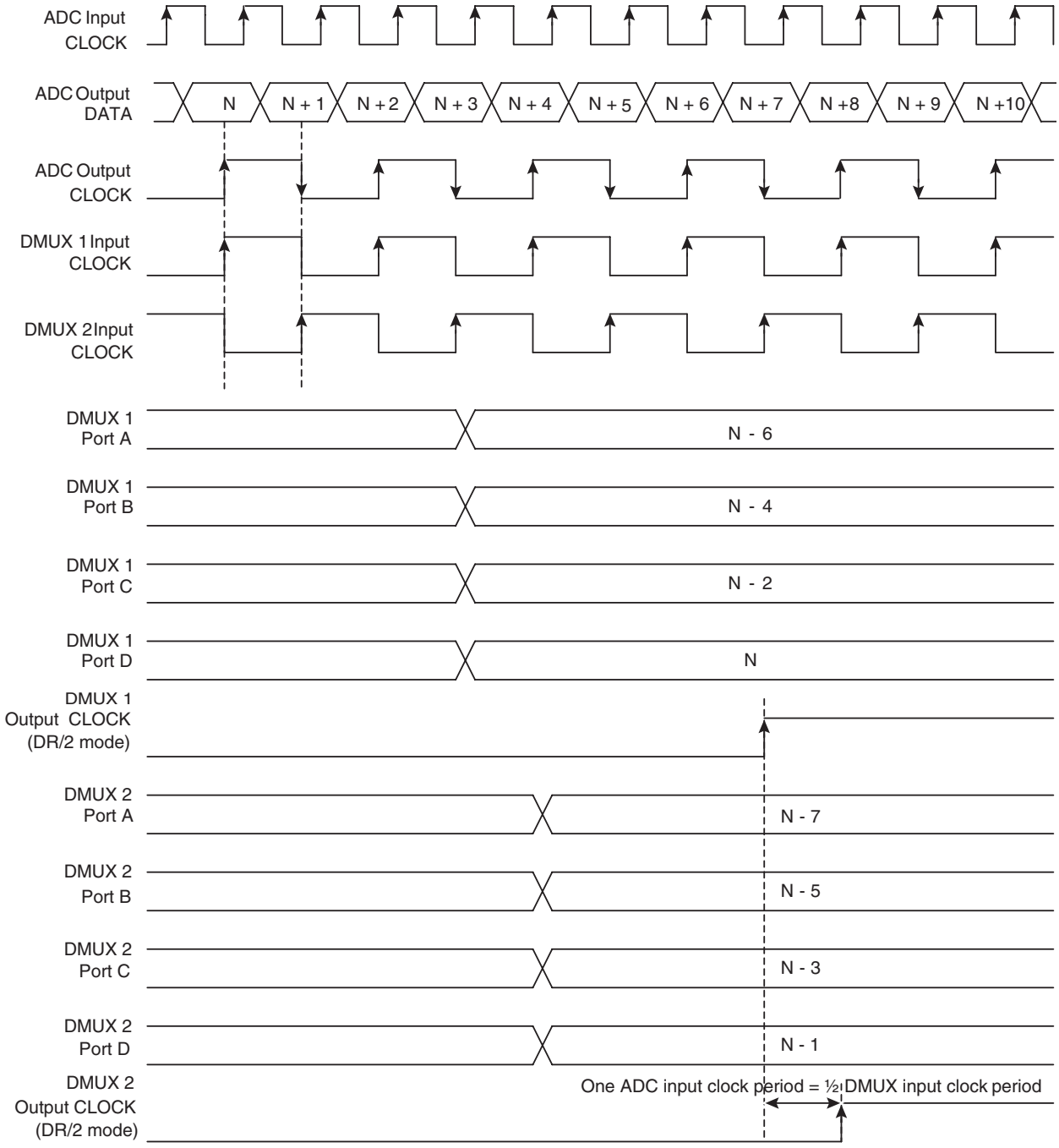
Figure 3-1. Interleaving Two AT84CS001 to Achieve 1:8 Ratio in CLK/2 Mode



Note: The AT84CS001 DMUX features a selectable input clock mode which prevents you from implementing an additional clock circuitry between the ADC and the DMUX. When the data output from the ADC is in CLK/2 mode, each DMUX will only see half of the bits if they are set in the DR input clock mode. This is illustrated in Section 4. "Timing Diagrams" on page 3.

4. Timing Diagrams

Figure 4-1. Interleaving Two AT84CS001 to Achieve 1:8 Ratio in DR/2 Mode - Principle of Operation



For the synchronization of the DMUXes at start-up, it is necessary to apply an asynchronous reset on the two devices simultaneously. Depending on the phase relation between the input clock and the asynchronous reset signal, DMUX 1 will start first or DMUX 2 will start first:

- If the asynchronous reset falling edge occurs when the DMUX 1 input clock is low, then, DMUX 1 will start first (the first data will be on port A of DMUX 1)
- If the asynchronous reset falling edge occurs when the DMUX 2 input clock is low, then, DMUX 2 will start first (the first data will be on port A of DMUX 2)

After reset, the first correct data and output clock at the output of the DMUXes are available after five input clock cycles.

Figure 4-2. Synchronization of the Interleaved DMUXes (DMUX 1 First)

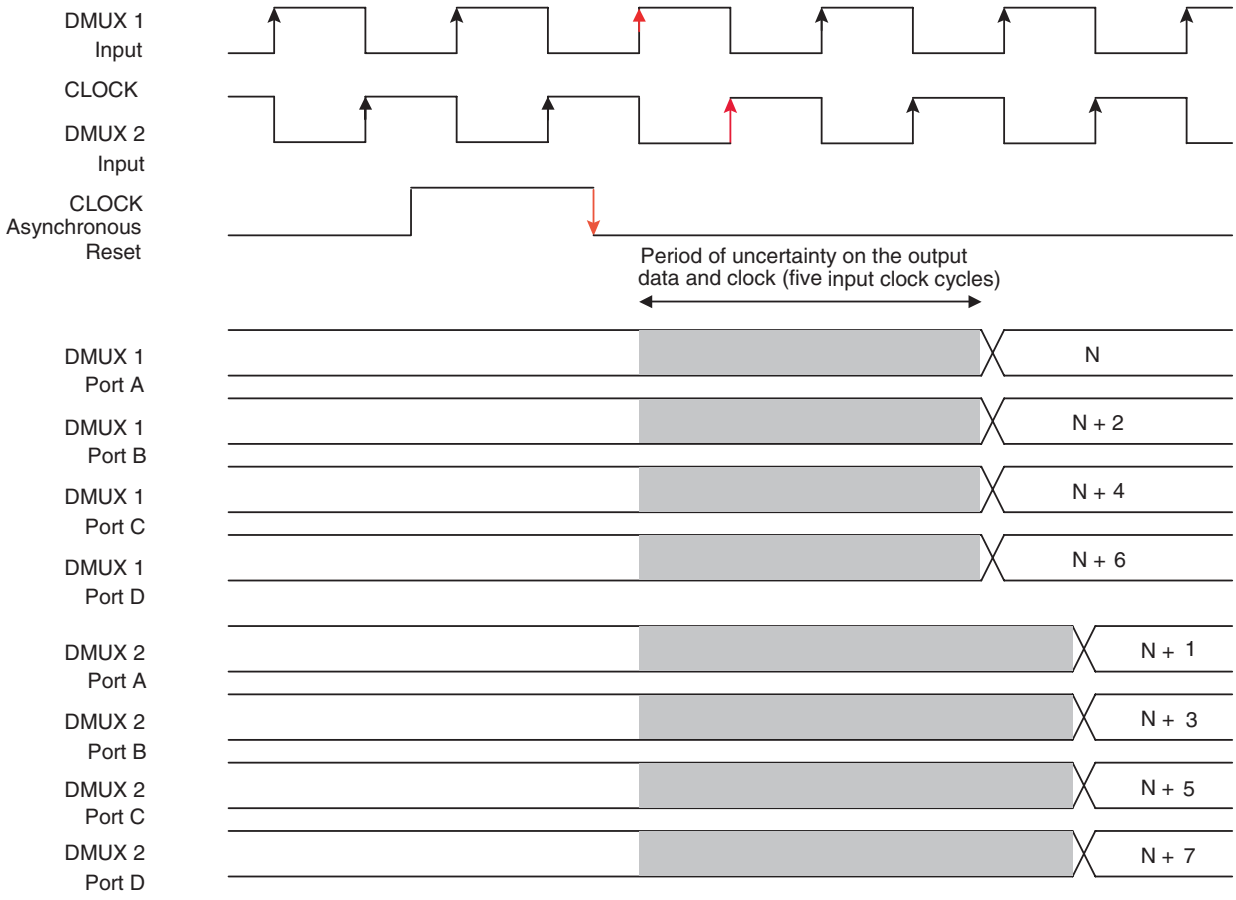
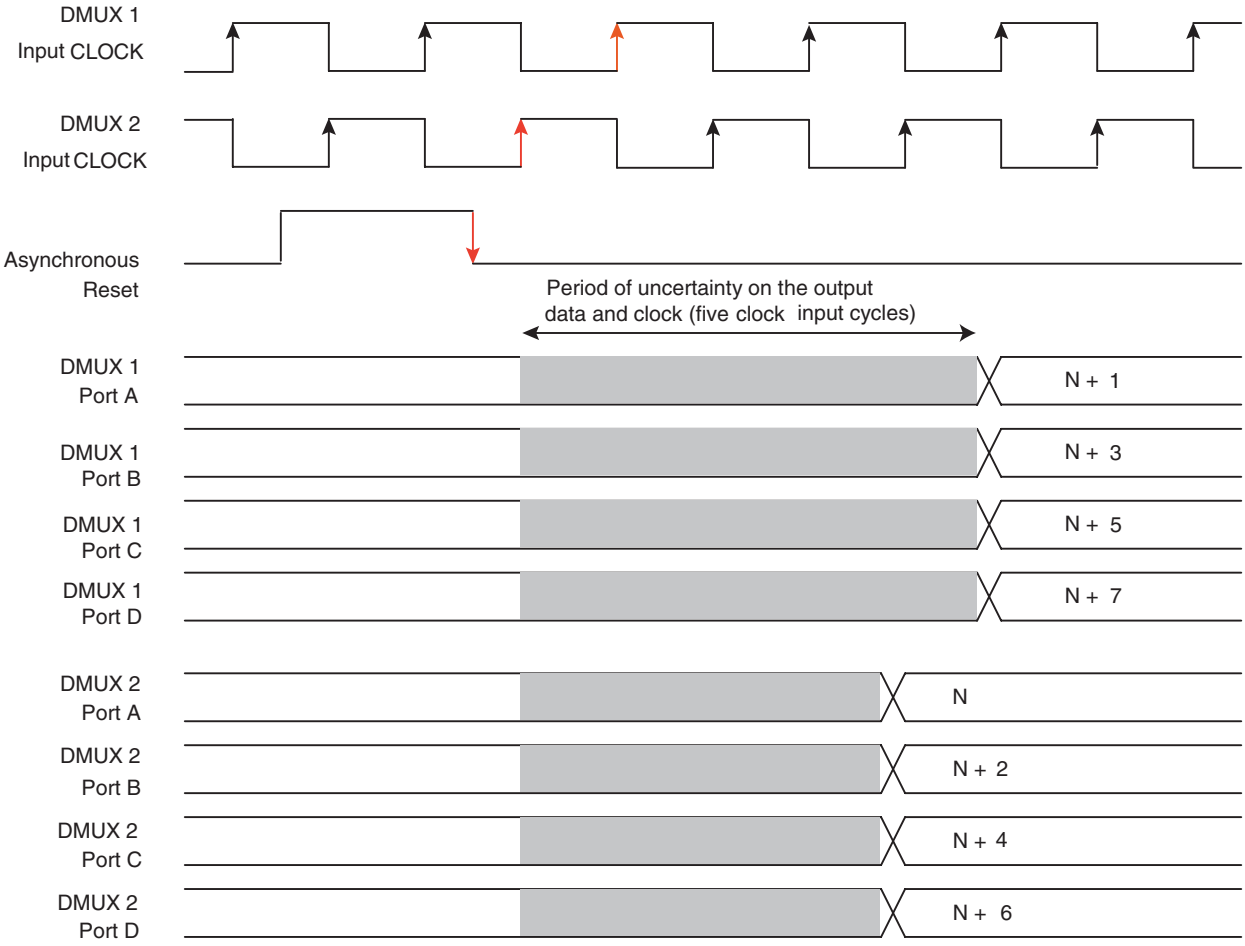


Figure 4-3. Synchronization of the Interleaved DMUXes (DMUX 2 First)



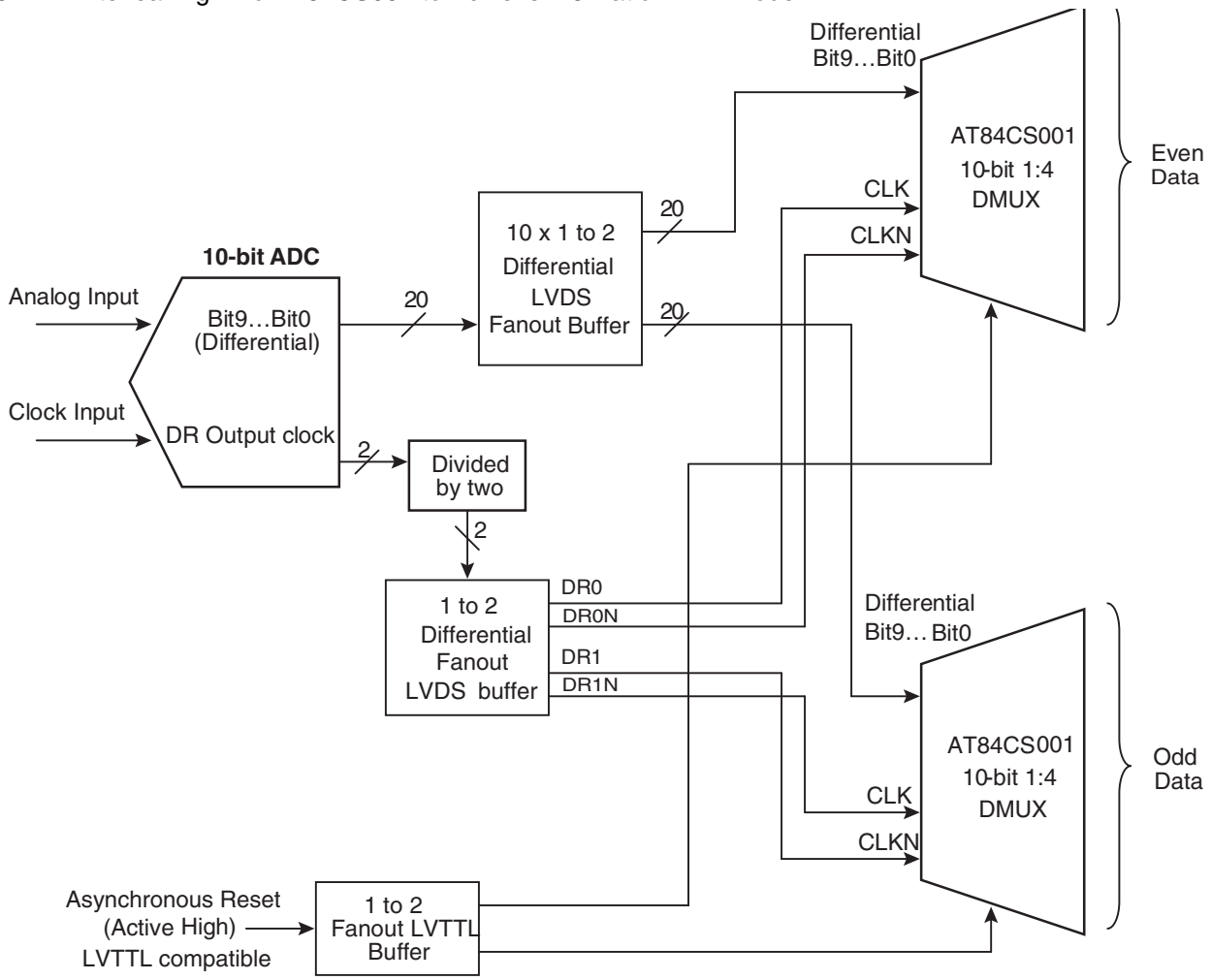
5. ADC in Single Data Rate

5.1 Block Diagram

The following simplified block diagram illustrates how to achieve a 1:8 demultiplexing ratio using two AT84CS001 LVDS DMUX interfaced with a 10-bit ADC operating in single data rate (DR mode).

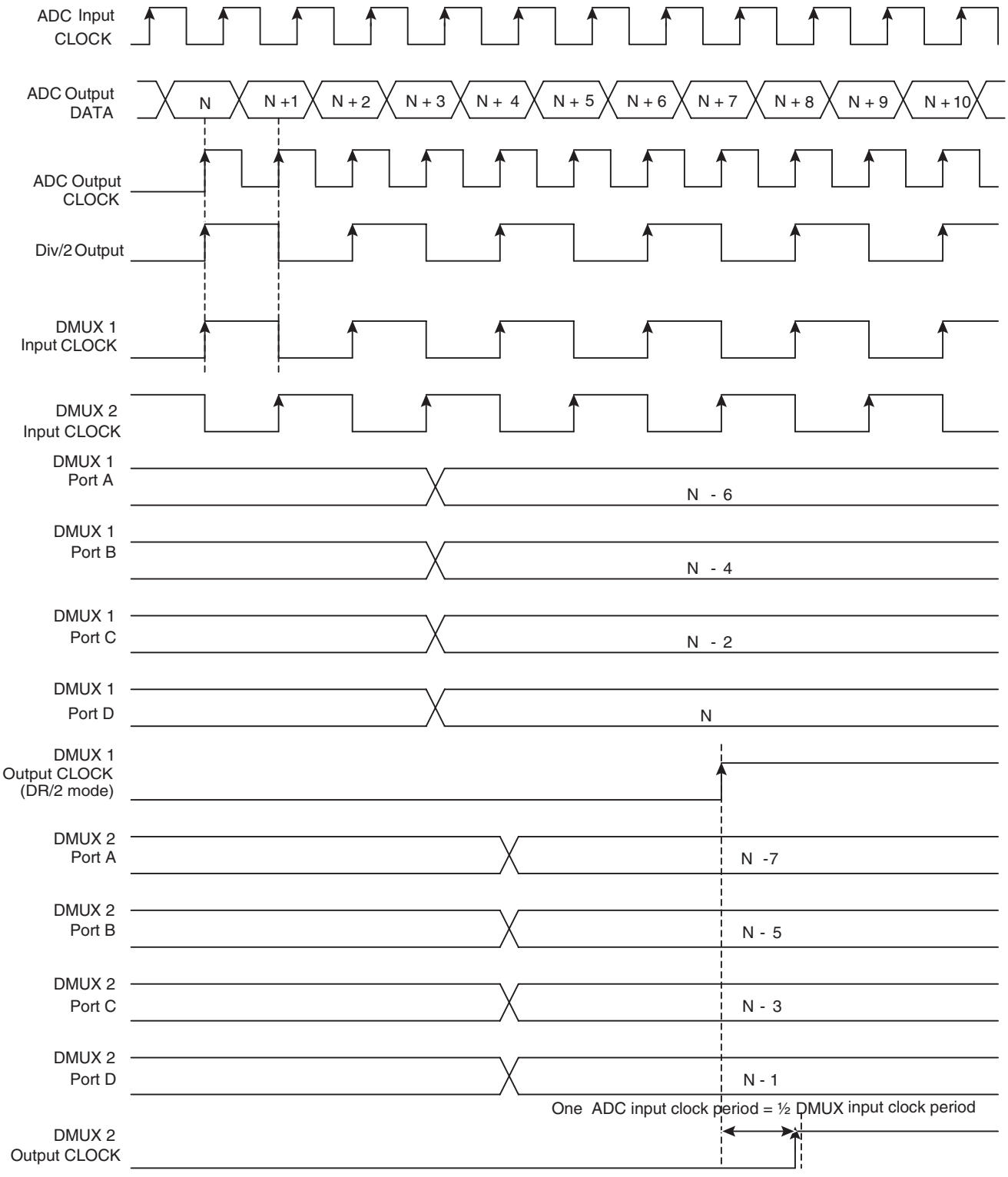
In this case, it is necessary to divide the ADC output clock so that each DMUX will only see half of the data (even data on one DMUX and odd data on the other one).

Figure 5-1. Interleaving Two AT84CS001 to Achieve 1:8 Ratio in DR Mode



6. Timing Diagrams

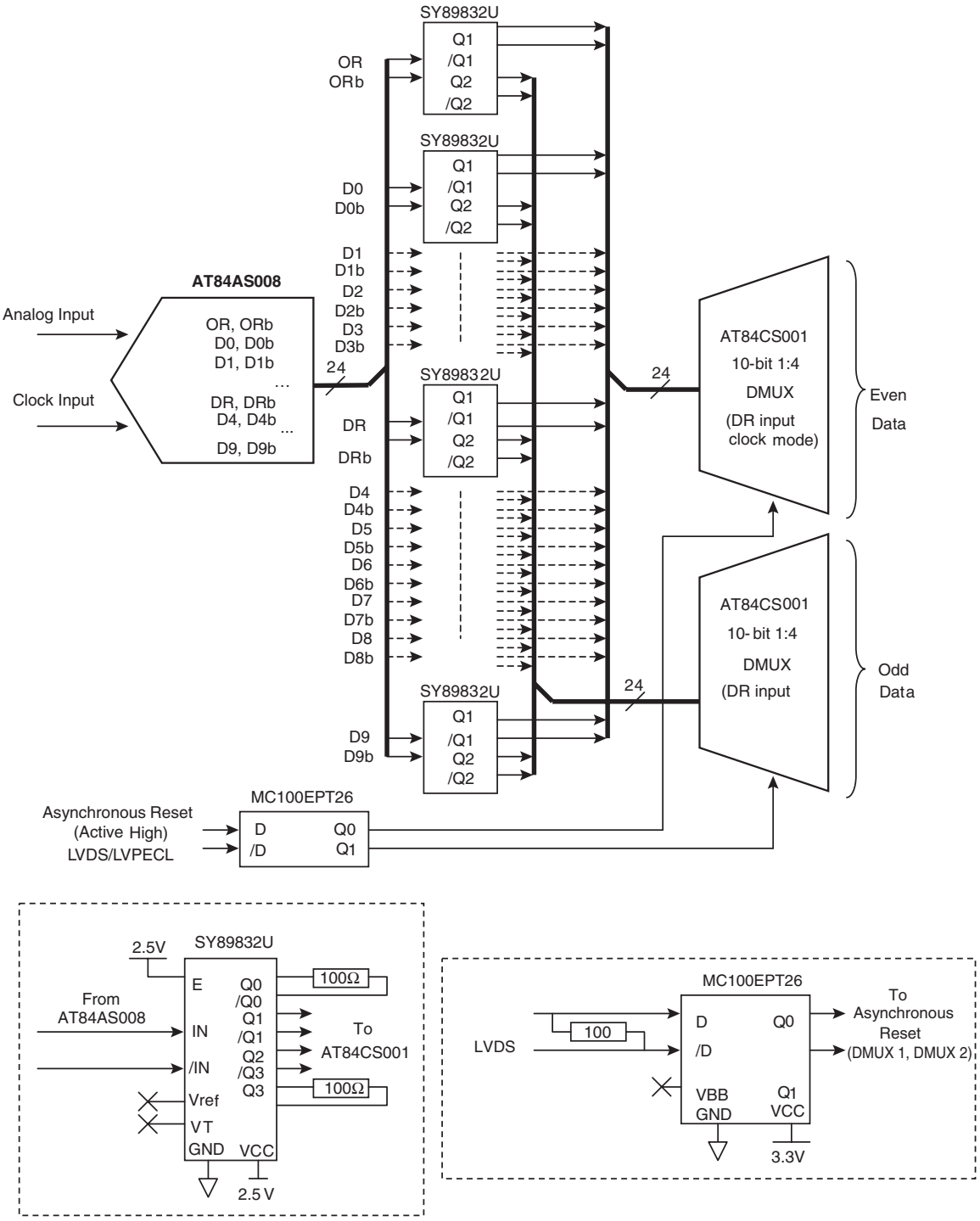
Figure 6-1. Interleaving Two AT84CS001 to Achieve 1:8 Ratio in DR Mode



7. Practical Example: Use with AT84AS008 ADC

When a 1:8 ratio is required to demultiplex the output data coming from the AT84AS008 10-bit 2.2 Gsps ADC, two AT84CS001 DMUXes can be used. The interface between the three devices is depicted in Figure 7-1.

Figure 7-1. Interleaving Two AT84CS001 DMUXes to Achieve 1:8 Ratio at the AT84AS008 ADC Output



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