EV12DS4xxZPY-EB Evaluation Board
12-bit DAC with 4/2:1 MUX
User Guide

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Section 1
Introduction

1.1 Scope

The EV12DS4xxZPY-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the EV12DS400A/EV12DS460A/EV12DS480A 12-bit DAC with 4/2:1 MUX in fpBGA package.

The EV12DS4xxZPY-EB Evaluation Kit includes:

- 1 evaluation board
- A cable for connection to the USB port
- USB key with GUI software.

The evaluation system of the EV12DS400A/EV12DS460A/EV12DS480A DAC device consists in a configurable printed circuit board, including the soldered DAC device, an FPGA chip, a serial interface and a user interface running on that platform.

1.2 Description

The EV12DS4xxZPY Evaluation board is very straightforward as it implements Teledyne-e2v EV12DS480A 12-bit DAC device, ALTERA® FPGA, SMA connectors for the sampling clock, analog outputs, SYNC inputs and DSP accesses.

Thanks to its user-friendly interface, the EV12DS4xxZPY-EB Kit enables to test all the functions of the DAC device.

To achieve optimal performance, the EV12DS4xxZPY-EB is designed in a 10-metal-layer board using RO4003 epoxy dielectric material. The board implements the following devices:

- The EV12DS4xxA-EB 12-bit DAC Evaluation board with the EV12DS480A 12-bit DAC soldered
- SMA connectors for CLK and CLKN, OUT and OUTN, SYNC and SYNCN, DSP and DSPN
- ALTERA FPGA (5AGXFB3H4) soldered to generate the logical pattern or test a user developed code
- Banana jacks for the power supply accesses and the die junction temperature monitoring

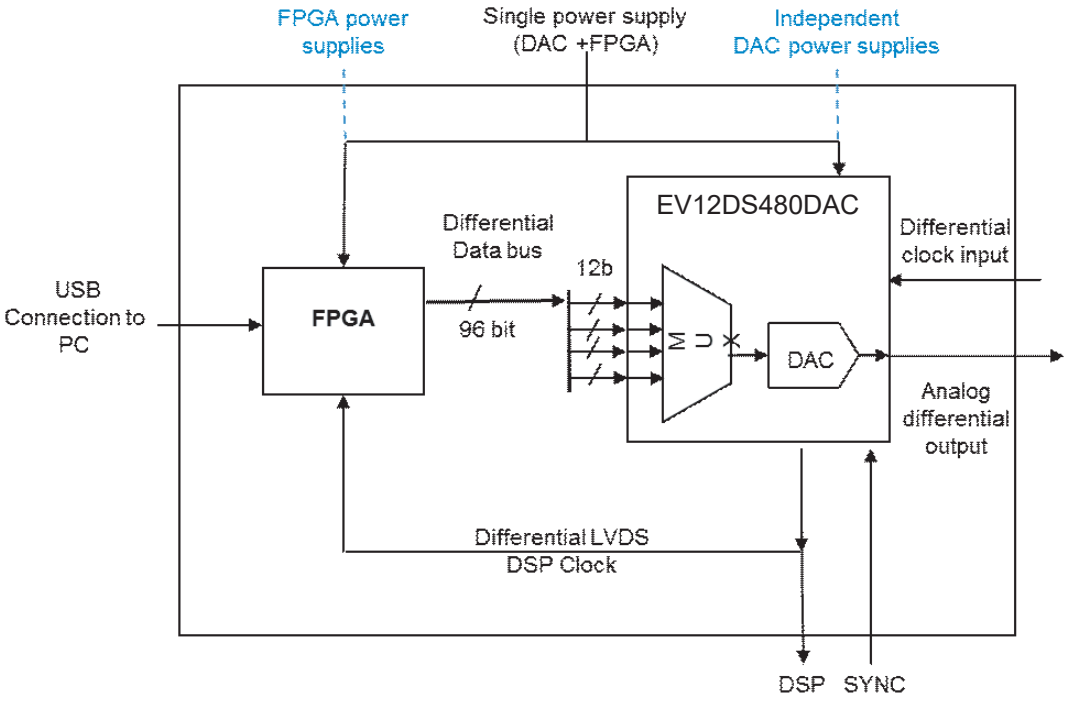
- Jumpers for OCDS and PSS functions
- USB connector for PC interface.

The board dimensions are 192 mm x 260 mm.

The board comes fully assembled and tested.

The following figure shows a simplified schematic of the evaluation board.

Figure 1-1. EV12DS4xxA-EB Evaluation board simplified schematic



As shown in Figure 1-1, the board can be powered up using two configurations:

Either through individual power supplies:

- V_{CCA5} = 5V analog power supply
- V_{CCD} = 3.3V digital power supply
- V_{CCA3} = 3.3V analog power supply
- 12V FPGA

Or through a single 12V power supply that supplies both the FPGA and the board through regulators.

Detailed protocol to switch from single to independent power supply is given in Section 2.9.3.

Section 2

Hardware Description

2.1 Board Structure

In order to achieve full speed operation of the EV12DS4xxZPY-EB 12-bit DAC, a multi-layer board structure was retained for the evaluation board. Ten copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in RO 4003 and 370 HR dielectric material.

Figure 2-1 gives the board thickness profile. Each layer is given by a brief description in Table 2-1.

Figure 2-1. Board layer thickness profile

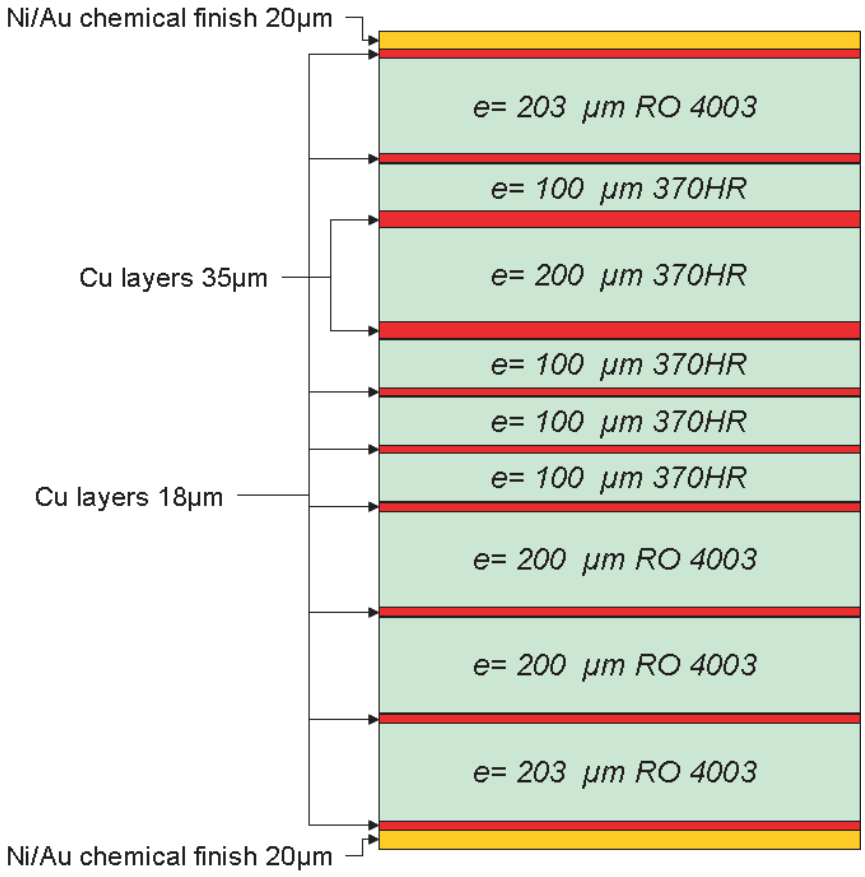


Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 / Copper layer	Copper thickness = 18 µm (with NiAu finish) Signals traces
RO 4003 / dielectric layer	Layer thickness = 203 µm
Layer 2 / Copper layer	Copper thickness = 18 µm Ground plane = AGND - DGND plane
370 HR / dielectric layer	Layer thickness = 100 µm
Layer 3 / Copper layer	Copper thickness = 35 µm Power plane $V_{CCA3,}$
370 HR / dielectric layer	Layer thickness = 200 µm
Layer 4 / Copper layer	Copper thickness = 35 µm Reference plane = ground
370 HR / dielectric layer	Layer thickness = 100 µm
Layer 5 / Copper layer	Copper thickness = 18 µm Power plane = DAC, V_{CCD} and V_{CCA}
370 HR / dielectric layer	Layer thickness = 100 µm
Layer 6 / Copper layer	Copper thickness = 18 µm Ground plane = AGND DAC
370 HR / dielectric layer	Layer thickness = 100µm
Layer 7 / Copper layer	Copper thickness = 18 µm Ground plane for layer 8
RO 4003 / dielectric layer	Layer thickness = 200µm
Layer 8 / Copper layer	Copper thickness = 18 µm Signals traces
RO 4003 / dielectric layer	Layer thickness = 200µm
Layer 9 / Copper layer	Copper thickness = 18 µm Ground plane for layer 10 AGND
RO 4003 / dielectric layer	Layer thickness = 203 µm
Layer 10 / Copper layer	Copper thickness = 18 µm (with Ni/Au finish) Signals traces

The board is 1.6 mm thick.

2.2 Analog Outputs

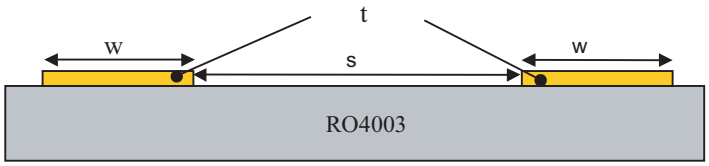
The differential analog output is provided by SMA connectors (Southwest Reference: 1092-01A-5).

Both pairs are AC coupled using 100 nF capacitors (ATC550L-104-K-T).

Special care was taken for the routing of the analog output signal for optimum performance in the high frequency domain:

- Differential lines, 100Ω differential characteristic impedance
- Max difference length between OUT and OUTN ±0.1mm
- 0.12 mm spacing (s) between the differential traces
- 0.22 mm line width (w)
- 0.038 mm thickness (t)
- 850 µm diameter hole in the ground layer below the OUT and OUTN ball footprints.

Figure 2-2. Board layout for the differential signals



Note: The analog output is AC coupled with 100 nF close to the SMA connectors.

2.3 Clock Inputs

The differential clock inputs is provided by SMA connectors (Reference: 142-0701-851).

Both pairs are AC coupled using 10 nF capacitors (Reference: ATC 520L103KT16T).

Special care was taken for the routing of the clock input signal for optimum performance in the high frequency domain:

- Differential lines, 100Ω differential characteristic impedance
- Max difference length between CLK and CLKN ±0.1mm
- 0.12 mm spacing (s) between the differential traces see Figure 2-2
- 0.22 mm line width (w)
- 0.038 mm thickness (t)

Note: The clock input is AC coupled with 10 nF very close to the SMA connectors.

2.4 Digital Inputs

The digital input lines were designed with the following recommendations:

- Differential lines, 100Ω differential impedance
- Max difference between each differential pairs ±0.5mm
- All differential lines for Digital input data and IDC IDCN are routed to have the same propagation time (whatever the layer) and taking into account FPGA and DAC skew package
- Digital inputs are routed in layer 1, 8 and 10.
- Spacing, width and thickness are different as a function of the layer. They are described below

	W (mm)	S (mm)	H (mm)	T (mm)
TOP	0,22	0,12	0,203	0,038
INTERNAL	0,13	0,12	0,4	0,018
BOTTOM	0,22	0,12	0,203	0,038

The digital inputs are compatible with LVDS standard.

2.5 SYNC Inputs

SYNC, SYNCN corresponds to the reset of the output of the DAC (analog reset).

The differential reset inputs are provided by SMA connectors (Reference: 142-0701-851).

- Differential lines, 100Ω differential impedance
- Max difference between SYNC and SYNCN ±0.1 mm
- 0.12 mm spacing (s) between the differential traces see Figure 2-2
- 0.22 mm line width (w)
- 0.038 mm thickness (t)

2.6 DSP, DSPN Inputs

The differential DSP and DSPN signals are provided by the SMA connectors (Reference: 142-0701-851).

Special care was taken for the routing of DSP, DSPN signals for optimum performance in the high frequency domain:

- Max difference between DSP and DSPN ±0.1mm
- Digital signal LVDS
- 0.12 mm spacing (s) between the differential traces see Figure 2-2
- 0.22 mm line width (w)
- 0.038 mm thickness (t)

DSP, DSPN are not used for normal operation. They can be left open.

2.7 CALIBRATION Lines

Both pairs are AC coupled using 100 nF capacitors (ATC550L-104-K-T).

Calibration lines have exactly the same length as Analog Output lines. They are not used for normal operation. They can be left open.

2.8 Power Supplies

Layers 3 and 5 are dedicated to power supply planes (V_{CCA3}, V_{CCD}, V_{CCA5} and 12V FPGA)

The supply traces are low impedance and are surrounded by two ground planes (layer 4 and 6).

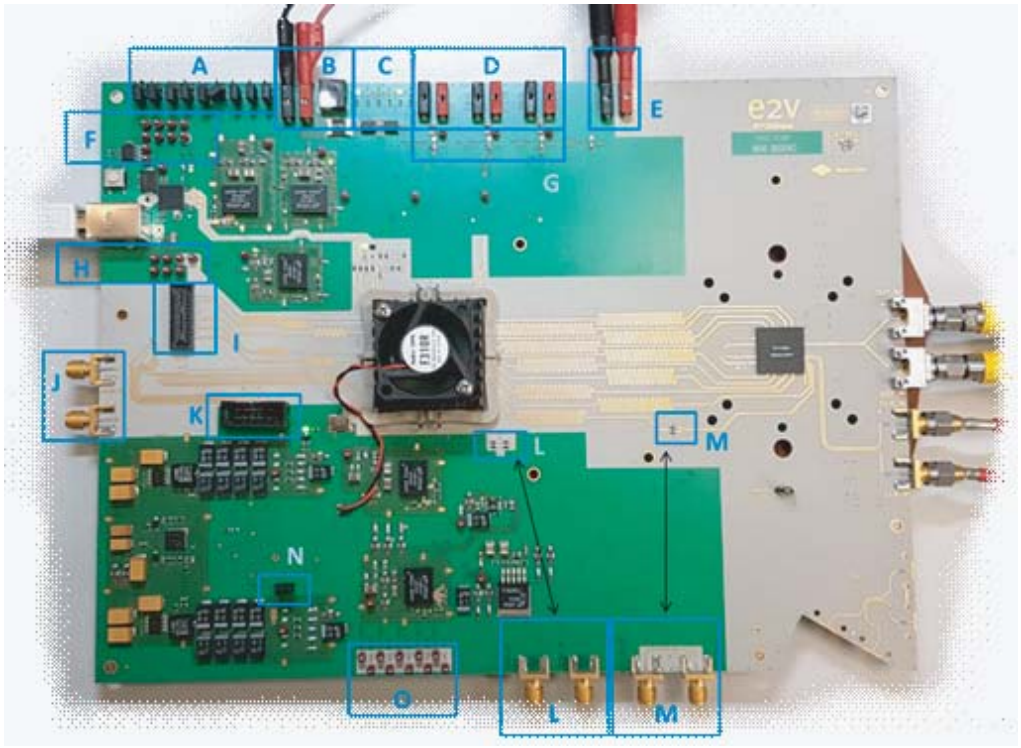
Each incoming power supply is bypassed at the banana jack by a 1 µF capacitor in parallel with a 100 nF capacitor.

Each power supply is decoupled as close as possible to the EV12DS480A device by 10 nF in parallel with 100 pF surface mount chip capacitors.

2.9 Board configuration

2.9.1 Overview

Figure 2-3. Board overview



The board, depicted in Figure 2-3, contains several areas which are described below:

- A : DAC jumper configuration
- B : General power supply
- C : Application LED
- D : External DAC power supplies

- E : DAC temperature diode
- F : Communication between FX2 and DAC through FPGA
- G : Configuration DAC power supplies
- H : Communication between FX2 and FPGA
- I : Spare SAMTEC connector
- J : Spare SMA
- K : JTAG FPGA connector
- L : DSP_CLK configuration and connectors
- M : SYNC configuration and connectors
- N : FX2 reset
- O : Communication from FPGA to DAC

These areas will be specifically detailed in the following paragraphs.

2.9.2 General power supply

The general power supply is in area B. You can supply the board by 1.3mm jack connector or banana plug.

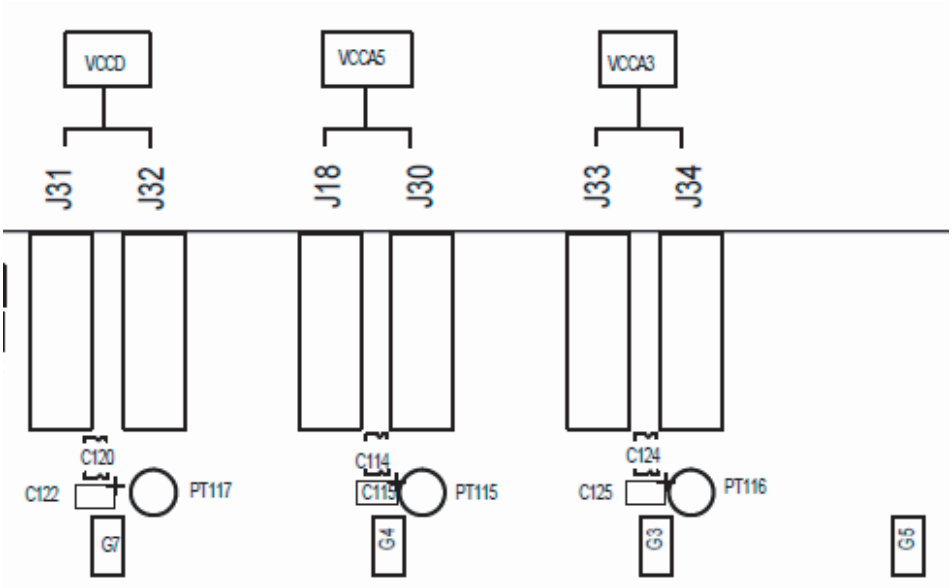
For banana plug, the red must be connected to +12V and the black to GND.

For jack connector, the +12V have to be in the center and the GND to the exterior.

2.9.3 DAC power supply

The DAC can be supplied by a single 12V power supply (that supplies both FPGA and DAC through regulators see general power supply section) or independent external power supplies through area D.

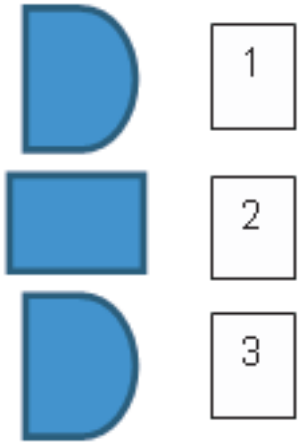
Figure 2-4.



PT117, PT115 and PT116 are test points of V_{CCD}, V_{CCA5} and V_{CCA3}.

Drops below banana jack (area G) enable to switch from single to external power supplies

All the drops G3, G4, G5 and G7 are represented below



To supply the DAC through the single 12V power supply (called INT on board), you have to do a short circuit between pin 2 and 3 on G37, G4, G5 and G7.

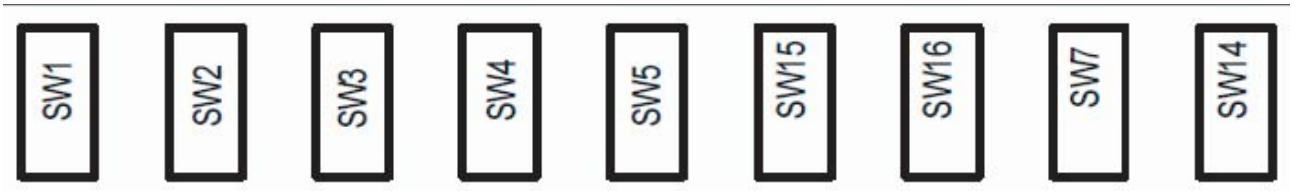
To supply the DAC with external power supplies (called EXT on board), you have to do a short circuit between pin 1 and 2 on G3, G4, G5 and G7.

2.9.4 Configuration

2.9.4.1 Jumper

Jumper configurations are in area A.

Figure 2-5.



Jumper signification:

SW1: PSS0

Open: Disable PSS0=0

Closed: Enable PSS0=1

SW2: PSS1

Open: Disable PSS1=0

Closed: Enable PSS1=1

SW3: PSS2

Open: Disable PSS2=0

Closed: Enable PSS2=1

SW4: OCDS

Open: Disable OCDS1

Closed: Enable OCDS2

SW5: Test ramp

Open: Disable ramp pattern

Closed: Enable ramp pattern

Jumper SW7, SW14, SW15 and SW16 are spare.

NB: If SW5 is closed, the DAC outputs a ramp, whatever PC bench or PC GUI configuration is.

2.9.4.2 Reset FX2

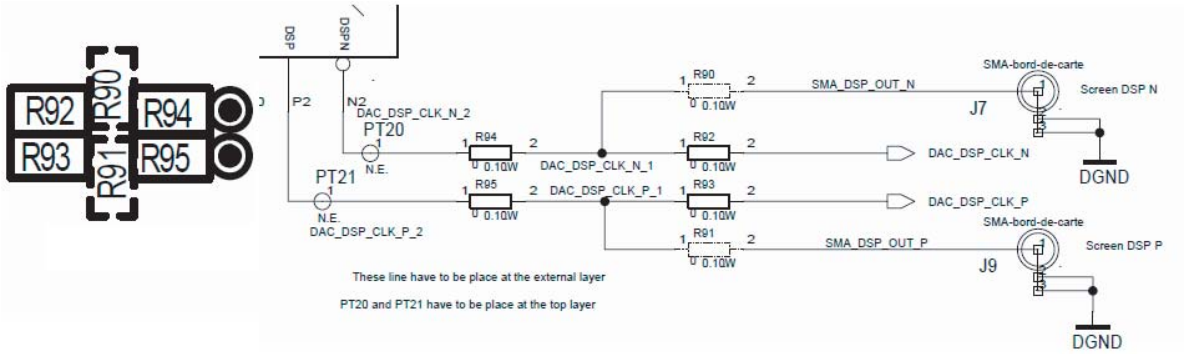
The FX2 controller can be reset using jumper at area N.

In closed position, the jumper disables the µcontroller so that the user can handle the FPGA directly. In open position the FX2 µC regains control over the FPGA (usual working condition).

2.9.4.3 DSP_CLK

You can configure the input/output of the DSP_CLK clock in area L.

Figure 2-6.



R92 and R93 must be mounted to connect the FPGA, R94 and R95 must be mounted to connect the DAC and

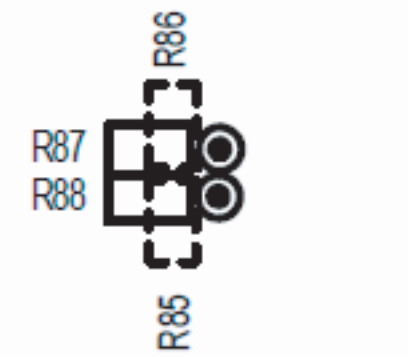
R90 and R91 are put to connect SMA.

In other terms, in order to connect the DSP_CLK of the DAC to the FPGA, you have to mount R92, R93, R94 and R95. Similarly, to connect the DSP_CLK from the SMA connector to the FPGA, you have to mount R90, R91, R92 and R93.

Note: Do not connect all the resistors in the same time

2.9.4.4 SYNC

You can configure the input/output of the SYNC in area M



R87 and R88 must be mounted to drive the DAC SYNC by the FPGA.

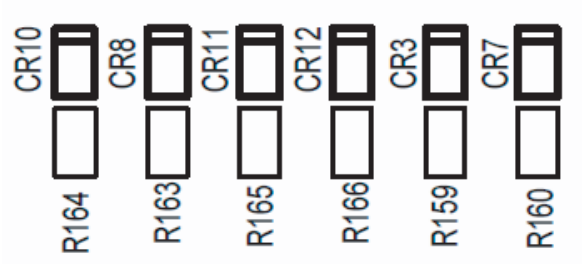
R85 and R86 must be mounted to drive the DAC SYNC by the SMA.

Note: Do not connect all the resistors in the same time

2.9.5 Indicators

2.9.5.1 LED signification

The LEDs are in area C.



CR7: TVF

On: violation is detected

Off: violation is not detected

CR3:

On: FPGA PLL is locked (on DSP_CLK)

Off: FPGA PLL is unlocked (no DSP_CLK or discontinued DSP_CLK)

CR10:

On: external configuration (by jumper)

Off: internal configuration (by GUI)

CR8, CR10, CR11 and CR12 are connected to FPGA.

2.9.5.2 DAC temperature

The banana plug in area E is directly connected to the DAC diode.

2.9.6 Communication

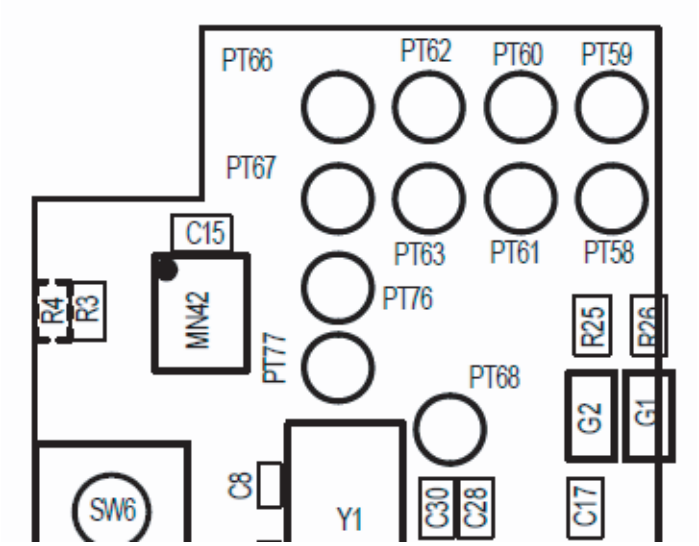
On this board, 3 elements communicate: FX2, FPGA and the DAC.

The area F has test points to check the communication between FX2 and DAC through FPGA.

The area H has test points to check the communication between FX2 and FPGA.

The area O has test points to check the communication between FPGA and DAC.

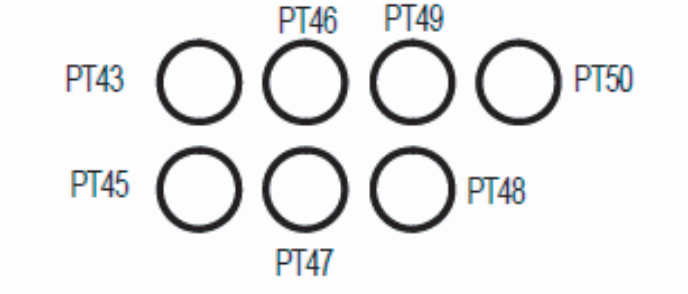
2.9.6.1 Communication between FX2 and DAC through FPGA



Tests point signification:

- PT58: RSTN (DAC 3WSI)
- PT59: MOSI (DAC 3WSI)
- PT60: SCK (DAC 3WSI)
- PT61: CSN (DAC 3WSI)
- PT62: PSS0
- PT63: PSS1
- PT66: PSS2
- PT67: OCDS
- PT76: SCL (to FX2 memory)
- PT77: SDA (to FX2 memory)

2.9.6.2 Communication between FX2 and FPGA

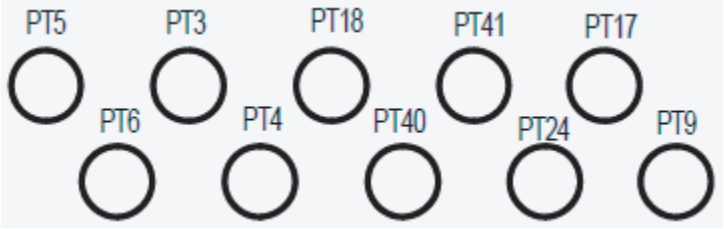


Test points signification:

- PT43: CSN0
- PT45: CSN1
- PT46: CSN2
- PT47: SCK
- PT48: MOSI
- PT49: MISO
- PT50: TVF (FPGA to FX2)

2.9.6.3 Communication between FPGA and DAC

Test points between FPGA and DAC are in area O.



Test points signification:

- PT3: PSS0
- PT4: PSS1
- PT5: Iref test
- PT6: OCDS
- PT9: TVF
- PT17: RSTN
- PT18: PSS2
- PT24: SLDN
- PT40: SCLK
- PT41: SDATA

2.9.7 SPARE/DEBUG

This board contains several debug/spare connectors whether SMA (area J) or Samtec connector (area I).

Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the EV12DS4xxZPY-EB board.

The analog output and the sampling clock signals are differential.

Note:The analog outputs and clock are AC coupled on the board.

3.2 Operating Procedure

1. Install the software as described in Section 4 "Software Tools".
2. Connect the power supplies and ground accesses through the dedicated banana jacks.
   V_{CCA3} = 3.3V, V_{CCD} = 3.3V, V_{CCA5} = 5V and +12V for the FPGA
   or only the +12V for single power supply depending on drops configuration G3,G4,G5 and G7.
3. Connect the clock input signals.
   The clock input level is typically -4 to 8.5 dBm and should not exceed 12 dBm.
4. Connect the analog output signals (the board has been designed to allow only AC coupled analog outputs). The analog output signals must be used in differential via differential-to-single transformer.
5. Connect the PC's USB connector to the Evaluation Board's serial interface.
6. Turn on the RF clock generator.
7. Switch on power supplies

   a. Either general power supply 12V

   b. Or the FPGA power supply (+12V) and the DAC power supplies.
   Mandatory power up sequence in the following order:

   1st power supply: V_{CCD} = 3.3V

   2nd power supply: V_{CCA3} = 3.3V

   3rd power supply: V_{CCA5} = 5V

If you do not perform the above power up sequence SYNC is necessary. SYNC can be done through GUI or SYNC/SYNCN input

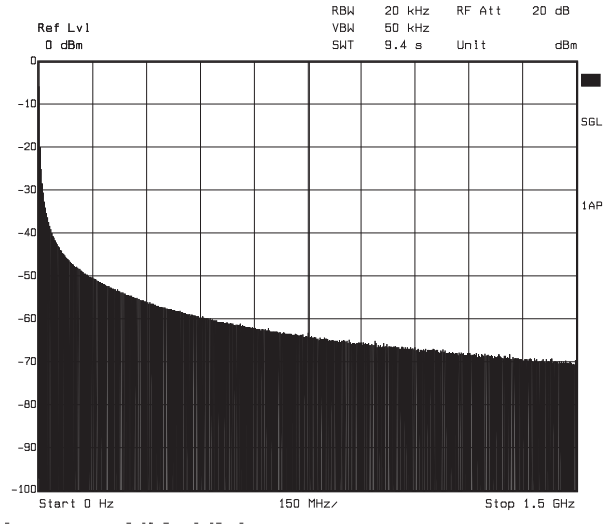
8. Launch software (software must be launched after evaluation board has been powered ON)
9. Perform a SYNC of the device on GUI.

The EV12DS4xxZPY-EB evaluation board is now ready for operation.

Note: To use the software, you should be in Administrator mode.

To check the good synchronization between FPGA and DAC, put the jumper ramp test (SW5) and NRZ mode. The following graph shows a good synchronization.

Figure 3-1. Neat ramp pattern in frequency domain (on spectrum analyzer). FPGA & DAC are correctly synchronized.



3.3 Electrical Characteristics

For more information, please refer to the device datasheets.

Table 3-1. Recommended Conditions of Use

Parameter	Symbol	Recommended Value	Unit
V_{CCA5} analog supply voltage	V_{CCA5}	5.0	V
V_{CCA3} analog supply voltage	V_{CCA3}	3.3	V
V_{CCD} digital supply voltage	V_{CCD}	3.3	V
Digital input (on each single ended input), IDC and SYNC signal Port P = A, B, C, D V_{IL} V_{IH} Digital input differential swing	 $[P_0..P_{11}]$, $[P_{1N}..P1_{1N}]$, IDC_P, IDC_N, SYNC, SYNCN	 1.075 1.425 700	 V V mVpp
Master Clock input differential mode swing	CLK, CLKN	1.77	Vpp
Master Clock input power level (differential mode)	P_{CLK}	3	dBm
Control function inputs V_{IL} V_{IH}	PSS[0..2], OCDS, reset_n, sclk, sdata, sld_n	 0 V_{CCD}	 V V

Note: Analog output is in differential

Single-ended operation is not recommended. Optimum performance is only in differential configuration. For optimal settings (RPB, RPW), please refer to the datasheet.

Table 3-2. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
RESOLUTION			12		bit
Power Supply voltage - Analog - Analog - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	 V V
Power Supply current (4:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}		 100 210 435		 mA mA mA
Power Supply current (2:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}		100 210 365		mA mA mA
Power dissipation (4:1 MUX)	PD4		2.6		W
Power dissipation (2:1 MUX)	PD2		2.4		W

Section 4

Software Tools

4.1 Overview

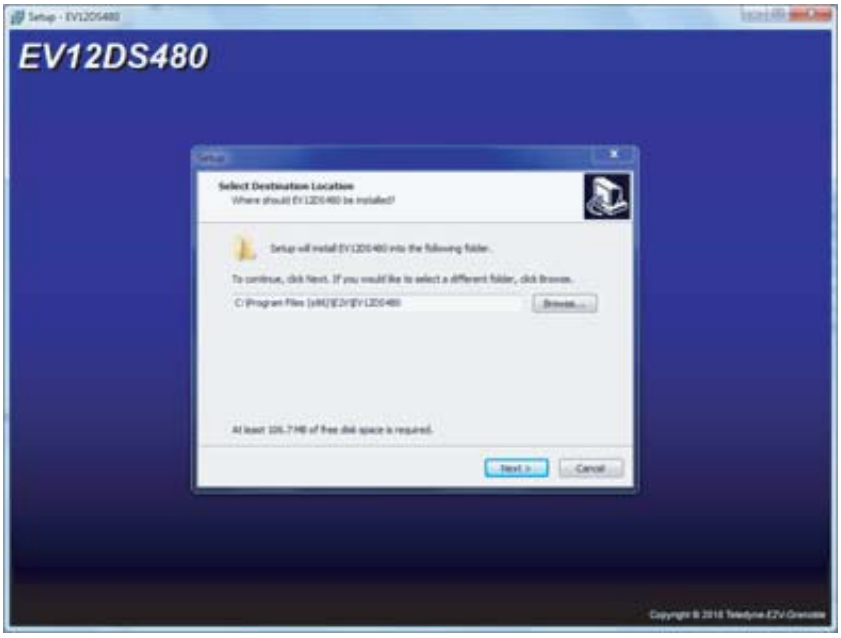
The 12-bit DAC Evaluation user interface software is a Visual C++® compiled graphical interface that does not require a licence to run on Windows® XP® and Windows® 7 PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Getting Started

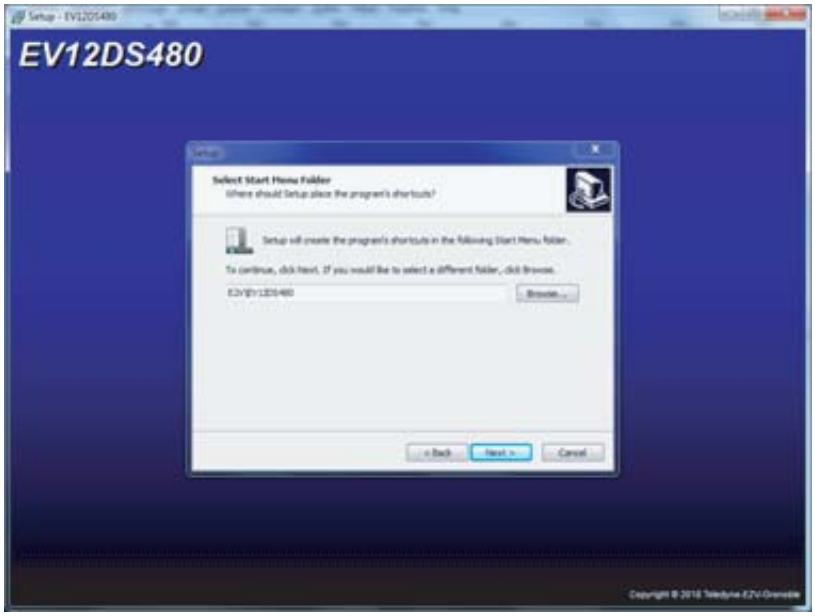
1. Install the EV12DS480 application on your computer by launching the .exe installer (please refer to the latest version available)

Figure 4-1. Application "Setup wizard" window



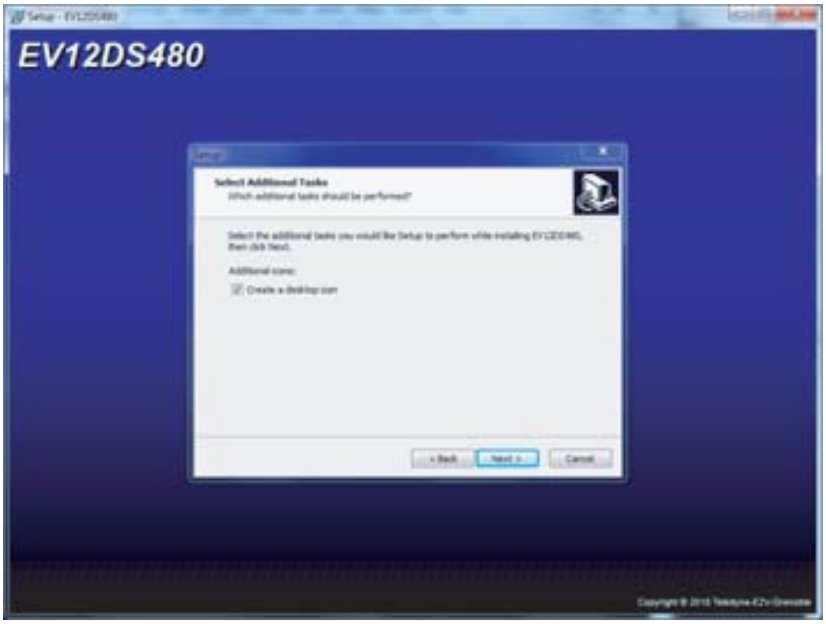
2. Select Destination Directory

Figure 4-2. "Select Destination Directory" window



3. Select Start Menu Folder

Figure 4-3. "Select Start Menu Folder"



4. Create desktop icon

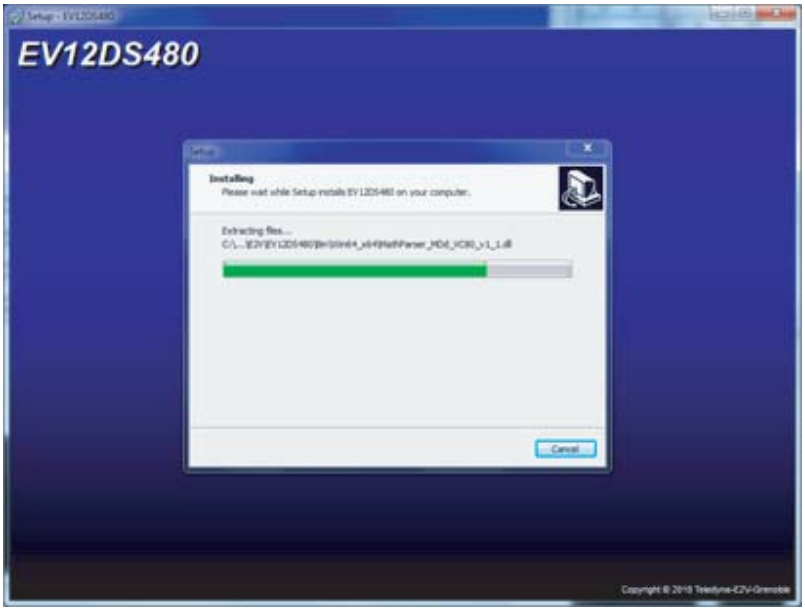
5. Ready to install

Figure 4-4. Ready to Install window

If you agree with the install configuration, press Install button.

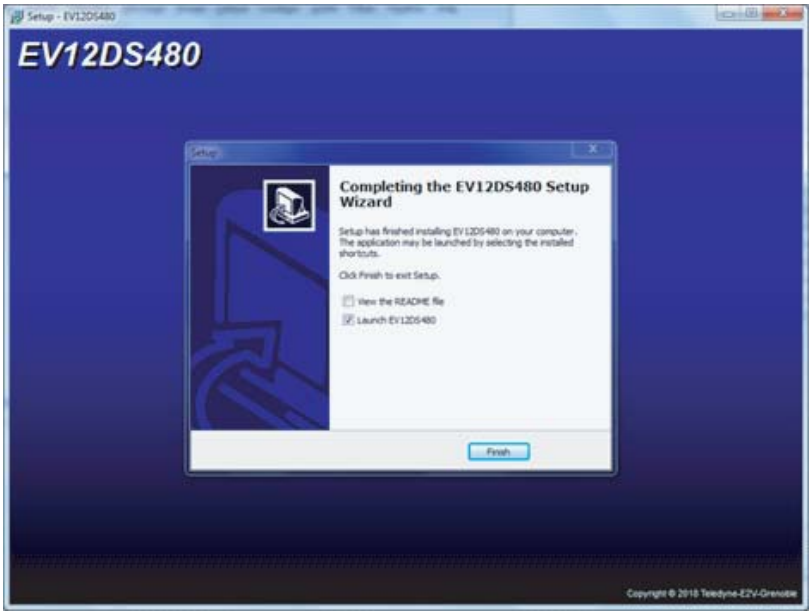
6. Install in progress

Figure 4-5. Install in progress windows



7. Setup complete

Figure 4-6. "Completing Setup wizard" window

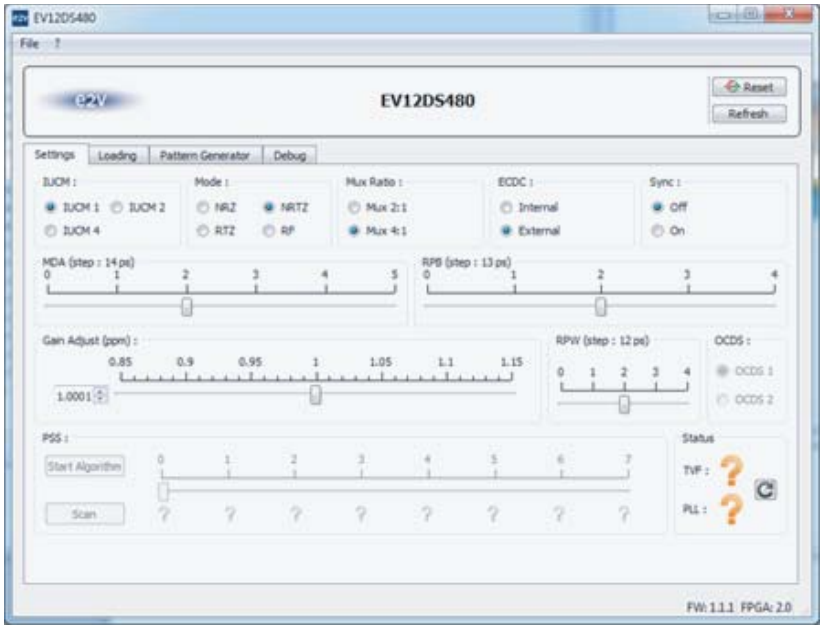


This window allows the user for two options: "View the read me file" and "Launch EV12DS480" application.

After the installation, you also can launch the interface with the following file: C:\Program Files (x86)\E2V\EV12DS480\

The window shown in Figure 4-7 will be displayed.

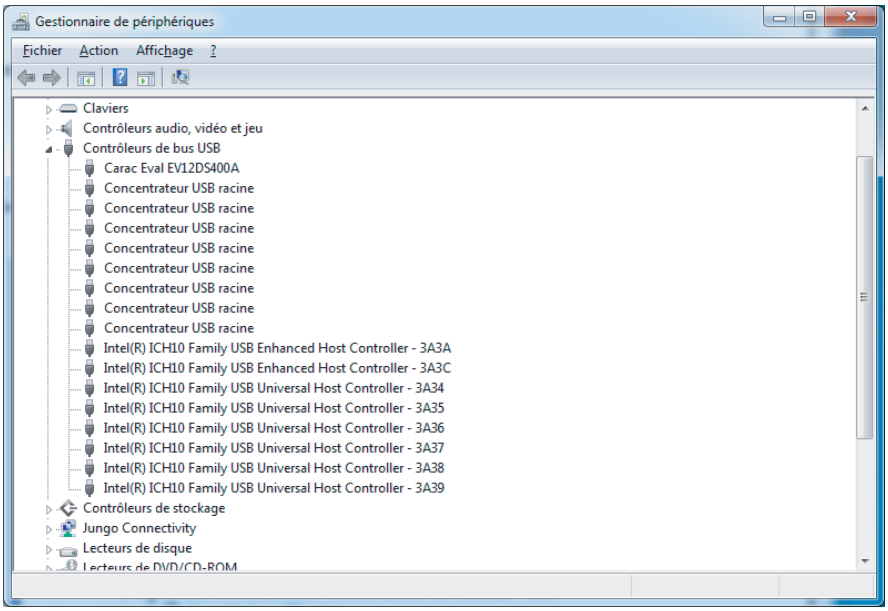
Figure 4-7. "User Interface" window



4.3 Troubleshooting

1. check that you own rights to write in the directory
2. check for the available disk space
3. check that at least one USB port is free and properly configured
4. check that all supplies are properly powered on

Figure 4-8. USB port driver configuration



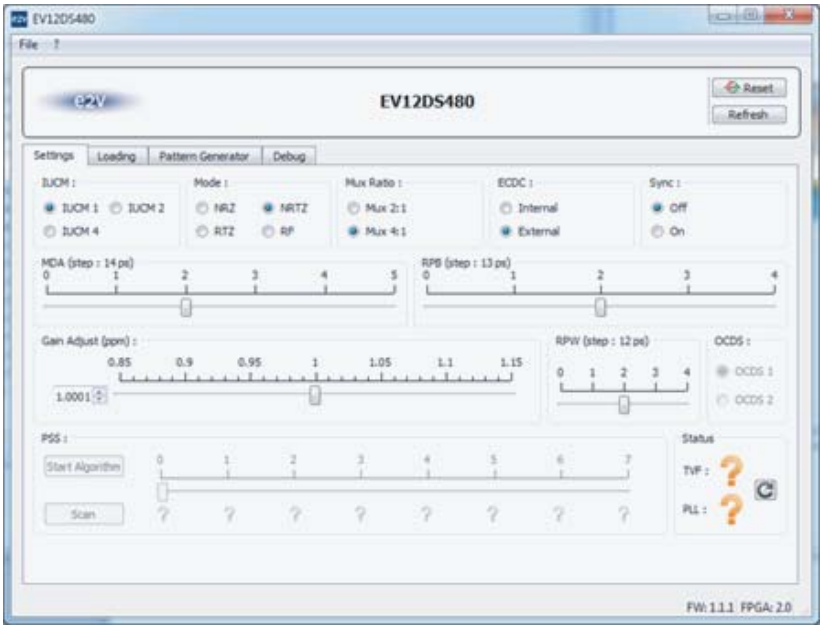
Warning: this installation is done for one USB connector only. If USB connector is changed, USB driver need to be re-installed before use.

4.4 Operating Modes

The DAC software included with the evaluation board provides a graphical user interface to configure the DAC.

4.4.1 Setting

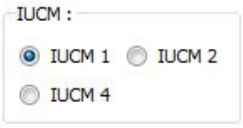
Figure 4-9. Main window



■ **IUCM :**

Two Input Under Clocking Modes have been added to the DAC in order to allow for a specific use where the input data are applied to the DAC at half the nominal rate (or a fourth of the nominal) with respect to the DAC sampling rate. These modes are available for both 4:1 MUX mode and 2:1 MUX mode.

A SYNC should be applied after this function used.



Label	Logic Value	Description	Default setting
IUCM<1:0>	00 or 01	IUCM1 Input Under Clocking Mode inactive	00 (IUCM1)
	10	IUCM2: clock division ratio between DAC core and MUX: 2	
	11	IUCM4: clock division ratio between DAC core and MUX: 4 for test and characterization purpose only	

■ **Mode**:

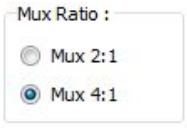
The MODE Function allows choosing between NRZ, NRTZ, RTZ and RF output modes.

Label	Value	Description	Default setting
MODE[1:0]	00	NRZ mode	01 (NRTZ)
	01	Narrow RTZ (a.k.a. NRTZ) mode	
	10	RTZ Mode (50%)	
	11	RF mode	

■ **MUX**:

The software allows choosing between the MUX Ratio 2 to 1 or 4 to 1

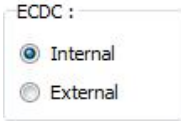
SYNC should be applied after this function used.



Label	Value	Description	Default setting
MUX	0	4:1 mode	0 (4:1MUX mode)
	1	2:1 mode	

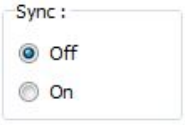
■ **ECDC**:

This function allows choosing the control of PSS and OCDS function. If bit ECDC is internal, pins are controlled by 3WSI. If not, it is directly controlled on board through jumper SW1 to SW4.



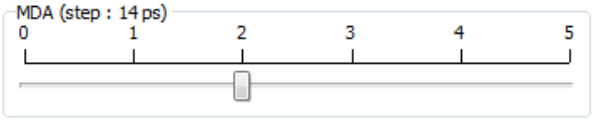
■ **SYNC**:

The SYNC function on GUI allows resetting the DAC. No synchronization is performed with the FPGA. This function has to be used after a modification of OCDS, MUX or IUCM. It is also possible to use external SYNC input (see Section 2.9.4)



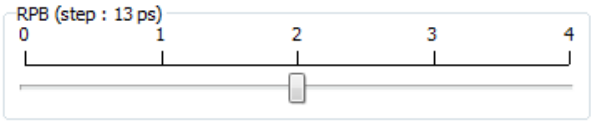
■ **MDA**:

MDA (Multiplexer Delay Adjust) capabilities allow tuning sampling time of the last Master/Slave clock of the MUX. MDA range varies from MDA0 to MDA5 (by steps of 14ps)



■ **RPB**:

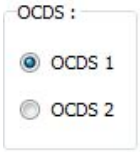
Only available in NRTZ, RTZ and RF mode, this function allows for Reshaping Pulse Begin adjustment. The pulse begin can be tuned from RPB0 to RPB4 (by 13ps steps).



■ **OCDS**:

The software allows changing the DSP clock internal division factor from 1 to 2.

SYNC should be applied after any use of this function:



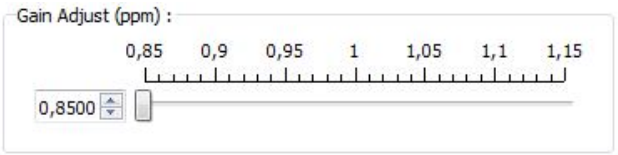
Label	Value	Description	Default setting
OCDS	0	OCDS1 DSP clock = Sampling Clock/(2*MUX ratio*IUCM ratio)	0
	1	OCDS2 DSP clock = Sampling Clock/(2* MUX ratio*IUCM ratio *2)	

■ **GA**:

This function allows you to adjust the internal gain of the DAC so that it can always be equal to unity gain.

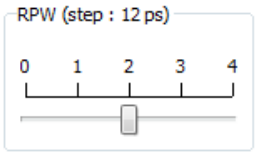
The gain of the DAC can be adjusted by ±11% (1024 steps) by setting the GAIN register through the 3WSI.

GA min is given for GAIN = 0x000 and GA max for GAIN =0x3FF



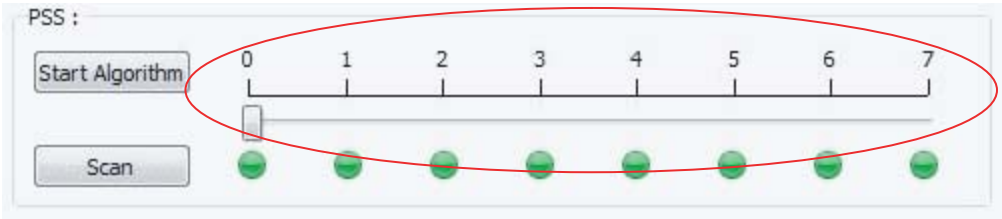
■ **RPW**:

Only available in NRTZ and RF mode, this function allows for Reshaping Pulse Width adjustment. The pulse width can be tuned from RPW0 to RPW4 with 12ps steps in NRTZ mode. Choosing the lower RPW value puts the device in a pseudo-NRZ mode. With higher RPW values, the circuit works near the RTZ mode. In RF mode, the pulse width can be tuned RPW0 to RPW4 with 6ps steps. Figure hereafter shows exemple of NRTZ mode on GUI.



■ **PSS**:

The software allows adjusting the "PSS" (Phase Shift Select) delay to avoid a forbidden timing area between the data input and the clock input.



The led indicators on the GUI depict the status of each PSS position. A green led indicates a functional PSS position. An orange led indicates a forbidden position.

The "Start Algorithm" button scans for PSS positions status and sets the cursor to the optimum position.

The "Scan" button only performs the scan for PSS positions and displays their respective statuses.

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock (Default value)
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycles delay on DSP clock
	101	2.5 input clock cycles delay on DSP clock
	110	3 input clock cycles delay on DSP clock
	111	3.5 input clock cycles delay on DSP clock

■ **Status**:

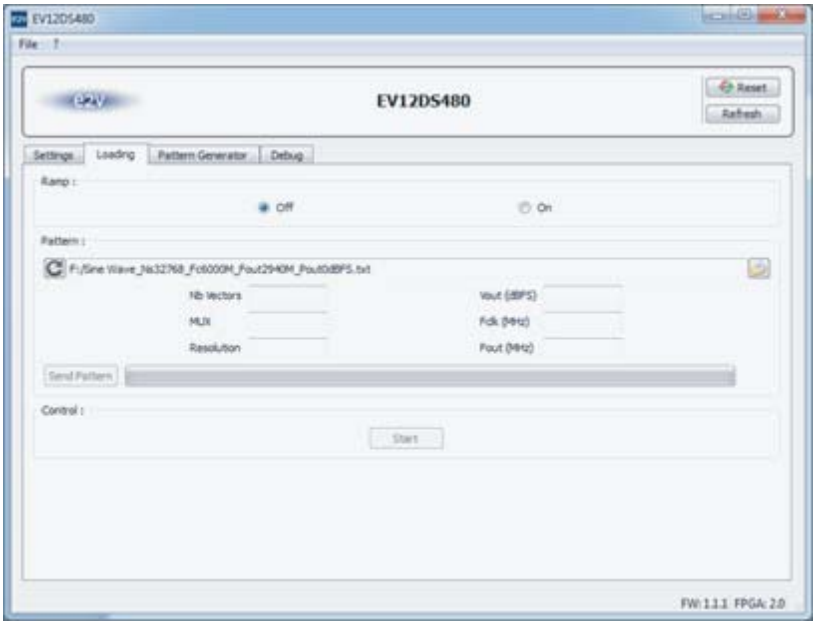
The polling function allows scanning the FPGA to know the FGPA version and the PLL state. They are used to know if the DAC is correctly sampling data transmitted by the FPGA.

4.4.2 Loading

This tab allows sending patterns to the DAC.

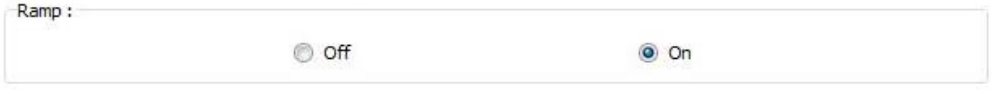
You can choose to send a ramp pattern or to send a dedicated pattern.

Figure 4-10. Pattern loading

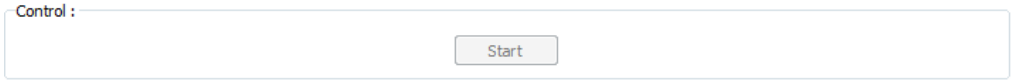


For ramp pattern:

- active "Ramp" ON



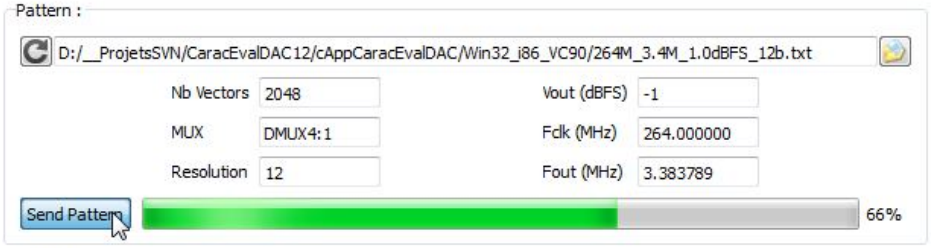
- Press start button in control panel



For dedicated pattern:

- Find the pattern file in the Folders architecture
- Check the information (nb vectors, MUX …)
- Press Send pattern

- Select ECDC in external or internal mode in setting window
- Press start button



Note: the maximum number of vectors is 512k in MUX2 and 256k in MUX4 (total of 1M samples)

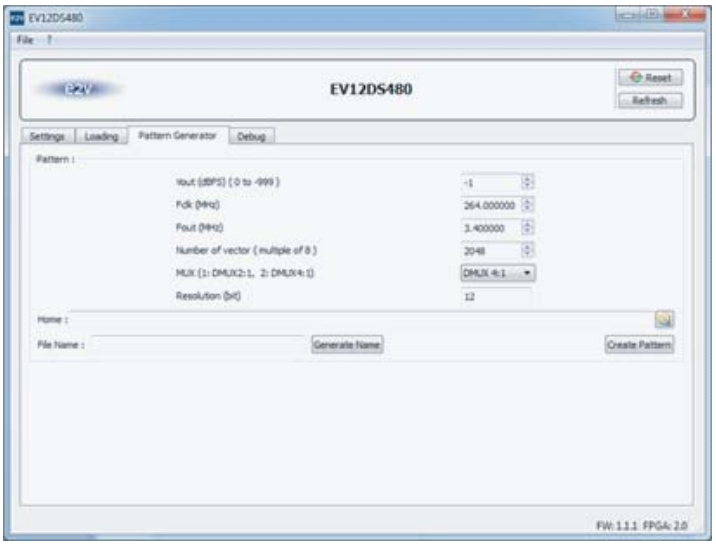
4.4.3 Pattern generator

This tab allows creating sine wave pattern file only.

Pattern generator procedure is the following:

- Fill all information fields.
- Select file directory
- Generate pattern name based on "Generate Name" button
- Create Pattern

Figure 4-11. Pattern generator



If you wish to create your own pattern file, please make sure to follow the syntax described in the example below.

Example of Pattern file

# Vout (dBFS)	0
# Fclk (MHz)	3000
# Fout (MHz)	998.108
# MUX	2 DMUX4:1

```
# Nb vectors                4096
# Resolution (bit)          12
#
Vector 0:    100000000000  111011110001  000100011010  011111100111
Vector 1:    111011111101  000100100111  011111001111  111100001001
Vector 2:    000100110011  011110110110  111100010100  000101000000
Vector 3:    011110011110  111100011111  000101001101  011110000110
Vector 4:    111100101010  000101011011  011101101110  111100110101


Vector 5:    000101101001  011101010101  111101000000  000101110110
……..
…….
Vector 4092:    000011010101  100001110111  111010110011  000011100001
Vector 4093:    100001100100  111010111101  000011101010  100001001011
Vector 4094:    111011001011  000011110101  100000110001  111011011000
Vector 4095:    000100000010  100000011000  111011100101  000100001110
<--
```

4.5 Configuration and software of the FPGA memory

4.5.1 FPGA configuration via JTAG

4.5.1.1 How to load the flash memory

To load the bitstream in the flash, you don't need the whole project fileset, neither the whole Quartus Tools suite.

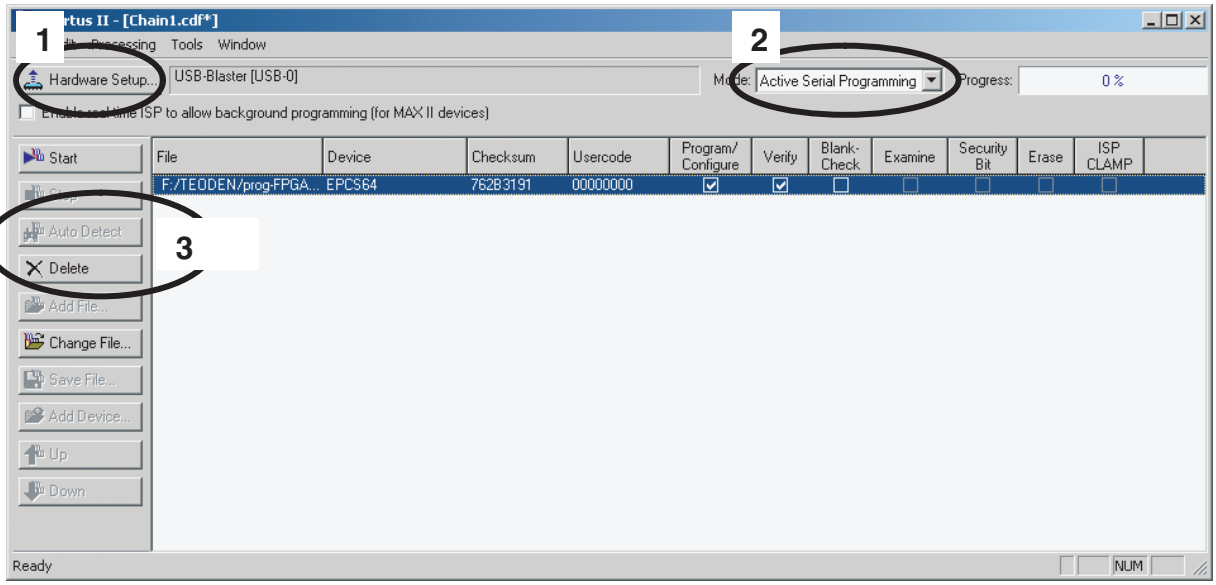
You will need:

- The .jic file
- The Quartus II Programmer (v13.0sp1 or later. Downloadable on Altera's website)
- The Altera USB JTAG probe (USB-blaster)
- The EV12DS4xxZPY-EB board

1. Plug the USB JTAG probe
   (pin 1 is indicated by a line on the Flex and by a square pad on the PCB)
2. Power up the board.

3. Launch the Quartus II Programmer (see Figure 4-12 Quartus II programmer)
   If you can read the name of your probe next to "Hardware Setup..." button go directly to step 4)
   If you read "No Hardware" try step 3)

Figure 4-12. Quartus II programmer

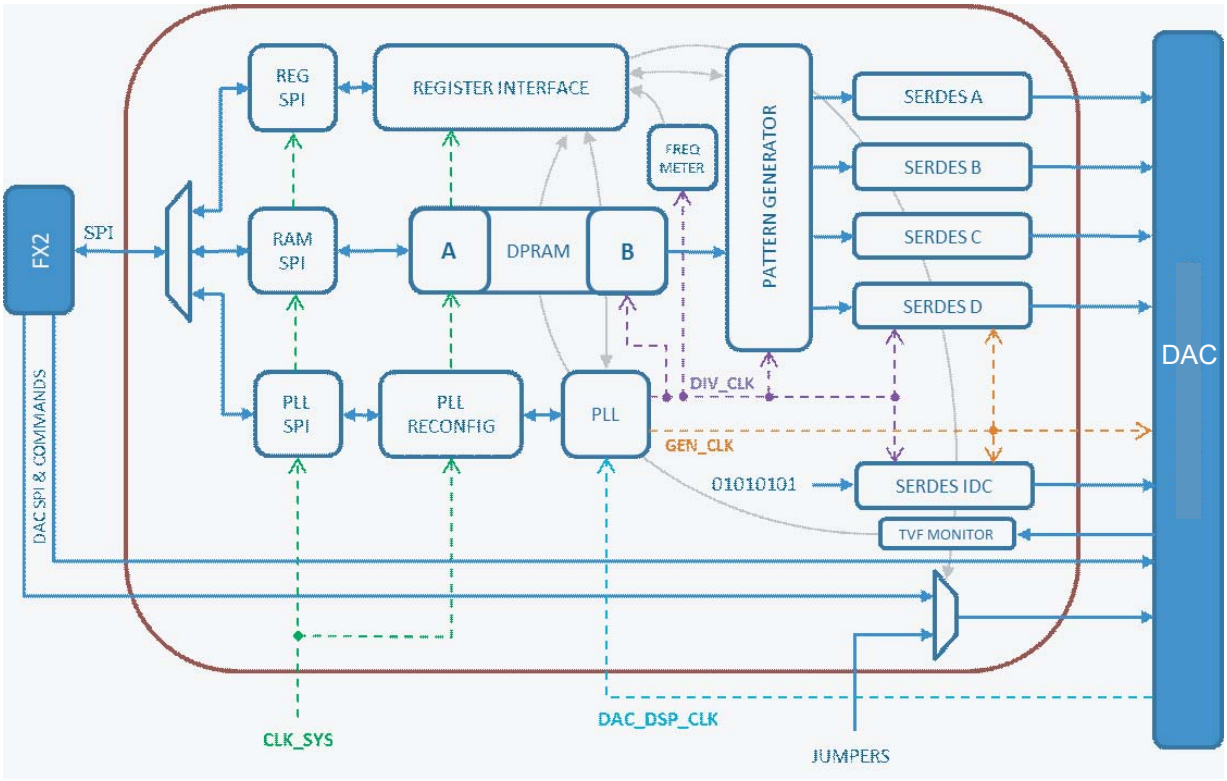


4. Click on the "Hardware Setup..." button (see 1 on Figure 4-12)
   Select your probe in the "Currently selected hardware" drop list
   or double click on the probe name in the "Available hardware items" list.
   If you don't see it, verify all the connections
5. Select the JTAG Mode in the drop list (see 2 on Figure 4-12)
6. Test your JTAG chain with the "Auto detect" button (see 3 on Figure 4-12).
   If the Programmer asks you to confirm the FPGA Reference, choose 5AGXFB3H4
7. Select the FPGA and delete it with the "Delete" button (see 3 on Figure 4-12)
8. Click on "Add File" (see 3 on Figure 4-12).
   Pick up your .jic file.
9. Check the "Program/Configure box of the EPCQ256 line
   A second box should be automatically checked on the FPGA line and a blue "Factory default enhanced SFL image" text should appear
10. Load the flash with the "Start" button (see 3 on Figure 4-12) wait the "Successful" mark next to "Progress:"

4.5.2 FPGA Block Diagram

The following figure represents the block Diagram of the FPGA code:

Figure 4-13. FPGA block diagram



Section 5
Application Information

5.1 Analog Output

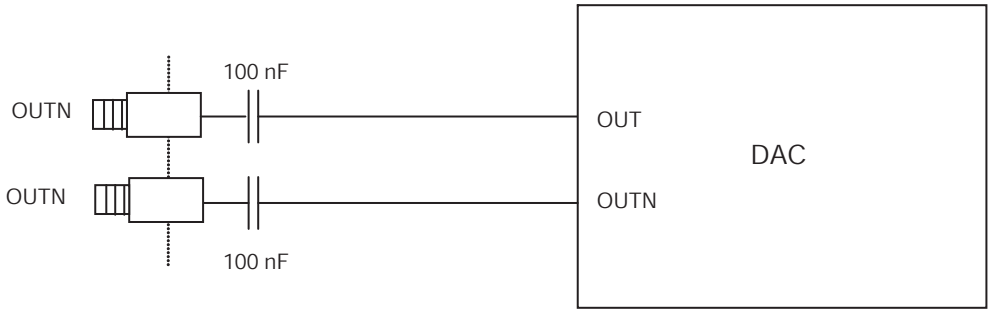
The analog output is a differential AC coupled signal as described in Figure 5-1.

The single-ended operation for the analog output is allowed but it may degrade the DAC performances significantly. It is thus recommended to use a differential configuration via an external balun or differential too single ended amplifier.

Note: References of external baluns:

- Marki BAL-010 200 kHz-10 GHz
- Krytar 4005070 0.5-7 GHz
- Krytar 4060265 6-26.5 GHz
- Hyperlabs HL9404 500 kHz-40 GHz

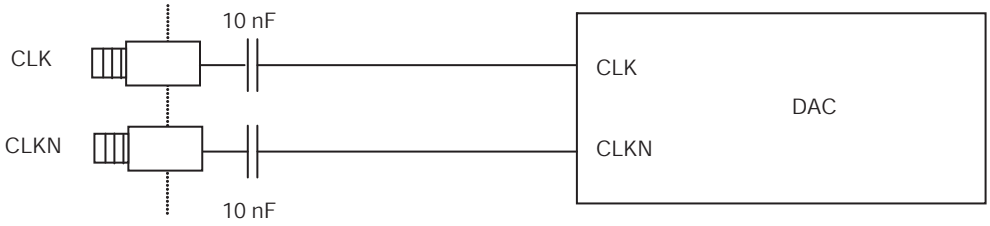
Figure 5-1. Differential analog output implementation



5.2 Clock Input

The clock input can be entered indifferently in single-ended or differential mode with no performance degradation. The clock is AC coupled via 10 nF capacitors as described in Figure 5-2.

Figure 5-2. Clock Input Implementation



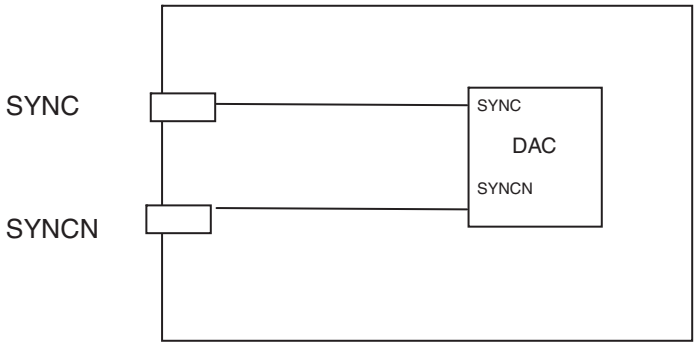
If used in single-ended mode, CLKN should be terminated to ground via a 50Ω resistor. The jitter performance of the clock is crucial to obtain optimum performance from the DAC. We thus recommend using a very low phase noise clock signal.

5.3 SYNC Input

The SYNC, SYNCN is necessary to start the DAC after power up if the power-up sequence described in Section 3.2 is not respected.

The reset signal is implemented as illustrated in Figure 5-3. We recommend applying a square LVDS signal.

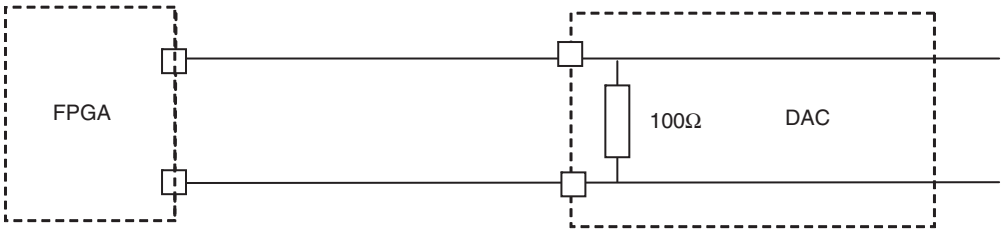
Figure 5-3. SYNC, SYNCN Inputs Implementation



5.4 Input Data

The input data are LVDS and are 100Ω on chip as shown in Figure 5-4 terminated to ground.

Figure 5-4. Output Data On-Board Implementation



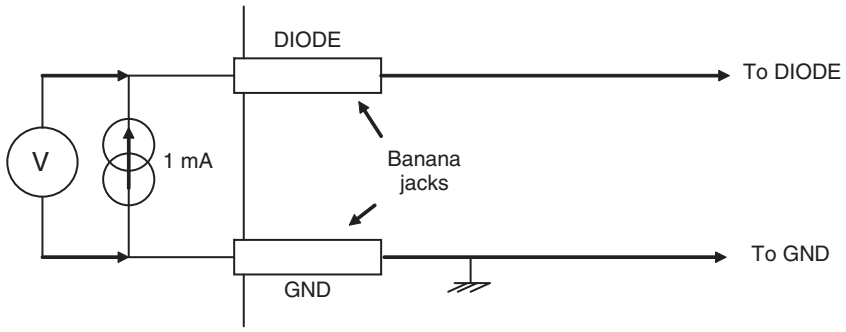
5.5 Diode for Junction Temperature Monitoring

Two 2 mm banana jacks are provided for the die junction temperature monitoring of the DAC.

One banana jack is labeled DIODE and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to GND.

Figure 5-5 describes the setup for the die junction temperature monitoring using a multimeter.

Figure 5-5. Die Temperature monitoring Test Setup



Section 6

Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EV12DS4xxZPY-EB		Ambient	Prototype	Evaluation board

Section 7
Appendix

7.1 EV12DS4xxZPY-EB Electrical Schematics

Figure 7-1. V_{CCD} and V_{CCA3} Power Supplies

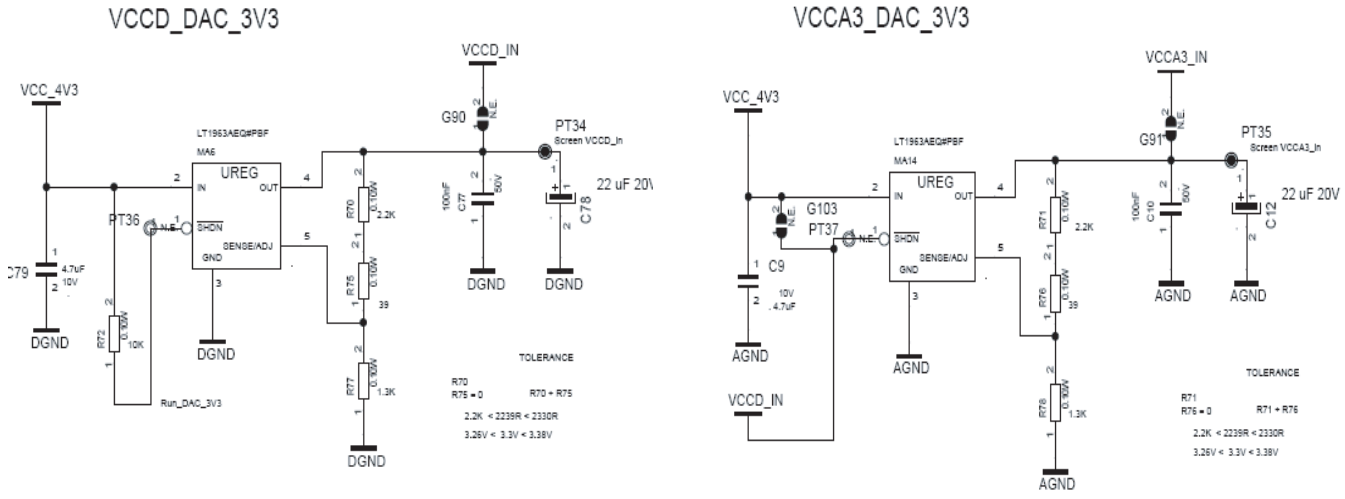
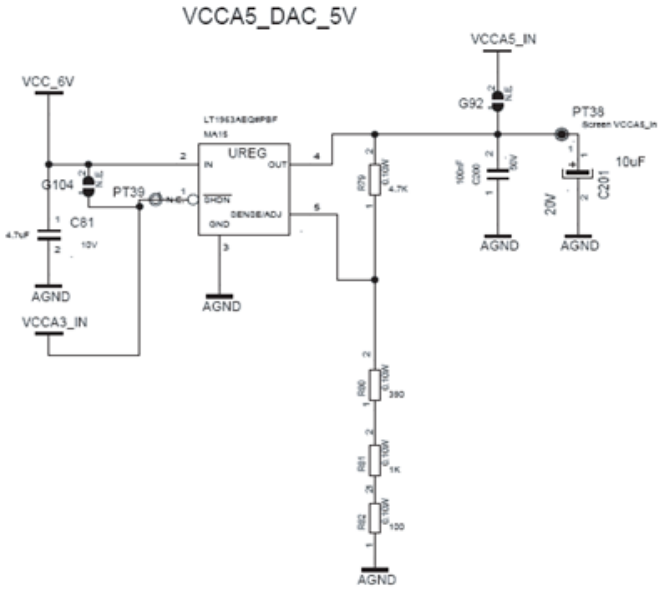


Figure 7-2. V_{CCA5} power supply and general power supply



General power supply

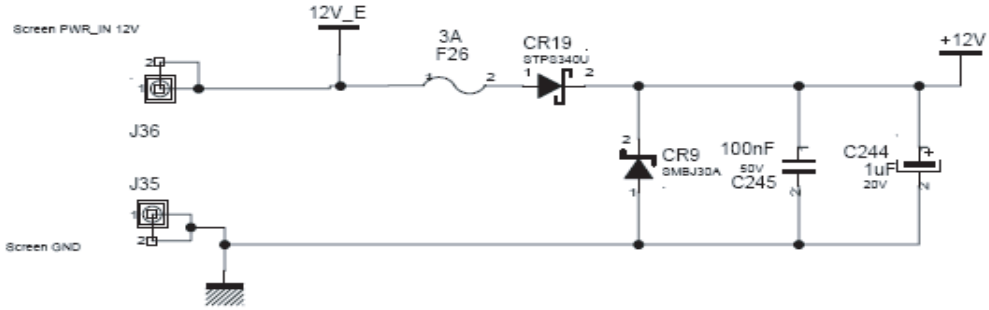


Figure 7-3. Power Supplies Decoupling

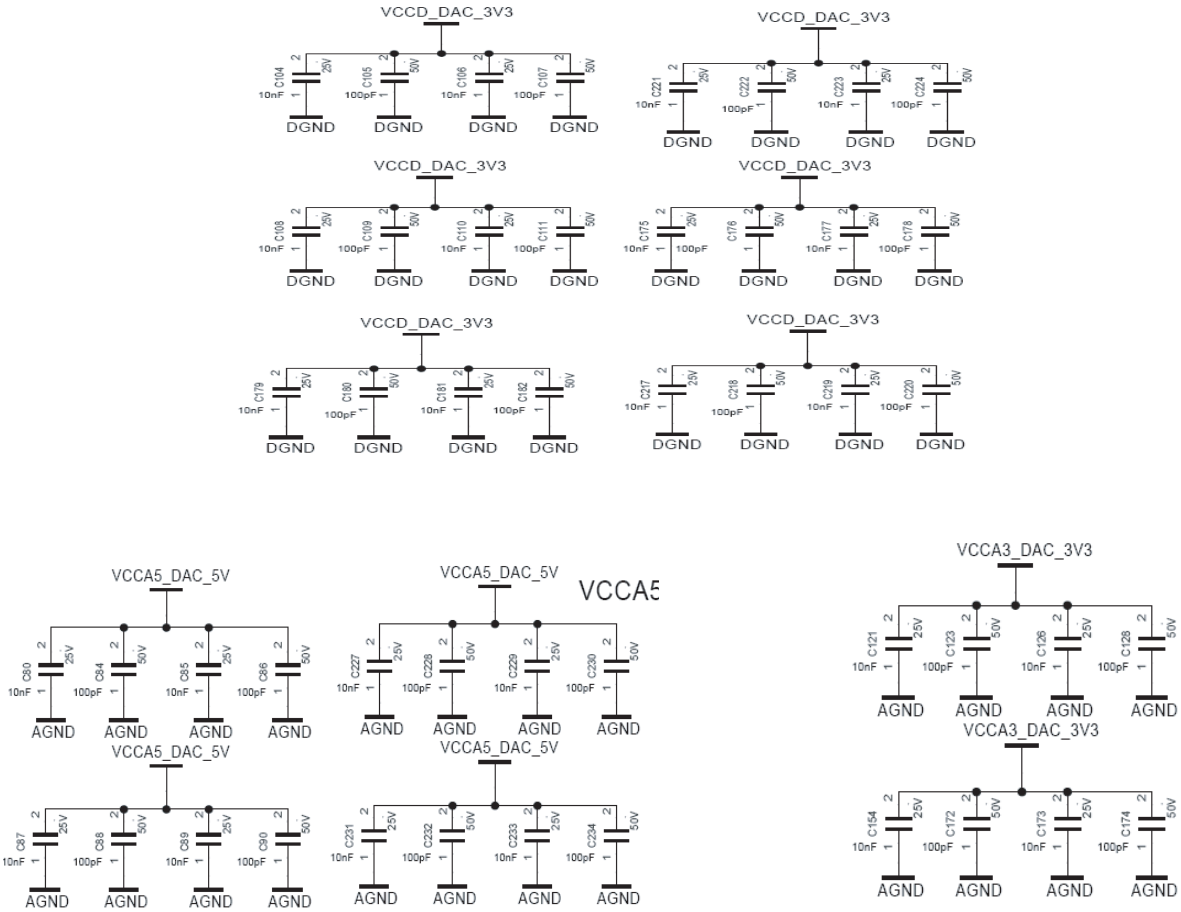
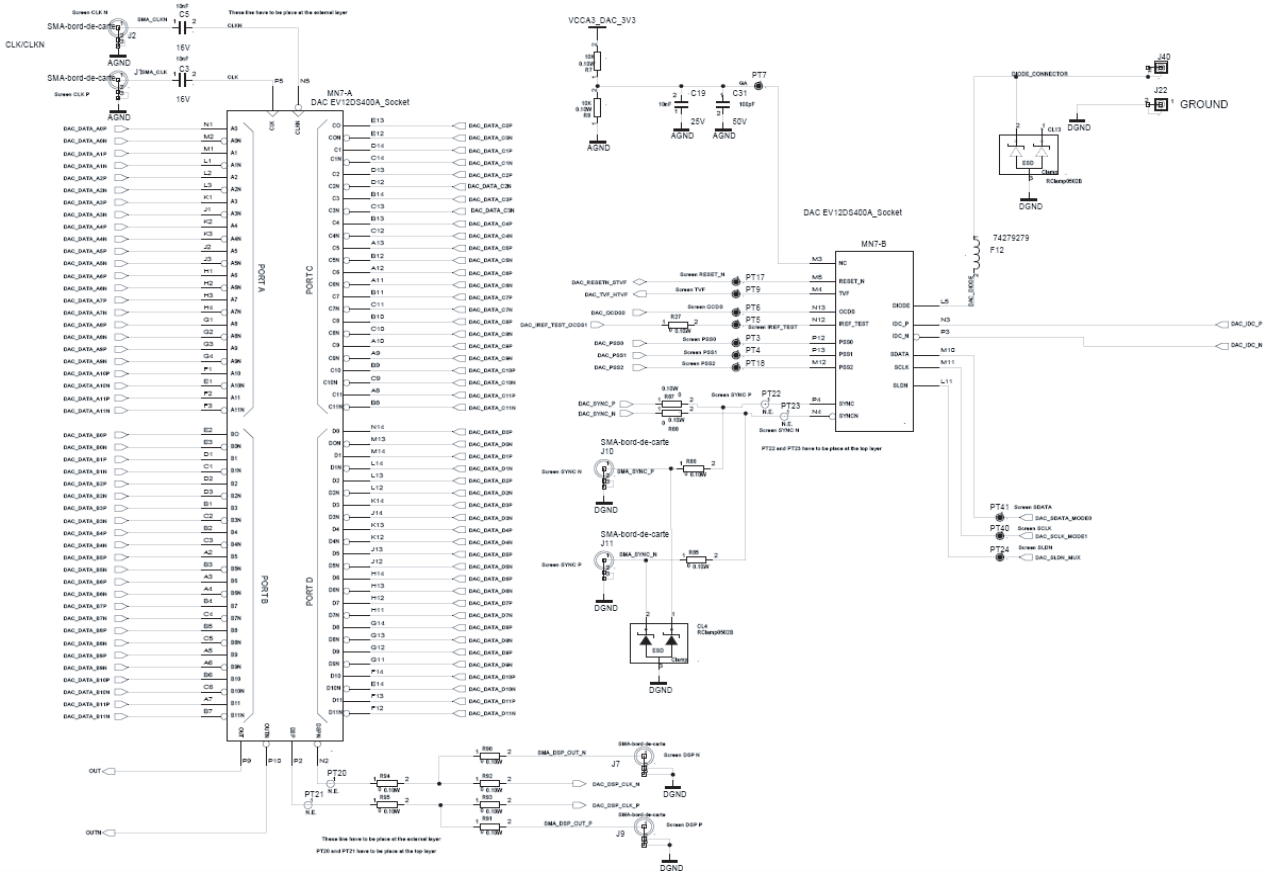


Figure 7-4. Electrical Schematics (DAC)



7.2 EV12DS4xxZPY-EB Board Layers

Figure 7-5. Top Layer

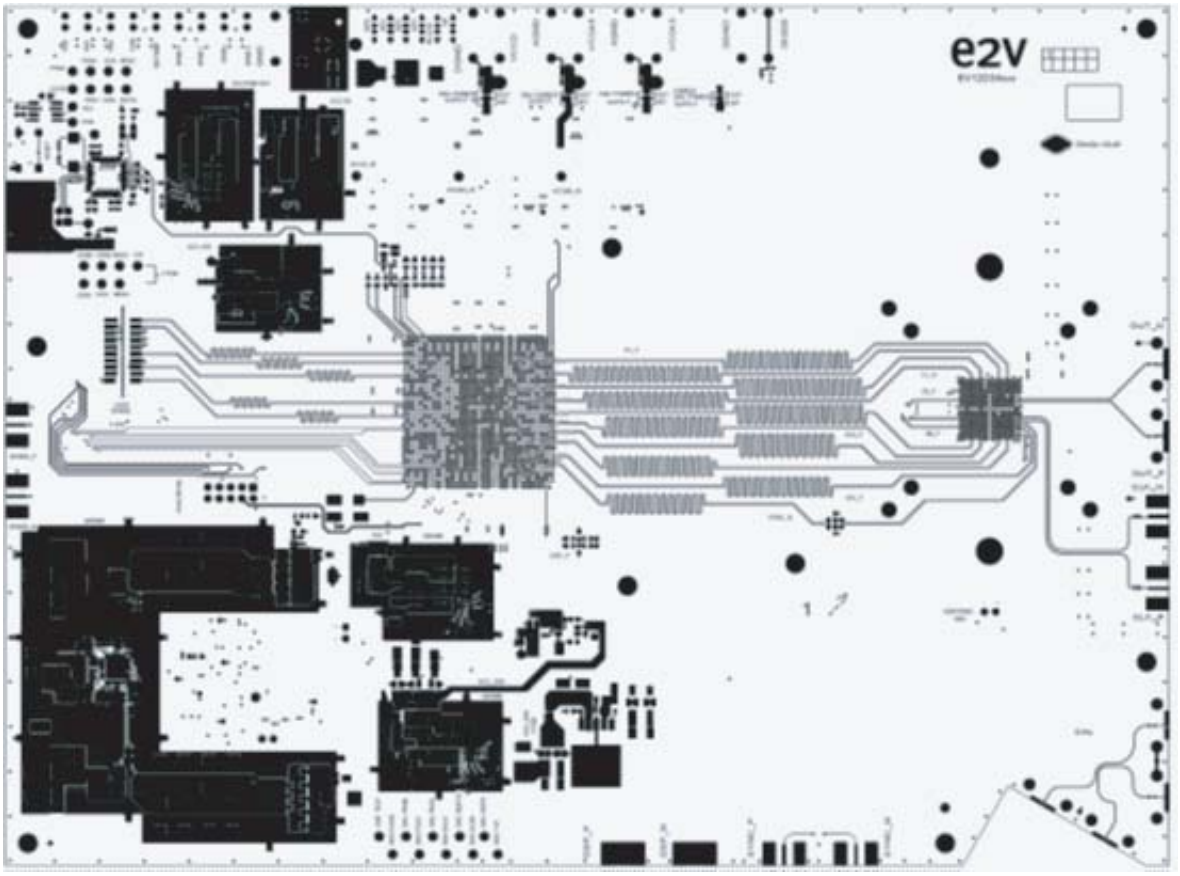


Figure 7-6. Bottom Layer