Design secrets behind the world's first K-band DAC

A white paper by Marc Wingender, Romain Pilard (PhD) and Julien Duvernay (PhD)

This article covers specific design choices in the creation of the world's first K-band data converter, the EV12DS460A, explaining that by avoiding established CMOS design principles and applying an ultra-high speed process, new capabilities can emerge. It also covers how a compact, single-core quantizer coupled with careful design choices leads to the breakthrough performance the EV12DS460A boasts. Lastly, you'll discover how subtleties in layout and circuit simplifications are dominant design considerations.

Introduction

Microwave system designers are constantly on the look out to improve performance and attain higher operating bandwidths. Design simplification and the reduction of power, size and weight are also desirable. Many component developments have emerged over the last few years that help. However, few of these have the potential impact of a new digital-to-analog converter (DAC), the EV12DS460A. Indeed, the novel DAC claims to place complex bandwidth across a huge spectral range that includes the microwave K-band out to 26.5 GHz.

Initial details of a prototype monolithic microwave IC (MMIC) emerged during last year's European Microwave IC conference. Early indications showed a product capable of turning in solid X-band performance (8 to 12 GHz). Subsequently, detailed wide-band testing revealed that this DAC is capable of lot more than that. The part operates across eight Nyquist zones with a low noise floor and minimal spurious signal generation.

The story here is of a device providing an early glimpse of a future where software defined microwave systems (SDeMS) become a reality. But in getting there, two obvious questions arise:

- What techniques were used to enable such stand-out performance?
- How good is this DAC when tested?

This article shows that by eschewing established CMOS design principles and applying an ultra-high speed process, that new capabilities emerge and how a compact, single-core quantizer coupled with careful design choices leads to breakthrough performance. You'll discover how subtleties in layout and circuit simplifications are dominant design considerations. First up, let's dip into the high-level architectural choices made.

High level design

Two factors determine the achievable performance namely:

- Basic architecture and
- Speed of the process technology

Most high-speed DAC designs time interleave several cores to boost sample rate. However, their challenge comes in reconstructing the output signal. It's hard to avoid spurious signal generation and the resultant dynamic degradation. The operation of interleaved DACs is not discussed here as their generally poor SFDR is the reason that an alternative segmented architecture was chosen for the described DAC.

Segmented design

Explaining basic DAC operation normally starts with the idea that a series of binary weighted current sources can be switched into a summing amplifier. Each 'power of 2' element is enabled or not, dependent on its relative bit position. The beauty of this implementation is simplicity and the limited number of elements (1 per bit) needed. In practice, its nigh impossible to scale sources linearly much beyond 8-bits.

Architecturally, there is one further simplification to help the quantizer core design. By adopting a hybrid segmented arrangement illustrated (fig 1). The segmented DAC divides the conversion task between an *m-bit* thermometer coding section and a second *(n-m)-bit* binary weighted section, handling fine (LSB) resolution. A time delay accounts for the thermometer encoding process after which the outputs from these two segments are summed for the final multi-bit result.

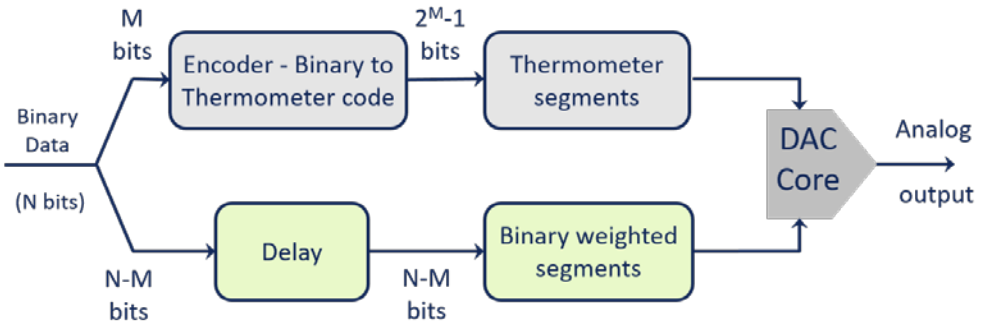


Figure 1: The hybrid segment DAC architecture of the EV12DS460A

As noted previously, attaining better than 8-bit linearity is a hard-won battle, but by dividing a multiple bit convertor up into most significant (MSB) and least significant bit (LSB) segments minimizes matching and lowers core complexity. With careful design, it is possible to construct both the thermometer and binary weighted segments from identical switches, resistors and current sources.

Single core simplicity

Delivering good static accuracy is the starting point for any convertor design, in the hybrid-segmented approach, precision is defined by the tolerances achievable in the binary weighted LSB section.

A design goal was to deliver high SFDR and avoid calibration, mandating the achievement of better than 0.5 LSB matching. Three potential quantizer configurations were considered:

1. 2-bit thermometer (= 3 segments) with 10-bit weighted segments = 13 segments
2. 3-bit thermometer (= 7 segments) with 9-bit weighted segments = 16 segments
3. 4-bit thermometer (= 15 segments) with 8-bit weighted segments = 23 segments

Initial inspection suggests option 1 is the obvious design choice; it promises the lowest number of segments and hence the smallest core area. However, its static accuracy lets it down. To understand this, consider that a 12-bit quantizer able to output a full-scale 1 volt peak to peak implies a LSB quantization voltage of 244 µV (1Vp-p/4096). Simulation shows that the matching achievable with 9-bit weighted segments is 125 µV. That's 2x better than this (i.e. 0.5 LSB at 12-bits) which guarantees monotonic DAC operation. However, with the 'obvious' 10-bit weighted option, it is not possible to improve matching, 125 µV is the physical process limit, thus option 1 is unviable. Simulation also eliminated the third option as it is compromised by the excessive dynamic loading it places on the clock buffer.

Process technology

Designing the DAC eschewed standard CMOS processes in favor of taking the path less trodden. This philosophy exploits controlling the raw speed of a heterojunction silicon-germanium carbon (SiGeC) bipolar process sourced from Infineon[1]. By introducing carbon inside the intrinsic base of the NPN bipolar transistors, the B7HF200 process allows for a thin and highly doped base. It is a key element to achieve a high transition frequency (Ft of 200 GHz) and a low base resistance, two parameters on which the DAC's performance strongly relies.

[1] J.Böck, H.Schäfer, K.Aufinger, R.Stengl, S.Boguth, R.Schreiter, M.Rest, H.Knapp, M.Wurzer, W.Perndl, T.Böttner, and T.F. Meister. "SiGe bipolar technology for automotive radar applications" in Proc. Bipolar/BiCmos Circuits and Technology Meeting (BCTM),Montreal, Canada, Sep. 2004, pp.265-268

This process has served high speed and mm-wave applications well for nearly a decade now and is applied in several solid-state microwave components.

		UHS npn	HS npn	HV npn
Transit frequency	f_T	200 GHz	180 GHz	40 GHz
Max. frequency of oscillation	f_{max}	250 GHz	250 GHz	120 GHz
Base-collector capacitance	C_{BC}	5.8 fF	5.2 fF	3.5 fF
Breakdown voltage	BV_{CE0}	1.6 V	1.7 V	4.0 V
Breakdown voltage	BV_{CB0}	5.8 V	6.5 V	15 V

Figure 2: Comparison of B7HF200 transistor types

B7HF200's speed is further enhanced by the provision of four layers of copper metal suitable for low current density interconnects. Copper helps minimize undesirable circuit parasitics, the bane of high speed designers.

DAC design secrets

Designers did not achieve the blistering speed of the EV12DS460A in a single serendipitous leap. Its architecture evolved over several generations since the introduction of a slower 12-bitter in 2011[2]. Even that earlier part demonstrated world-class performance; generating a 1.5 GHz bandwidth.

The design journey is focused on three general design principles:

- Driving the quantizer's dynamic load & reducing trace length
- Guaranteeing stable operation
- Output pulse reshaping to curtail distortion & extend performance

Driving the quantizer's dynamic load

The quantizer's design is partially reproduced (fig 3). On the right is the quantizer comprising 16 segments, whilst on the left, is the analog circuitry of the sample clock system. Lumped together, bridging the two halves of the circuit are parasitics that arise from on chip traces and represented here by Lp and Cp.

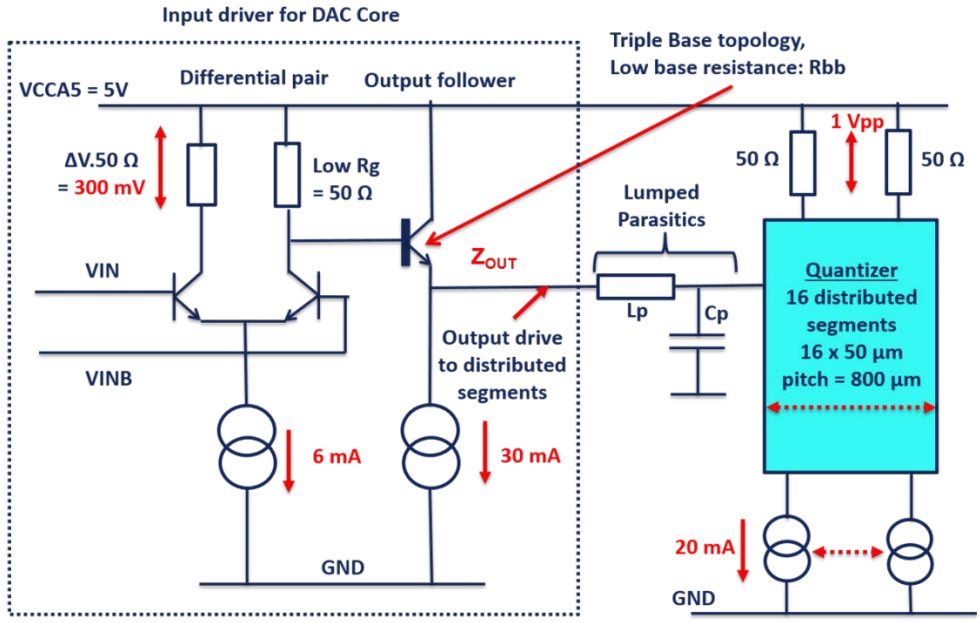


Figure 3: Simplified input driver for EV12DS460A

[2] François Boré, Marc Wingender, Nicolas Chantier, Andrew Glascott-Jones, Emmanuel Dumaine, Carine Lambert, Sergio Calais. "3 GS/s 7GHz BW 12 Bit MuxDAC for Direct Microwave Signal Generation over L, S or C Bands" in Proc. COMCAS, Tel Aviv, Nov 2011

To support sampling at 6 to 7 GSps, it is important to have a low jitter clock source with ultra-fast transitions. At 6 GSps the clock period is only 166 ps. Ensuring clean, rapid transitions is paramount to enable fast quantizer settling and thus sampling. However, the relatively high, full-scale quantizer current is set at 20 mA in this design. To drive this quickly, demands a sophisticated driver comprising the differential pair and output follower circuit which features extremely low output impedance.

For such a driver circuit, the output impedance Zout can be expressed as:

Zout = $(1/g_m + R_{bb} + R_g)/Beta(f)$, where g_m is the transistor transconductance ($1/g_m$=1,25 ohms), R_{bb} is the follower output resistance, R_g the output resistance of the differential pair and Beta(f) is the dynamic current gain of the transistors versus frequency.

Considering the B7HF200 process characteristics (cutoff frequency f_T = 200 GHz), the current gain Beta(f) at 20 GHz is equal to 10. Also, the very low bipolar transistor intrinsic base resistance delivers an R_{bb} in triple base configuration of 25 ohms.

R_g should also be minimized as much as practical with the constraint of maintaining a sufficient value to avoid increasing the bias current too much and consequently the power consumption. A value of roughly 50 ohms was obtained.

Finally, a first order estimate for driver output impedance is: Zout = (1.25 + 25 + 50)/10 = ~ 7.5 ohms. This low output impedance is a key element for fast operation.

Maintaining a 300 mV pulse amplitude at the output buffer demands driving 300 mV across 50 ohm termination (300 mV/50 = 6 mA). Further improvements in R_g make only modest impedance improvements at a cost of higher power consumption. Halving R_g, the bias current must rise to 12 mA.

Minimized trace lengths and guaranteed DAC stability

Back to the importance of trace length and its impact on parasitics in high-speed design; each quantizer segment of the described design is only 50 µm wide, so its modest sixteen segments combine to form a total signal trace length of 800 µm (16 x 50 µm), any reduction in pitch is therefore helpful.

The EV12DS460A's global time constant can be factored from three contributors:

1. The dynamic load capacitance (C_L) estimated at 0.5 pF (C_L=g_m.T_f with g_m = ΔI/ΔV = ~ 20mA/25mV and T_f the transistor forward transit time = 0,8 ps)
2. The passive parasitic capacitance(C_P) of the metal signal trace estimated at 0.5 pF
3. The passive parasitic inductance (L_P) of the metal trace estimated at 50 pH

Under worst case conditions, the global time constant ΣT can be calculated as follows:

ΣT = Zout.C_L + Zout.C_P + L_P/Zout, so ΣT = 7.5 Ω. 0.5 pF + 7.5 Ω.500 fF + 50 pH/7.5 Ω = 3.75 ps + 3.75 ps + 6.66 ps = ~**14 ps**

This time constant correlates well with measured DAC data of 35 ps rise and fall times (t_r/t_f). Furthermore, at this level, t_r/t_f individually represent less than 20% of the total sample clock period (of 166 ps) giving fast enough clock edges to support a first order bandwidth approximation of 10 GHz, hitting the DAC's design goal.

Beyond this first order assessment, some special damping techniques were used to ensure dynamic stability within the DAC. Maximum overshoot (+4%) and minimal ring back (-2%) were achieved. Certainly, the fact that the B7HF200 process offers low sheet resistance, copper metallization helps further tweak and damp critical chip nodes. The performance of the resulting exceptionally clean, 6 GHz sampling is illustrated in the step response (fig 4).

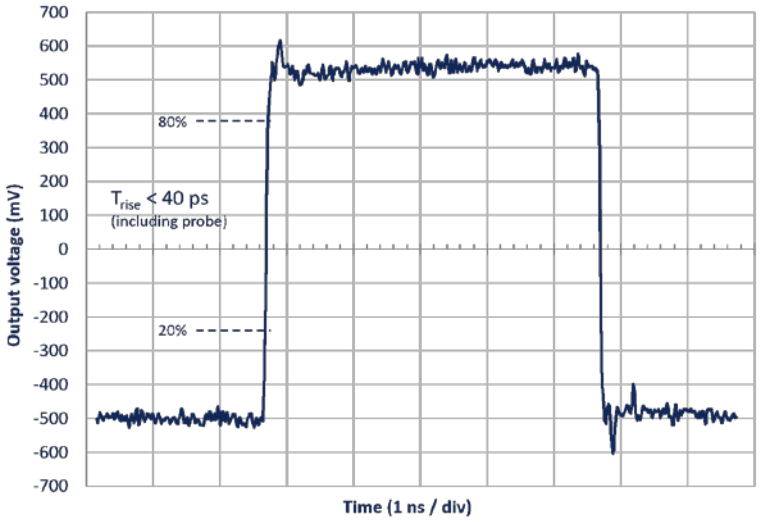


Figure 4: Step response shows 30 ps rise time once adjusted for scope probe loading

Dynamic enhancement through output pulse shaping

Four output pulse shaping modes (NRZ, NRTZ, RTZ, RF) are provided to give system designers freedom to tailor the DAC's dynamic response to specific output frequency bands, thus facilitating frequency planning. Most quantizer distortion can be tracked down to switching transitions. Any switching glitches are ultimately superimposed on the output signal (fig 5), however if these glitches can be removed, then the output spectral purity benefits.

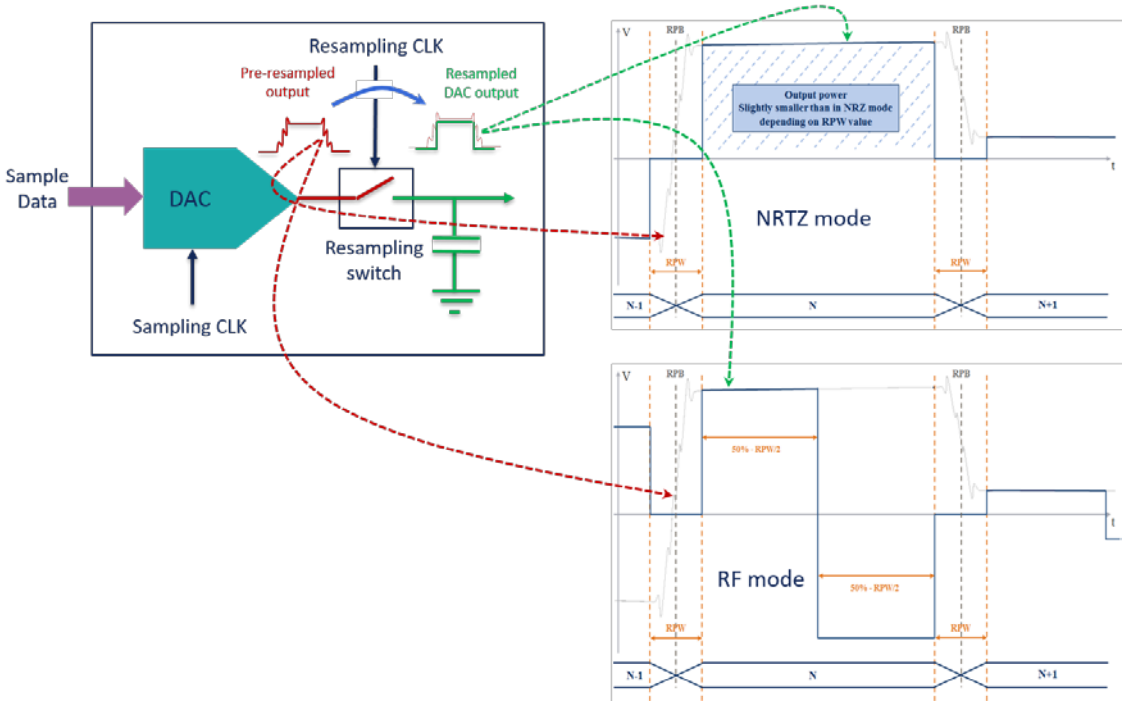


Figure 5: DAC pulse shaping: Concept diagram and expanded waveform with NRTZ and RF output modes

This is achieved in the pulse shaped trace above, by forcing a return to zero ahead of each edge transition, visible here for both the NRTZ and RF modes. Pulse shaping is programmed via a 3-wire serial interface with two user shaping controls, the re-shaping pulse width (RPW) and pulse centering (RPB). The pulse center must coincide with the center of the transition edge if all glitch energy is to be removed. Note that this technique sacrifices a small amount of output signal power (equivalent to the area defined by RPW).

Characteristic curves (fig 6) illustrate the benefits of pulse shaping. This data shows the frequency spectrum across eight Nyquist zones out to 27 GHz (for both fs = 6 & 7 GSps) at two RPW settings. Note that increasing sample rate noticeably expands the typical SINC (sin(x)/x) DAC output characteristic.

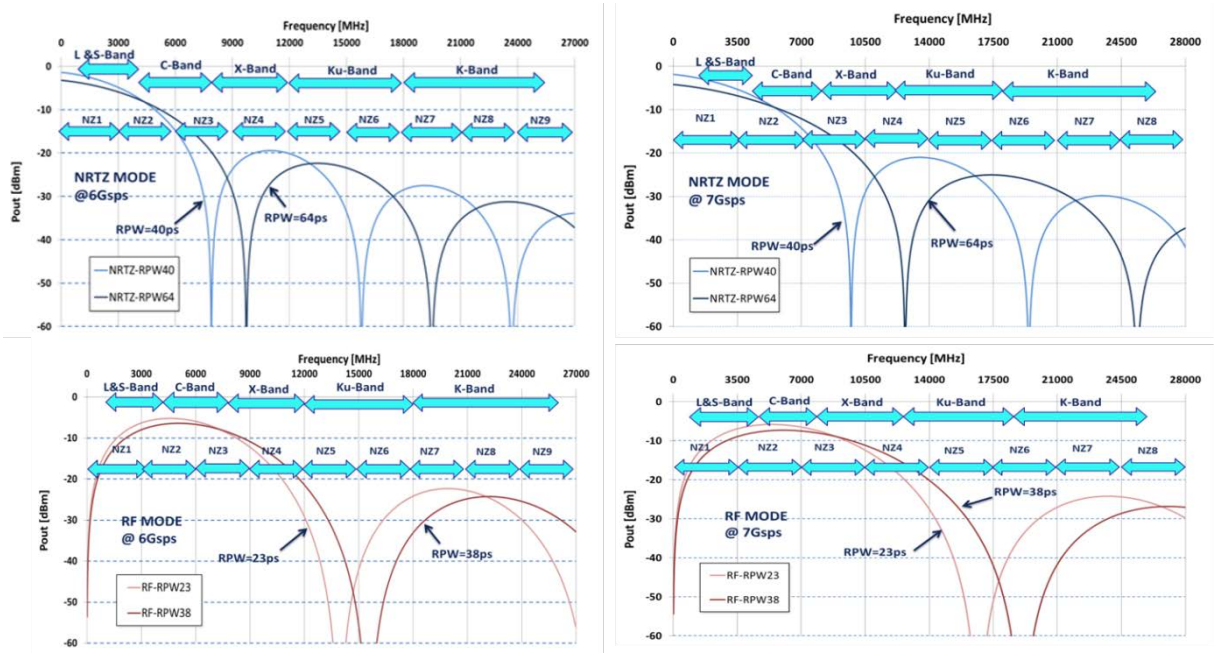


Figure 6: Effect on DAC output power spectrum of EV12DS460 in two pulse shaping modes (sampling at 6/7Gsps)

Up to + 12 dB improvement in harmonics levels is shown for the third harmonic due to reshaping (H3 improved from -57 dBm to -69 dBm), stretching the DAC's 'reach'. To further emphasize this, the following spectra (fig 7) has been produced at 6 Gsps with Fout = 2940 MHz, both with (NRTZ mode) and without reshaping (NRZ mode). In NRTZ mode, the benefit of re-shaping is clearly visible.

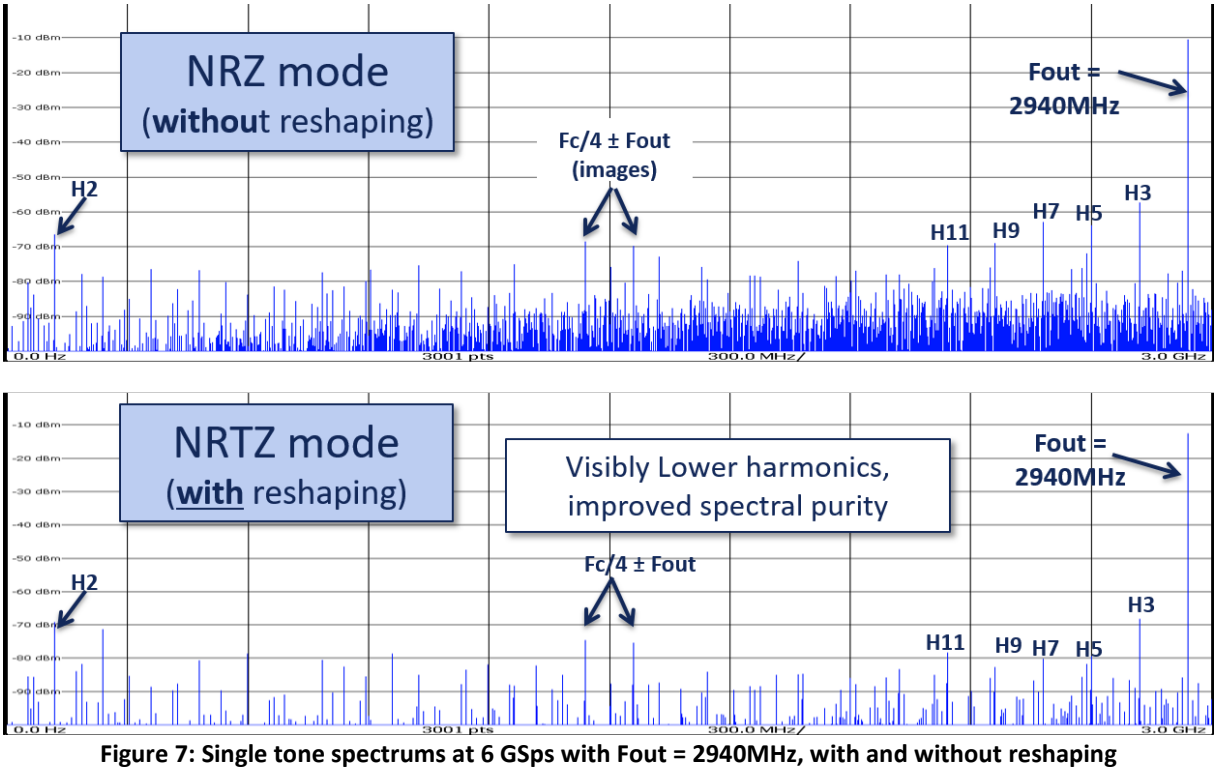
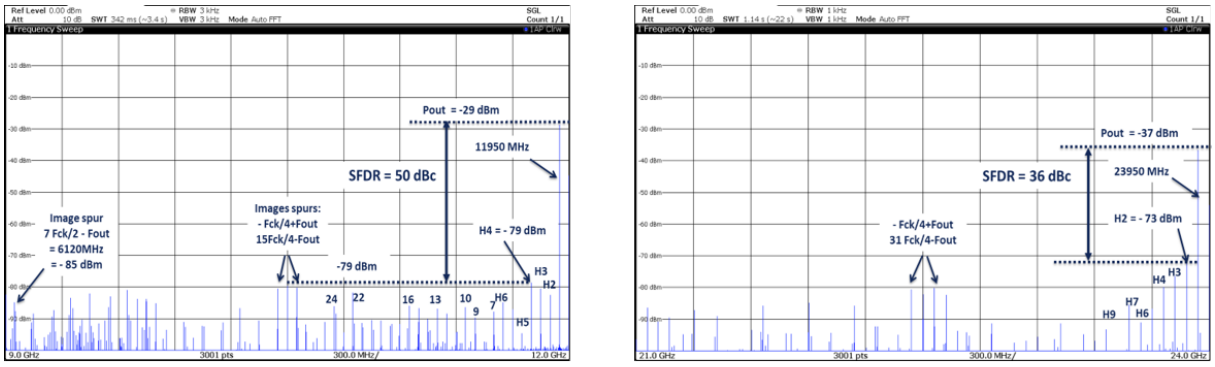


Figure 7: Single tone spectrums at 6 GSps with Fout = 2940MHz, with and without reshaping

Measured Performance

Output 3 dB bandwidth extends up to 7 GHz, with a guaranteed sample rate of 6 GSps enabling the generation of a 3 GHz wide, complex bandwidth. Usable output power is clearly visible in the X-band (fig 8a). The curve shows a single tone carrier at 11950 MHz with a SFDR of 50 dBc in the 4th Nyquist zone. Here the 4th harmonic dominates SFDR. This carrier frequency was carefully selected to lie on the edge of the X-band allowing many of the harmonic signals to be easily spotted as they occur in their natural harmonic order.

Increasing carrier frequency into the K-band (fig 8), with a signal reference now set at 23950 MHz in the 8th Nyquist zone, the 2nd harmonic dominates SFDR (-36.5 dBc). Again, a clean progression of harmonics is visible.



a. b.

Figure 8: SFDR at 11950 MHz and 23950 MHz

Other performance characteristics standout from these two curves, both plots show non-harmonic spurs at the mid-frequency point. These spurs can be traced back to insufficient crossover signal rejection within the DAC's 4:1 input multiplexer. Even so, the spurs peak at -80 dBm, a very respectable level. The DAC's noise floor is measured at close to -110 dBm.

Testing data convertor products with single or multi-tones is easily arranged in the lab. Judging the capability of a DAC on the strength of these tests, only partly tells the story. Today's digital communication systems deploy complex modulation on large chunks of bandwidth, and so a more representative broadband test is desirable. That's where noise o power ratio (NPR) testing helps; it exercises a DAC across a wide bandwidth and can gauge how a signal comprising of many incoherent and narrow band tones, interact and interfere with one another when mixed by the DAC. A DAC with an NPR closely matching the ideal NPR of an n-bit device is clearly a desirable broadband component.

The NPR test is usually performed using a digital pattern with a Gaussian noise power density. A (digital) notch filter is applied to the pattern in the frequency domain to give a 'quiet' zone within the bandwidth of interest. The pattern is sent to the DAC and the NPR performance is calculated as the ratio of average magnitudes of power densities measured both within and outside the notch. For an ideal DAC, the signal power within the notch is related to quantization noise only. For a real DAC, the quantization noise is combined with DAC thermal and voltage noise induced by clock jitter, (output referred) plus intermodulation products due to any cross-channel interferers.

Broadband NPR for this part is shown below (fig 9). Sampling at 7 GSps allows the generation of 3.150 GHz wide synthetic bandwidth. The resultant NPR is 42.6 dB, equivalent to an 8.6 effective number of bits (ENOB). Note the considerable NPR flatness out to 3325 MHz.

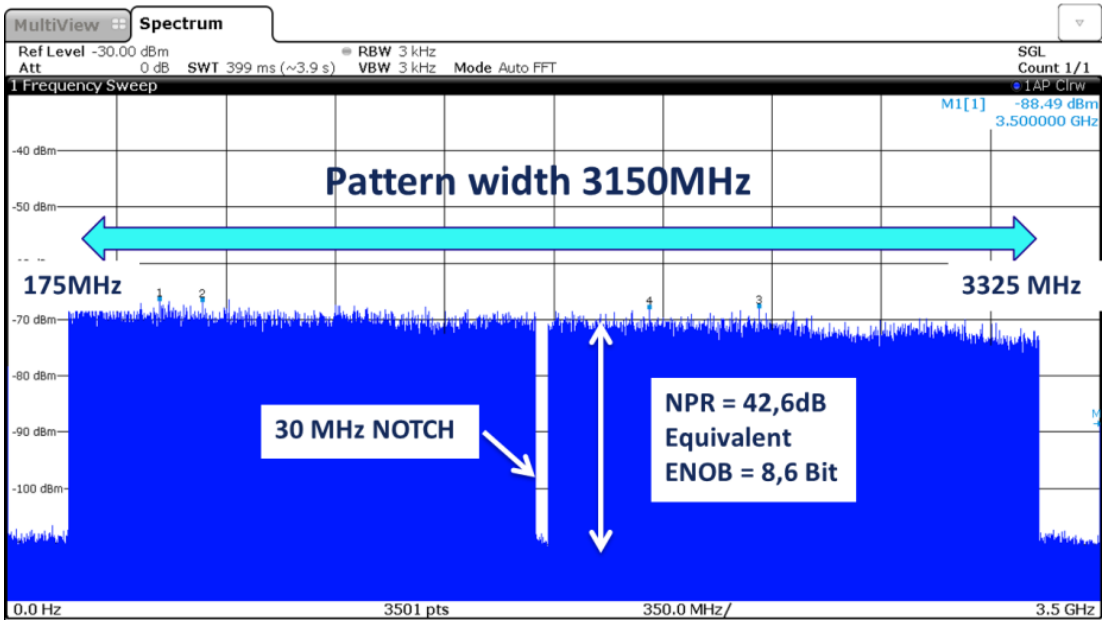


Figure 9: Broadband NPR for 3.15 GHz bandwidth signal with a 30 MHz notch

The second NPR characteristic (fig 10) replicates a 3.150/2.700 GHz NPR pattern across + 22 GHz using 7/6 GSps sampling with the DAC operating in RF mode. This graph pair helps to highlight one of the benefits of increased sample rate. Not only does it impact the maximum bandwidth generation capability of a DAC, but it expands the SINC characteristic and the output power available in high order Nyquist zones.

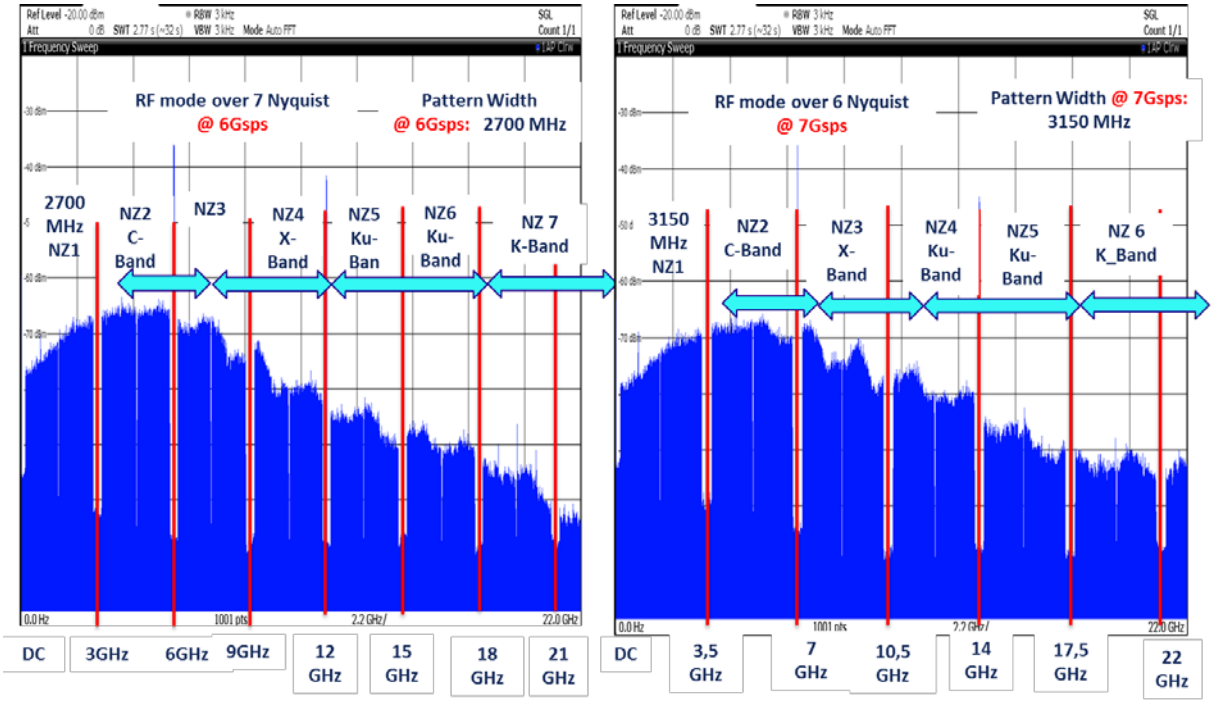


Figure 10: Repeated NPR patterns at 6 & 7 GSps over multiple Nyquist zones – K-band NPR uplift at 7 GSps clearly visible

Other state-of-the-art DACs

Texas Instruments recently described a 14-bit 8.9 GSps RF DAC using 40 nm CMOS process supporting 4G LTE applications. It features an SFDR of 50 dBc at 8.9 GSps (Fout = 4300 MHz) [3]. Although the DAC is capable of sampling at 8.9 GSps, no measurement results are available for frequencies above 4300 MHz excluding it from most microwave bands.

Another development is Analog Devices' 11/16-Bit, 12 GSps DACs (the AD9161/AD9162). The AD9161/62 specifies sampling rate at 12 GSps in RF mode (also called mixed mode). In RF mode, since data is inverted every half a clock period, it looks like the DAC is sampling at 12 GSps. For the EV12DS460A operating in RF (see Fig. 5), the Data inversion is not considered in the specified sampling rate (6 GSps). Therefore, the EV12DS460A and AD9161/62 are strictly equivalent in terms of sampling rate. This is validated by the fact that for all, the instantaneous bandwidth is 3 GHz.

Both Analog Devices parts feature excellent SFDR across the first two Nyquist zones of 65 dBc (Fclock = 5 GSps, Fout = 4000 MHz). Unfortunately, performance collapses at frequencies above 7500 MHz. Output power rolls off to -66 dBm (Fout = 7500 MHz) preventing them doing useful work in X and K-bands.

Final thoughts

With the arrival of the EV12DS460A, microwave engineers now have a practical broad-band DAC capable of projecting complex bandwidth from DC all the way into the K-band frequency. Certainly, the device is not the only giga-sample DAC available, but as shown here, it is the first one capable of projecting large synthetic bandwidth into higher Nyquist zones whilst maintaining good spectral purity. It opens a realm of exciting and innovative possibilities for new mm-wave applications.

References

From Infineon:

(1) J.Böck, H.Schäfer, K.Aufinger, R.Stengl, S.Boguth, R.Schreiter, M.Rest, H.Knapp, M.Wurzer, W.Perndl, T.Böttner, and T.F. Meister, "SiGe bipolar technology for automotive radar applications" in Proc. Bipolar/BiCmos Circuits and Technology Meeting (BCTM), Montreal, Canada, Sep. 2004, pp.265-268

From Teledyne e2v:

(2) François Boré, Marc Wingender, Nicolas Chantier, Andrew Glascott-Jones, Emmanuel Dumaine, Carine Lambert, Sergio Calais « 3 GS/s 7GHz BW 12 Bit MuxDAC for Direct Microwave Signal Generation over L,S or C Bands" in Proc. COMCAS, Tel Aviv, Nov 2011

From TI:

(3) Ravinuthula, V., Bright, W., Weaver, M., Maclean, K., Kaylor, S., Balasubramanian, S., ... & Dwobeng, E. (2016, June). A 14-bit 8.9 GS/s RF DAC in 40nm CMOS achieving> 71dBc LTE ACPR at 2.9 GHz. In VLSI Circuits (VLSI-Circuits), 2016 IEEE Symposium on (pp. 1-2). IEEE.

Author biographies

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Marc has an engineering diploma in microelectronics and automation awarded by the Institut National Polytechnique Grenoble. He has been working in the rarified field of high frequency components now for more than 33 years. His career started at Thomson CSF in Paris where he was involved in early RF characterization of GaAs devices for microwave applications (LNAs and PAs). In 1985 he relocated to Teledyne e2v Grenoble (formerly Thomson CSF/Atmel). Since 2003 Marc has been working to advance the state of the art in giga-sample conversion and has published several papers on the topic over the years.

Romain Pilard (PhD) Application Engineer - Broadband Data Converters

Romain received his B.S. and M.S. degrees in Electronics Engineering from Polytech'Nantes (University of Nantes, Nantes, France) in 2006 and completed a Ph.D. degree in electrical engineering from Telecom Bretagne (Brest, France) in 2009. From 2010 to 2015, he was with STMicroelectronics (Crolles, France), where he worked on the development of integrated antennas and high performance passive components in advanced bulk and SOI RF CMOS technologies. His work dealt with millimeter wave antenna design and packaging technology development. Since 2015 Romain works at Teledyne e2v as an application engineer for Broadband Data Converter solutions.

Julien Duvernay (PhD) Characterization Engineer - Broadband Data Converters

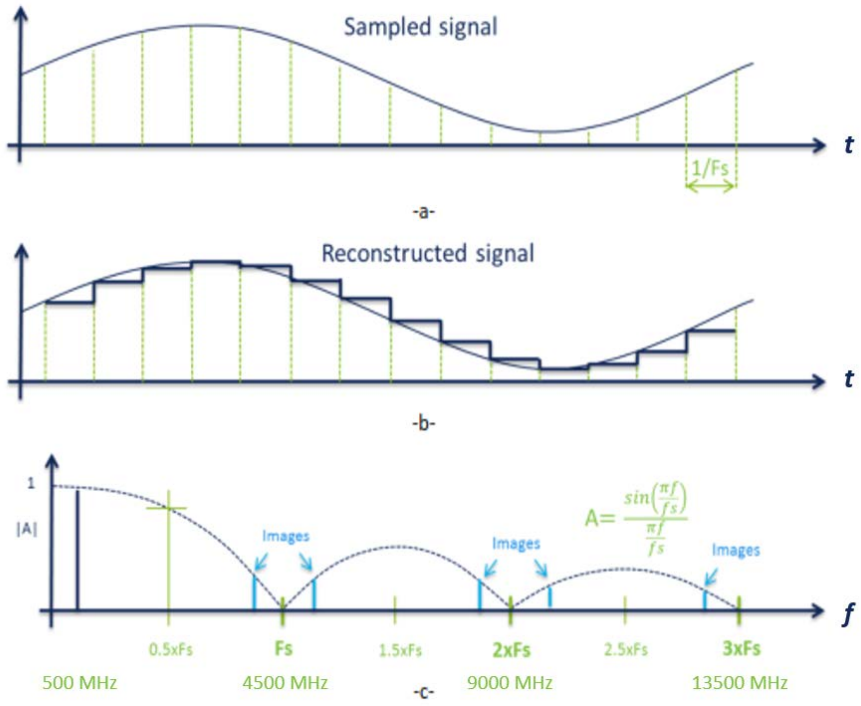
Julien obtained his Engineering diploma in Physics/Electronics from INSA, Lyon engineering school in 2004
He then went on to obtain his doctorate whilst working at STMicroelectronics from 2005-2008 on PNP heterojunction bipolar transistors. Having achieved his doctorate, Julien decided to cycle the world (2008-2009). Julien went on to pursue post-doctoral research at the European Synchrotron facility on surface and interface physics and As doped Silicon (2010-2013). Then Julien moved to CEA working on the characterization of III-V semiconductors for electronics and photonic applications. Finally, Julien joined Teledyne e2v in 2015 to work on the characterization of the broadband data converter portfolio.

Spotlight on sampling theory and up-conversion

One of the harder aspects of high bandwidth digital communication systems to grasp, is the effect sampling has in producing alias image signals at a DAC's output, this brief section shines a light on this process.

Most engineers are aware of the basics of Nyquist sampling theory. The theorem states that any bandwidth limited signal can be properly reconstructed from time discrete samples, provided that the samples are made at a sample rate more than twice the signal bandwidth (2 x fa where fa is the maximum bandwidth).

When considering the implications of sample theory in terms of the frequency domain performance, interesting things happen. A reconstruction DAC provides varying output pulses in response to digital sample data provided, output pulses appear every 1/fs second.



Sidebar figure: Waveform sampling in the time and frequency domains

The two upper curves (Fig. 1 a & b) above show the original and reconstructed waveforms in the time domain with regular sample points illustrated. The middle curve shows the DAC's output. Note the output signal here shows the 'standard', non-return to zero (NRZ) pulse stream. The resulting frequency domain spectrum seen in the lower curve shows the characteristic DAC sinc(x) signal attenuation envelope.

Note the fundamental carrier frequency (f_c) placed at 500 MHz together with multiple attenuated alias signals (images – marked in blue) centered around integer multiples of the sample rate (4.5 GSps). The lower curve maps the frequency domain out to beyond 13.5 GHz showing just over six consecutive Nyquist zones (each fs/2 in width).

With UWB DACs working at high sample rates, the creation of alias signals in the higher order Nyquist zones has positive system benefits. Aliasing can be used to directly up-convert base-band signals to microwave frequencies without additional analog mixers. However, because of the sinc(x) roll-off, power delivered in high order Nyquist zones is attenuated. Assuming a solution can be found to counter this roll-off; direct digital synthesis can enable complex modulation and provide wideband frequency agility even in microwave systems.