Using EV1xDS130B at Sampling Rate Higher than 2.1GSps

Application Note

1. Introduction

In order to ease the data transfer from a FPGA to the DAC, the EV1xDS130B features a fraction of the sampling clock frequency called DSP clock.

On EV1xDS130B, despite high performance is guaranteed at sampling rates up to 3 Gsps, the DSP clock feature is only supported up to 2.1 Gsps sampling rate. In case of higher sampling rate, the DSP clock signal could exhibit some jitter.

In this case, it is recommended to implement an equivalent DSP clock with an external PLL to guarantee the best data transfer from the FPGA to the DAC.

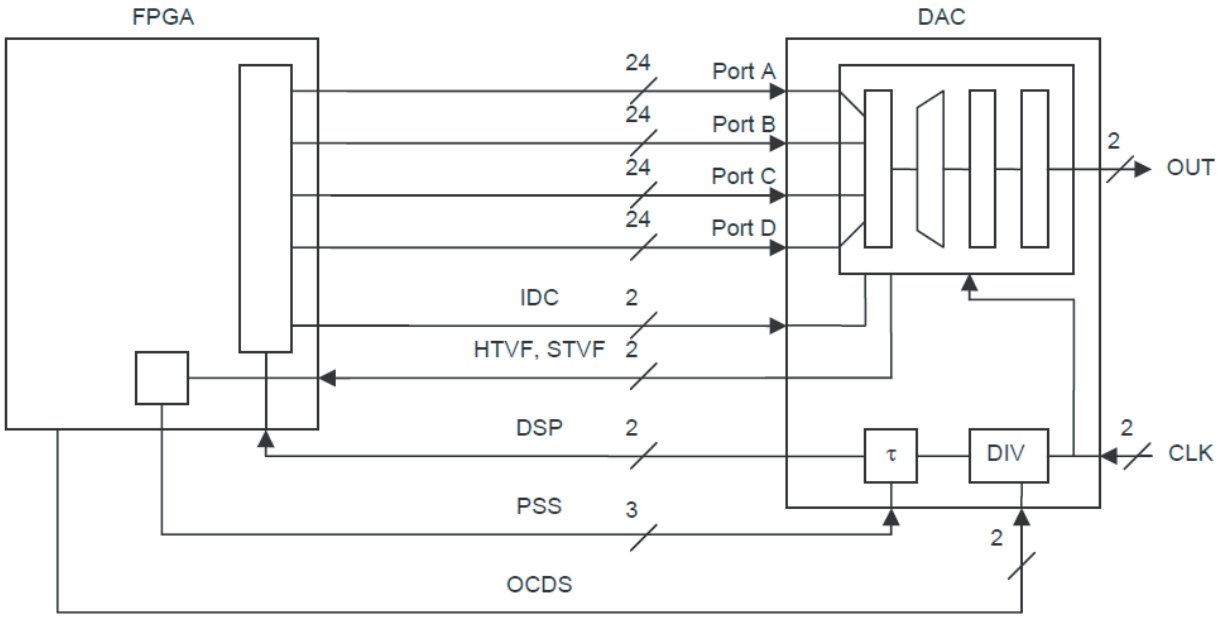
This application note describes the DSP clock feature and gives pieces of advice to be able to use the EV1xDS130B at sampling rates from 2.1 Gsps up to 3 Gsps.

It applies to all EV10DS130BG, EV10DS130BZP, EV12DS130BG, and EV12DS130BZP product families and must be read with the latest datasheet version of the product available on www.e2v.com.

For further information please contact hotline-bdc@e2v.com.

2. Data Synchronization Principle with Built-in DSP (under 2.1 Gsps)

The DSP output clock is an LVDS signal which is used to synchronize the FPGA transmitting the digital data with the DAC sampling clock. The DSP clock frequency is a fraction of the sampling clock frequency.



In order to check that the FPGA data are aligned with the DAC, it is necessary that the FPGA outputs a reference signal toggling at each cycle synchronously with other data bits. This signal called IDC (Input Data Check), considered as DAC input data, allows the DAC checking in real-time whether the timings between the FPGA and the DAC are correct or not.

The IDC line is constantly checked by the DAC, and a timing violation is directly output on the HTVF (Hold Time Violation Flag) or STVF (Set-up Time Violation Flag) pins. (The HTVF flag indicates a hold time violation while the STVF flag indicates a set-up time violation).

In case one or the other flag indicates a data misalignment between the FPGA and the DAC, the DSP clock should be delayed via the PSS (Phase Shift Select) function.

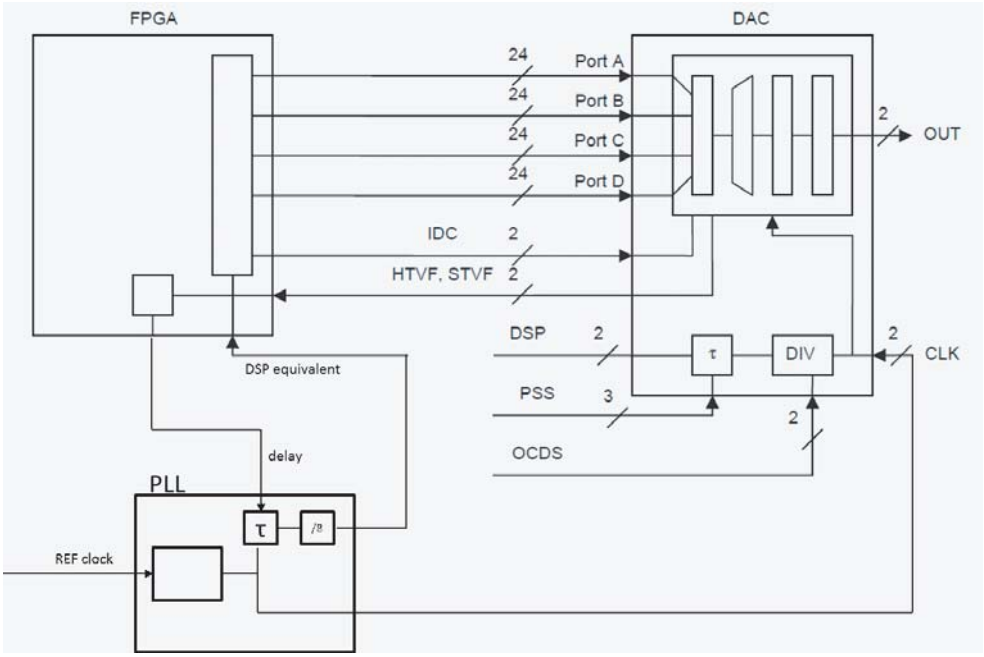
When the data alignment is correct neither the HTVF nor the STVF flag is set.

For further information please see Application Note 1087.

3. Using an External PLL to generate an equivalent DSP Clock Signal

With sampling rates higher than 2.1 Gsps, we recommend recreating a DSP clock signal. Because the equivalent DSP clock frequency is a fraction of the clock frequency with a delay depending on the design of the board, it is possible to generate such signal directly from the DAC master clock PLL.

Indeed, a PLL could generate a fraction of the clock frequency, and a delay adjustment of this clock fraction could be made directly in the FPGA.



The IDC (Input Data Check) will always be sampled, and the HTVF (Hold Time Violation Flag) and STVF (Set-up Time Violation Flag) pins will indicate a violation of set-up or hold time.

In case of timing violation (setup or hold), the user could shift the phase in the FPGA PLL (using IODELAY in Xilinx FPGA or DPA in Altera FPGA for example) for changing the internal timing of data and IDC signal inside the FPGA.

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