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EV12DS130AGS-EB Evaluation Board

12-bit DAC 3Gsps with 4/2:1 MUX User Guide

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Section 1

Introduction

1.1 Scope

The EV12DS130AGS-EB evaluation board is designed to facilitate the evaluation and characterization of the EV12DS130A 12-bit DAC with 4/2:1 MUX in fpBGA package.

The EV12DS130AGS-EB Evaluation Kit includes:

- One MUXDAC evaluation board
- A cable for connection to the RS-232 port
- One CD-ROM that contains the software Tools necessary to use the SPI

The evaluation system of the EV12DS130A MUXDAC device consists in a configurable printed circuit board, including the soldered MUXDAC device, an FPGA chip, a serial interface and a user interface running on that platform.

This user guide should be read in parrallel with the product datasheet and the relative application note.

1.2 Description

The EV12DS130AGS evaluation board is very straightforward as it implements e2v EV12DS130A 12-bit MUXDAC device, ALTERA FPGA STRATIX II EP2S60F672C5N, SMA connectors for the sampling clock, analog outputs and reset inputs accesses.

Thanks to its user-friendly interface, the EV12DS130AGS-EB Kit enables to test all the functions of the EV12DS130A 12-bit MUXDAC.

To achieve optimal performance, the EV12DS130AGS-EB is designed in a 6-metal-layer board using RO4003 epoxy dielectric material. The board implements the following devices:

- The EV12DS130A 12-bit MUXDAC evaluation board with the EV12DS130A 12-bit MUXDAC soldered
- SMA connectors for CLK, CLKN, OUT, OUTN, SYNC, SYNCN, IDC_N, IDC_P
- ALTERA FPGA STRATIX II EP2S60F672C5N soldered to generate the logical pattern
- Banana jacks for the power supply accesses, the die junction temperature monitoring functions, reference resistor
- An RS-232 connector for PC interface

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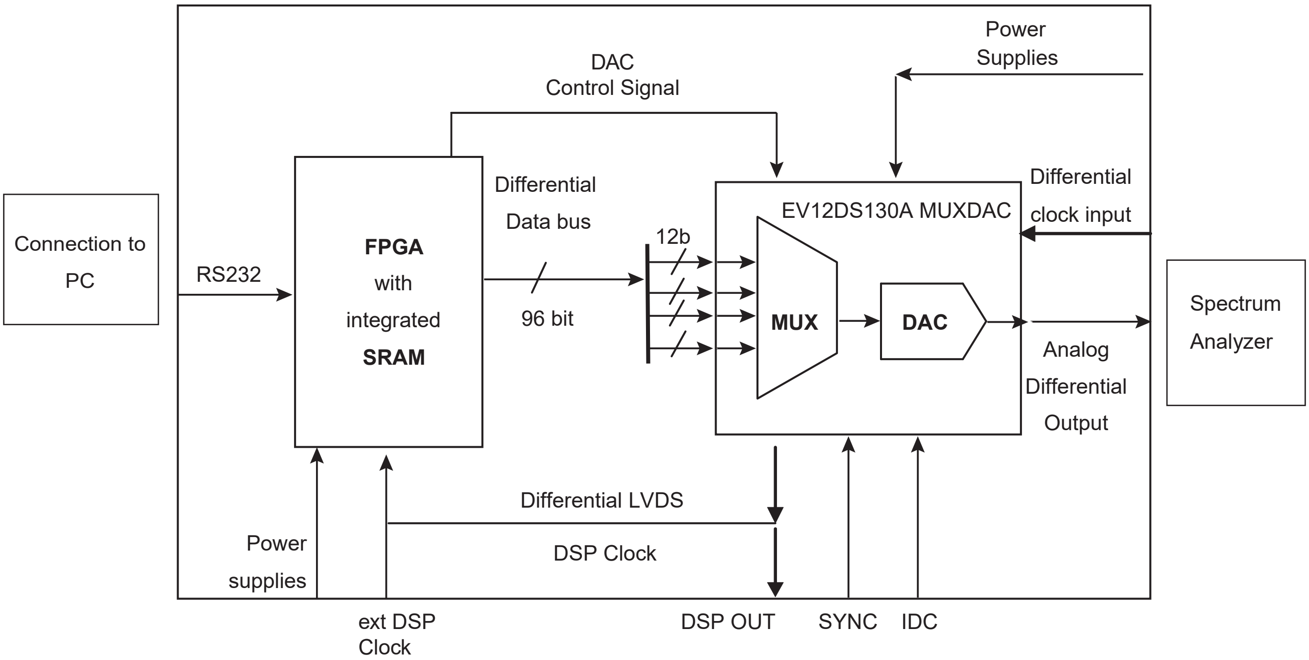
The board dimensions are 180 mm x 210 mm. The board comes fully assembled and tested with the EV12DS130A installed.

Figure 1-1. EV12DS130A-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CCA5} = 5V analog positive power supply
- V_{CCD} = 3.3V digital positive power supply
- V_{CCA3} = 3.3V analog output power supply
- 5V FPGA

Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full-speed operation of the EV12DS130AGS-EB 12-bit MUXDAC, a multi-layer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in RO4003 dielectric material. Table 2-1 gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
RO4003/dielectric layer	Layer thickness = 200 µm
Layer 2 Copper layer	Copper thickness = 18 µm Ground plane = AGND - DGND plane
FR4/dielectric layer	Layer thickness = 350 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power plane = FPGA supplies, VCCD, VCCA3, signals
FR4/dielectric layer	Layer thickness = 350 µm
Layer 4 Copper layer	Copper thickness = 18 µm Reference plane = ground and power plane
FR4/dielectric layer	Layer thickness = 350 µm
Layer 5 Copper layer	Copper thickness = 18 µm Power planes = DGND, V_{CCA5}, GA plane
RO4003/dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces

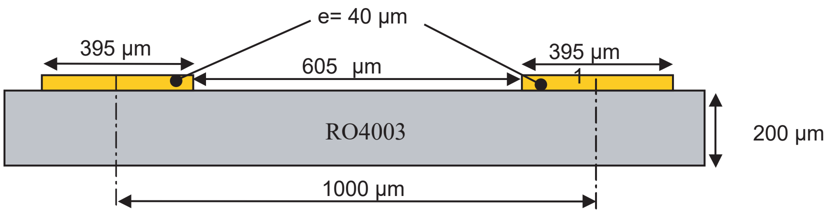
2.2 Analog Outputs

The differential analog output is provided by SMA connectors (reference: VITELEC 142-0701-8511). Both pairs are AC coupled using 100 nF capacitors. (Reference ATC545L Series UBC).

Special care was taken for the routing of the analog output signal for optimum performance in the high-frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between OUT and OUTN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the OUT and OUTN ball footprints

Figure 2-1. Board Layout for the Differential Analog and Clock Inputs



Note: The analog output is AC coupled with 100 nF very close to the SMA connectors.

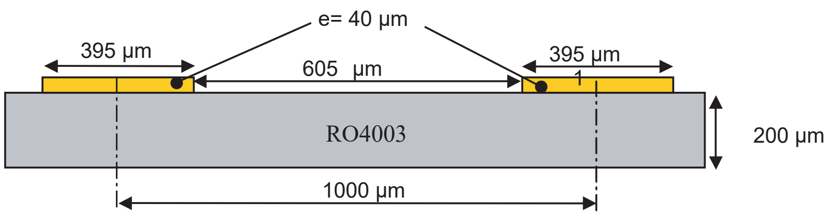
2.3 Clock Inputs

The differential clock inputs is provided by SMA connectors (reference: VITELEC 142-0701-8511). Both pairs are AC coupled using 100 pF capacitors.

Special care was taken for the routing of the clock input signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between CLK and CLKN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the CLK and CLKN ball footprints

Figure 2-2. Board Layout for the Differential Analog and Clock Inputs



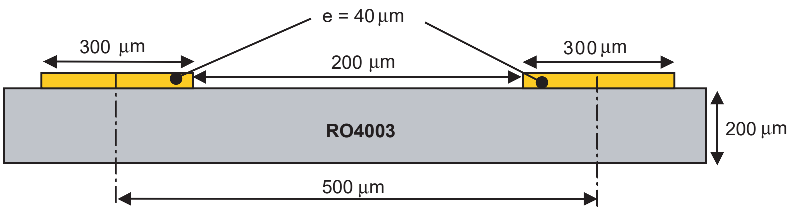
Note: The clock input is AC coupled with 100 nF very close to the SMA connectors.

2.4 Digital Inputs

The digital input lines were designed with the following recommendations:

- 50Ω lines matched to ±2.5 mm (in length) between signal of the same differential pair
- ±1 mm line length difference between signals of two differential pairs
- 500 µm pitch between the differential traces
- 650 µm between two differential pairs
- 300 µm line width
- 40 µm thickness

Figure 2-3. Board layout for the Differential Digital Inputs



The digital inputs are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

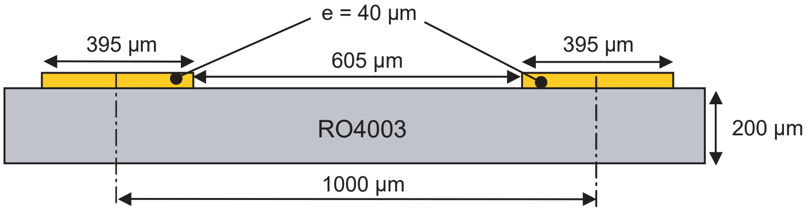
2.5 SYNC Inputs

The hardware reset signals are provided; SYNC, SYNCN corresponds to the reset of the output of the DAC (analog reset).

The differential reset inputs are provided by SMA connectors (Reference: VITELEC 142-0701-8511).The signals are AC coupled using 10 nF capacitors and pulled up and down resistors.

- 50Ω lines matched to ±0.1 mm (in length) between SYNC and SYNCN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness

Figure 2-4. Board Layout for the SYNC Signal



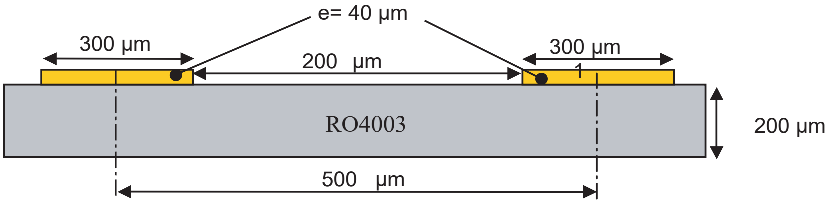
2.6 DSP, DSPN Signals Inputs

The differential DSP and DSPN signals can be provided by SMA connectors (not connected).

Special care was taken for the routing of DSP, DSPN signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between DSP and DSPN
- 500 µm pitch between the differential traces
- 650 µm between two differential pairs
- 300 µm line width
- 40 µm thickness

Figure 2-5. Board layout for the DSP signal



These signals are compatible with LVDS standard. They are on-chip 100Ω differentially terminated. DSP, DSPN are not used for normal operation. They can be left open.

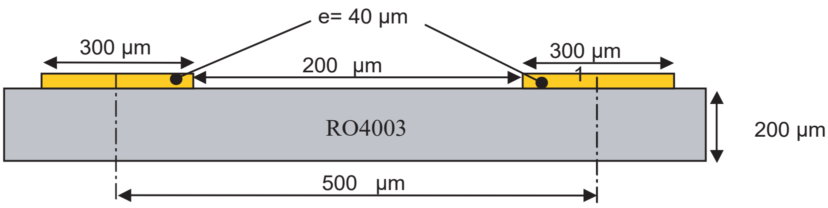
2.7 DSP OUT, DSPN OUT Signals Outputs

The differential DSP OUT and DSPN OUT signals can be provided by the SMA connectors (not connected).

Special care was taken for the routing of DSP OUT, DSPN OUT signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between DSP OUT and DSPN OUT
- 500 µm pitch between the differential traces
- 650 µm between two differential pairs
- 300 µm line width
- 40 µm thickness

Figure 2-6. Board layout for the DSP OUT signal



These signals are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

DSP, DSPN are not used for normal operation. They can be left open.

2.8 CALIBRATION Lines

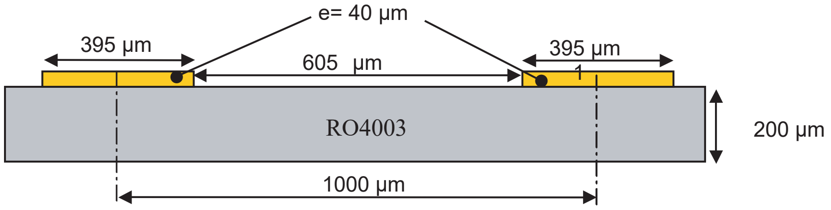
Both pairs are AC coupled using 100 nF capacitors. (Reference ATC545L Series UBC).

Calibration lines have exactly the same length than Analog Outputs.

Special care was taken for the routing of the analog output signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between CAL and CALN;
- 605 µm pitch between the differential traces;
- 1000 µm between two differential pairs;
- 395 µm line width;
- 40 µm thickness;
- 850 µm diameter hole in the ground layer below the CAL and CALN ball footprints.

Figure 2-7. Board layout for the differential analog and clock inputs



Note: The calibration lines are AC coupled with 100 nF very close to the SMA connectors.

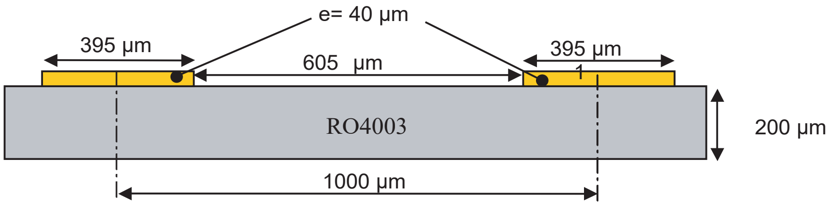
2.9 IDC Inputs

The differential IDC signals are provided by SMA connectors. (reference: VITELEC 142-0701-8511).

The signals are AC coupled using 10 nF capacitors.

- 50Ω lines matched to ±0.1 mm (in length) between SYNC and SYNCN
- 605 µm pitch between the differential traces;
- 1000 µm between two differential pairs;
- 395 µm line width;
- 40 µm thickness;

Figure 2-8. Board Layout for the IDC signal



2.10 Power Supplies

Layers 3, 4 and 5 are dedicated to power supply planes (V_{CCA3}, V_{CCD}, V_{CCA5}, 5V FPGA).

The supply traces are low impedance and are surrounded by two ground planes (layer 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor. Each power supply is decoupled as close as possible to the EV12DS130A device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the EV12DS130A 12-bit MUXDAC.

The analog output signal and the sampling clock signal should be in a differential fashion.

Note: The analog outputs and clock inputs are AC coupled on the board.

3.2 Operating Procedure

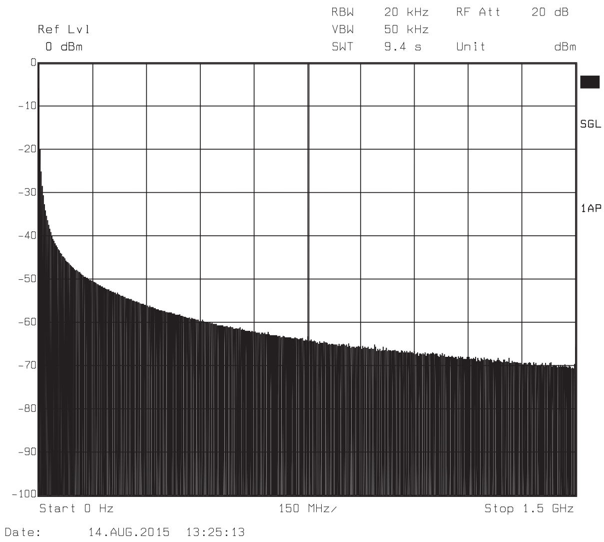
1. Install the SPI software as described in section 4 “Software Tools”.
2. Connect the power supplies and ground accesses through the dedicated banana jacks.
   V_{CCA3} = 3.3V, V_{CCD} = 3.3V, V_{CCA5} = 5V and for the FPGA +5V
3. Connect the clock input signals. The clock input level is typically 3 dB to 10 dBm and should not exceed 12 dBm (into 50Ω).
4. Connect the analog output signals to a spectrum analyzer (the board has been designed to allow only AC coupled analog outputs). The analog output signals must be used in differential via differential-to-single transformer.
5. Connect the PC's RS-232 connector to the Evaluation Board's serial interface.
6. Switch on the DAC power supplies : See section 3.2 and 7.9 of the datasheet
7. Turn on the RF clock generator.
8. Switch on the FPGA power supply (+5V)
9. Launch the software, (the software must be launched with the evaluation board powered on).
10. Launch software. (software must be lunch with evaluation board power ON).

The EV12DS130AGS-EB evaluation board is now ready for operation.

Note: To use the software, you should be in Administrator mode.

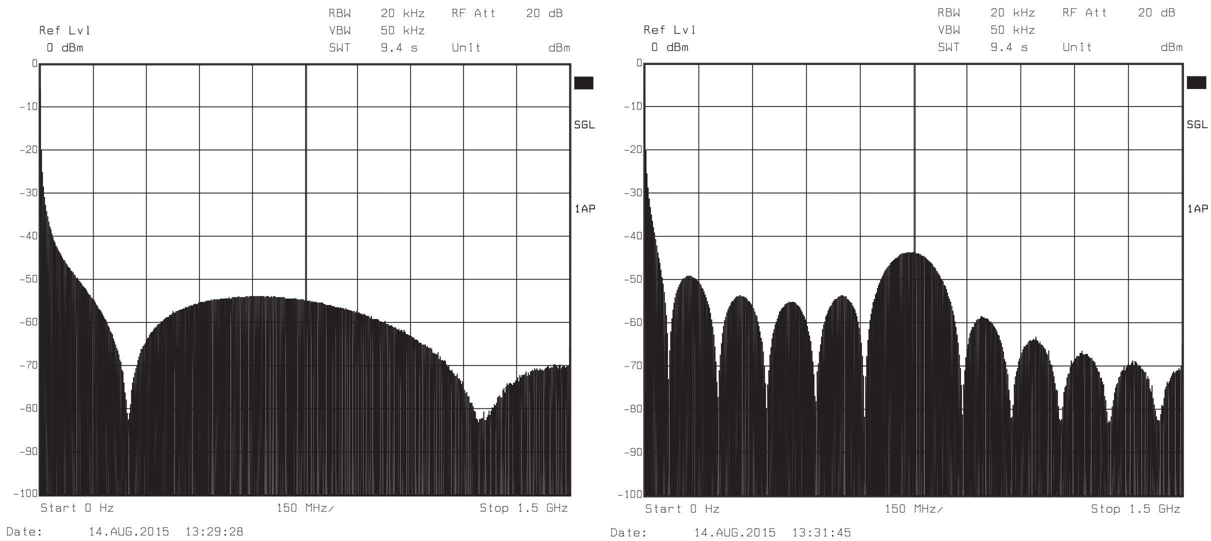
The following graph shows a good synchronization.

Figure 3-1.



If you have not ramp (cf: graphs below) on the output, push reset board.

Figure 3-2.



3.3 Electrical Characteristics

For more information, please refer to the device datasheet.

See section 3.2 of the datasheet.

Table 3-1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RESOLUTION			12		bit	
ESD CLASSIFICATION			Class 1B			
POWER REQUIREMENTS						
Power Supply voltage - Analogue - Analogue - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	 V V	
Power Supply current (4:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 95 110 200	 mA mA mA	
Power Supply current (2:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 95 110 170	 mA mA mA	
Power dissipation (4:1 MUX)	P_D		1.33		W	
Power dissipation (2:1 MUX)	P_D		1.25		W	

Section 4

Software Tools

4.1 Overview

The MUXDAC 12-bit evaluation user interface software is a Visual C++ compiled graphical interface that does not require a licence to run on a Windows NT and Window 2000/XP PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Configuration

The advised configuration for Windows 98 is:

- PC with Intel Pentium Microprocessor of over 100 MHz
- Memory of at least 24 Mo.

For other versions of Windows OS, use the recommended configuration from Microsoft.

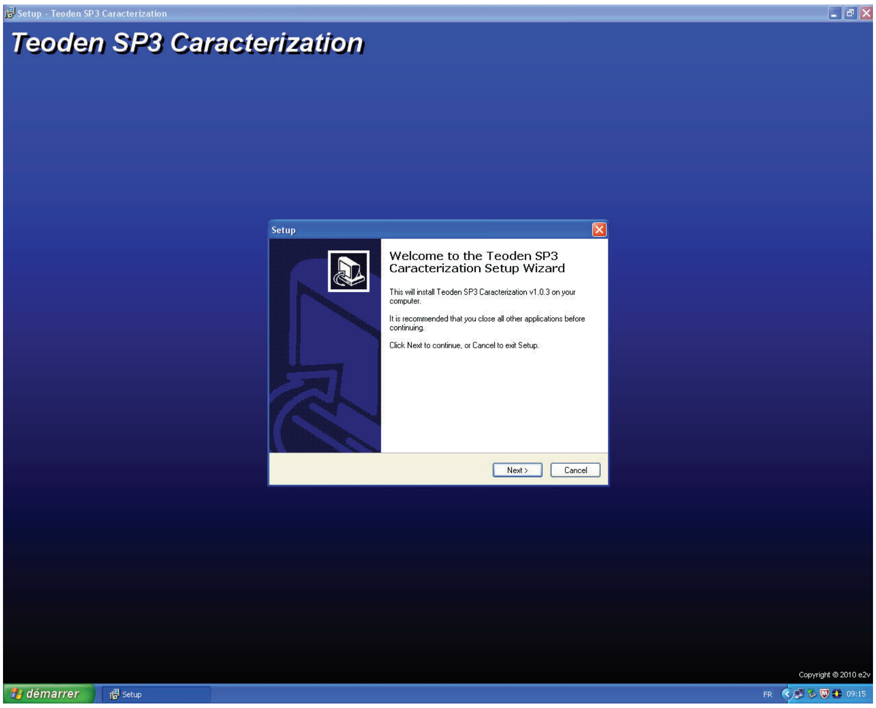
Note: Two COM ports are necessary to use two boards simultaneously.

4.3 Getting Started

1. Install the 12-bit MUXDAC application on your computer by launching the Setup_TeodenSP3 Carac.exe installer (please refer to the latest version available).

The screen shown in Figure 4-1 is displayed:

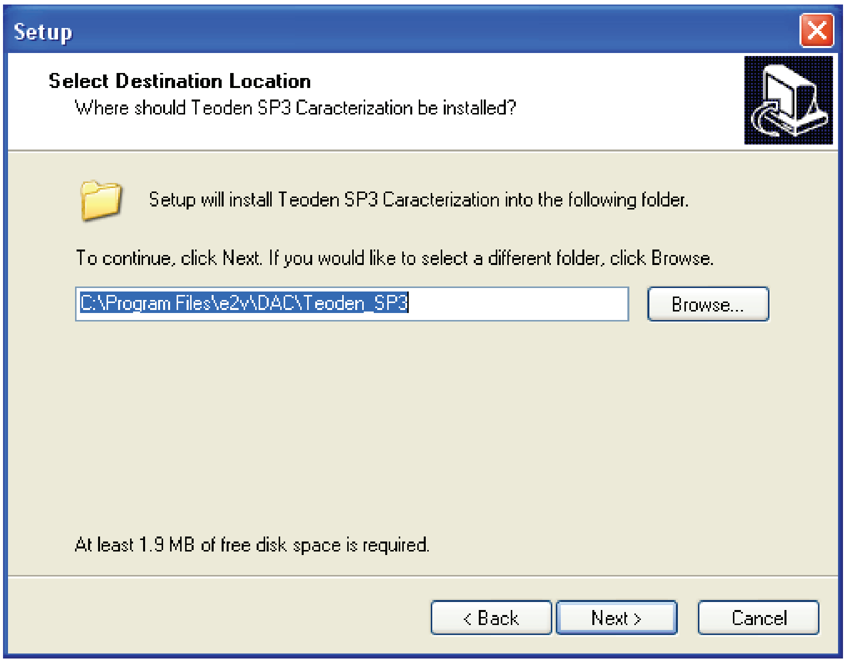
Figure 4-1. Application *Setup Wizard* Window



Note: "Teoden" is a nickname of EV12DS130A used in e2v.

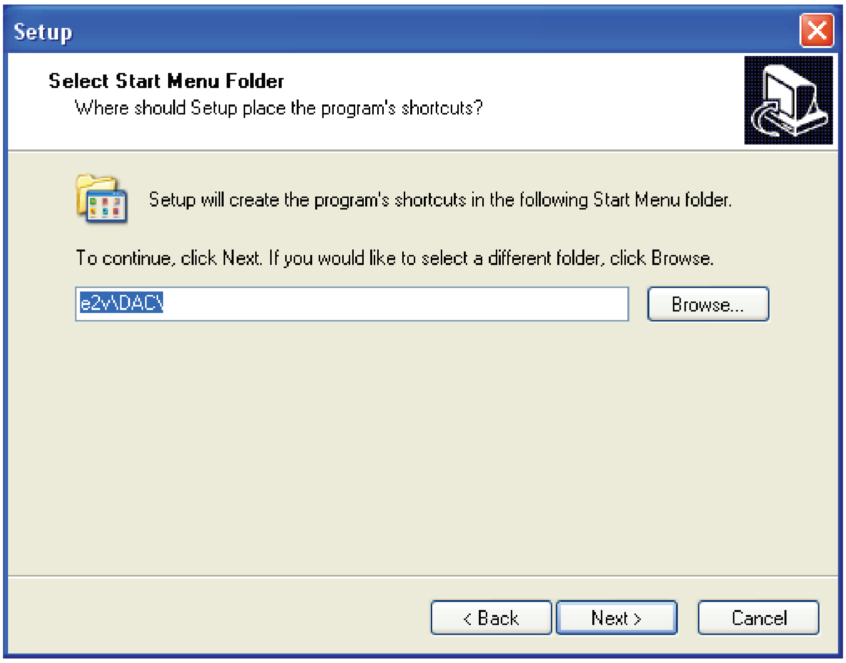
2. Select Destination Directory

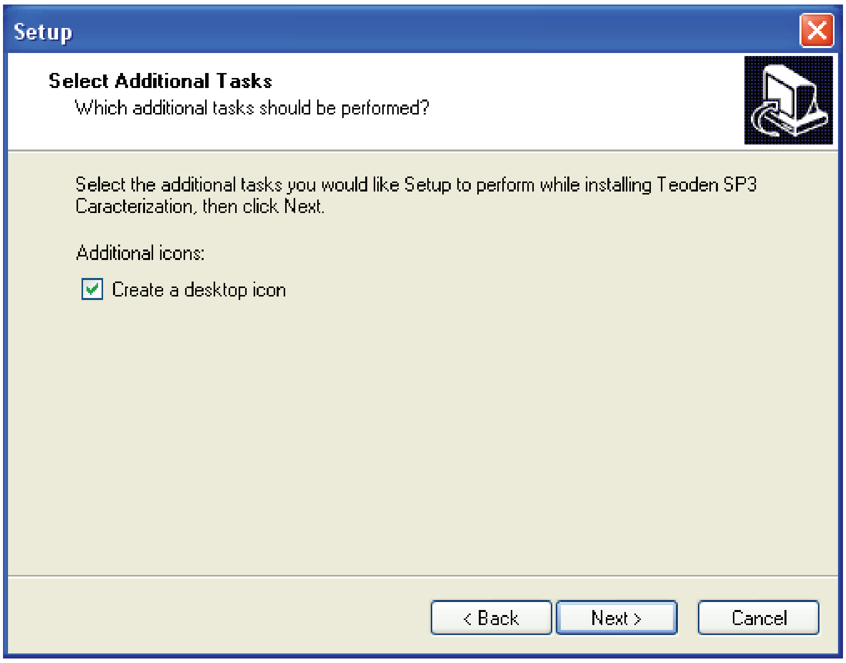
Figure 4-2. *Select Destination Directory* Window



3. Select Start Menu Folder

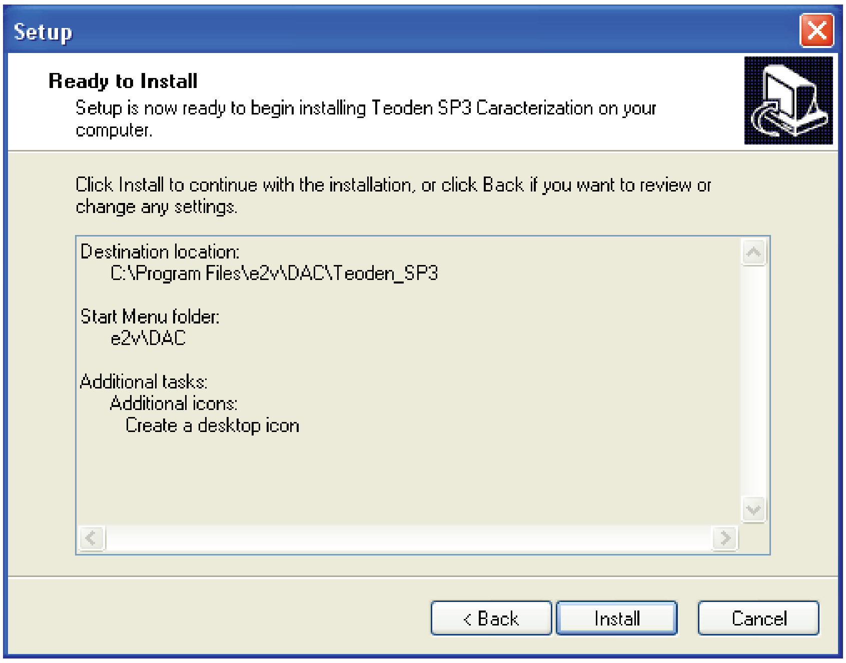
Figure 4-3. Select *Start Menu* Window





4. Ready to install

Figure 4-4. *Ready to Install* Window

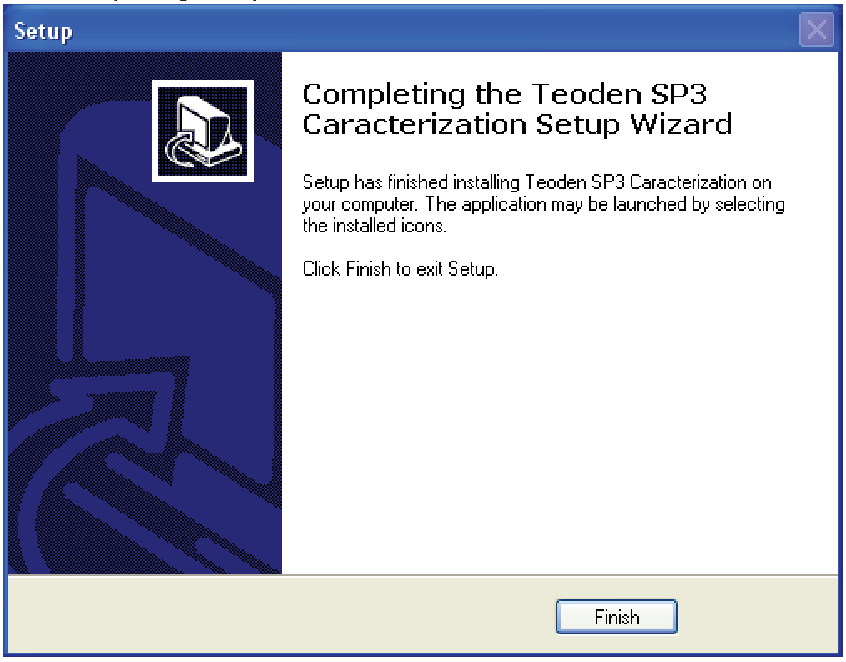


If you agree with the install configuration, press **Install**.

The installation of the software is now completed.

Note: If a problem appears at the end of the installation, please install the setup vcredist_x86.exe available in the "My program dependencies" file of the CD.

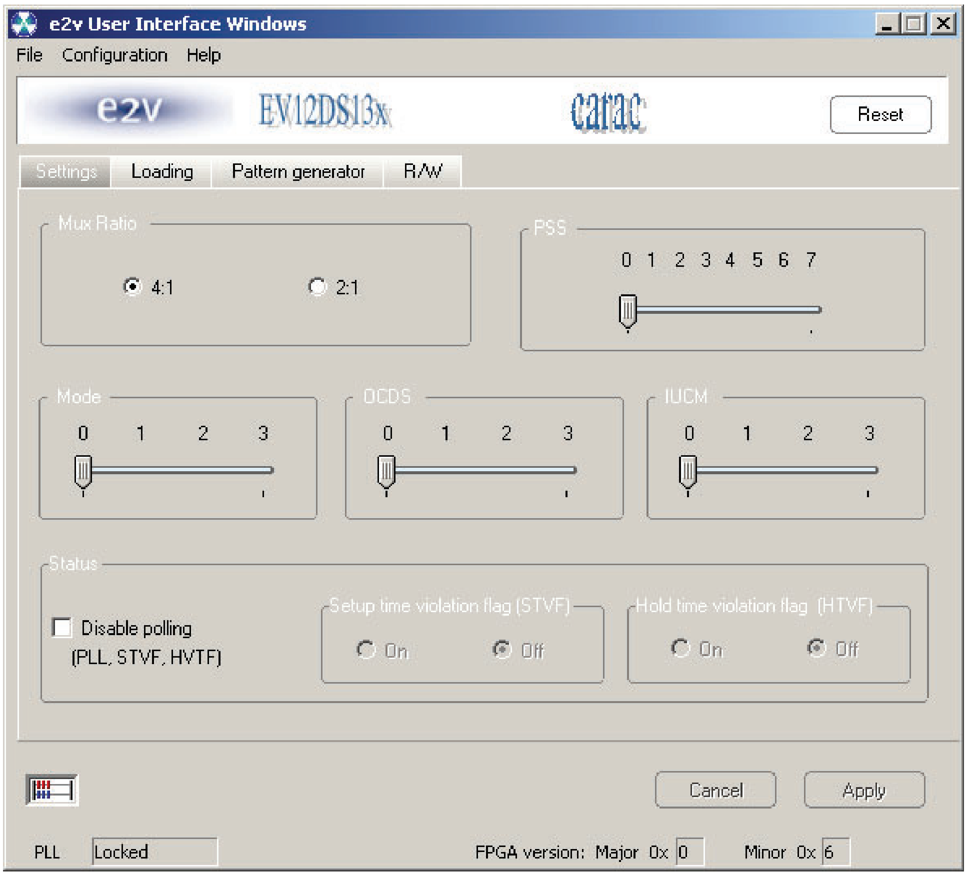
Figure 4-5. Completing *Setup Wizard* Window



After the installation, you can launch the interface with the following file: C:\Program Files\e2v\...

The window shown in Figure 4-6 will be displayed.

Figure 4-6. User Interface Window



Notes: 1. If the MUXDAC application board is not connected or not powered, an error message is displayed.

2. Check your connection and restart the application (refer to section 3).

4.4 Troubleshooting

1. Check that you own rights to write in the directory.
2. Check for the available disk space.
3. Check that at least one RS-232 serial port is free and properly configured.
4. Check that the serial port and DB9 connector are properly connected.
5. Check that all supplies are properly powered on.

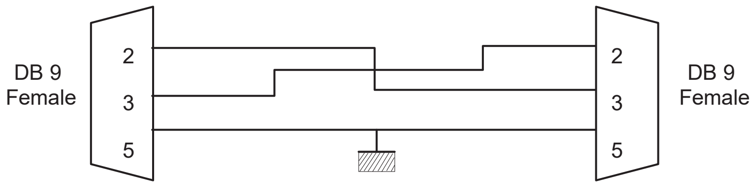
The serial port configuration should be as follows:

- Bit rate: 19200
- Data coding: 8 bits
- 1 start bit, 1 stop bit
- No parity check

Figure 4-7. User Interface Hardware Implementation

1. Use an RS-232 port to send data to the DAC.
2. Connect the crossed DB9 (F/F) cable between your PC and your evaluation board as illustrated in Figure 4-8.

Figure 4-8. Crossed Cable



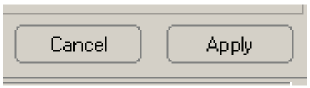
4.5 Operating Modes

The MUXDAC software included with the evaluation board provides a graphical user interface to configure the DAC.

Push buttons, popup menus and capture windows allow easy:

With Setting and Test mode windows always click on *Apply* button to validate any command.

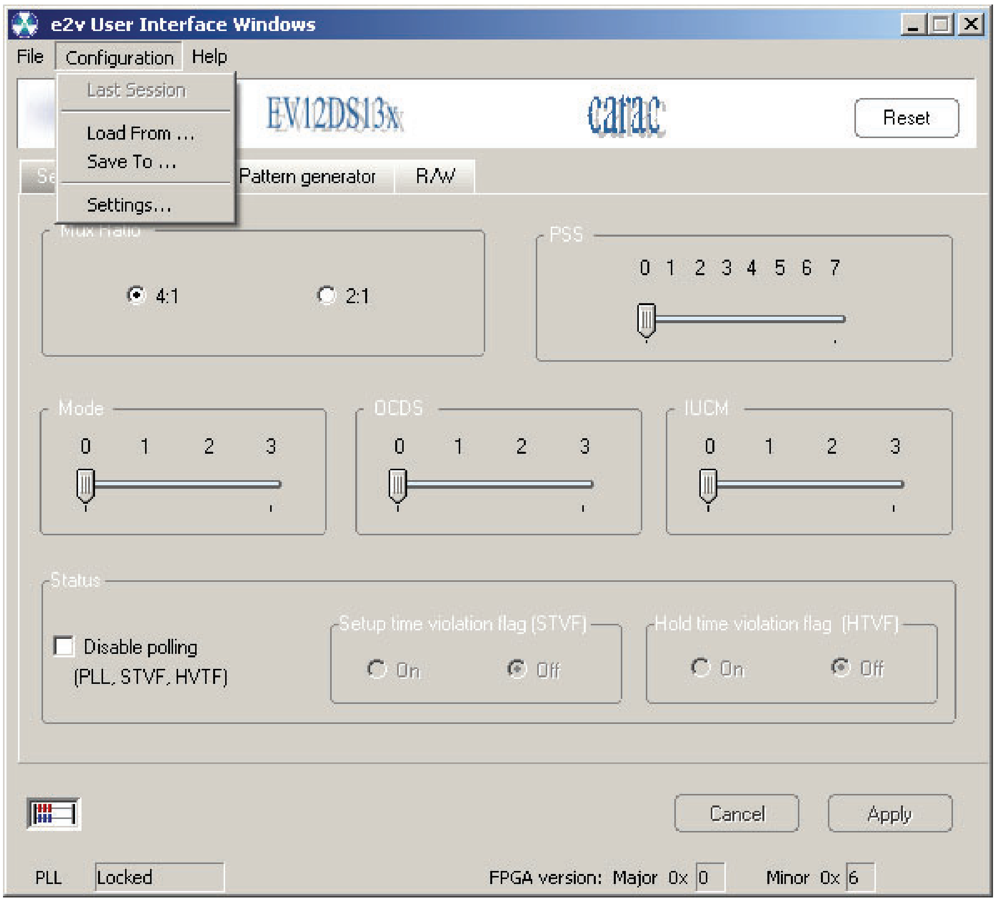
Figure 4-9. Cancel/Apply Buttons



Clicking on the *Cancel* button will restore last settings sent with *Apply* button.

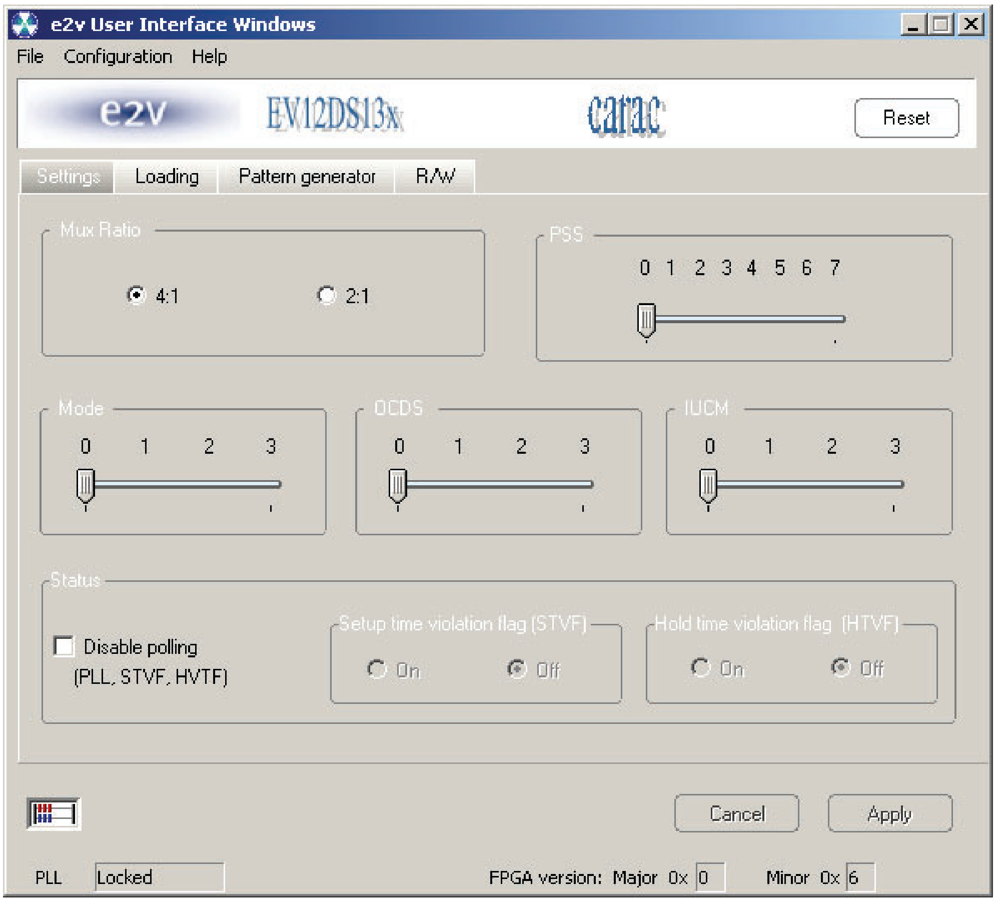
The user could "save" or "load" the register configuration via the configuration function.

Figure 4-10. Save/Load Register Configuration Window



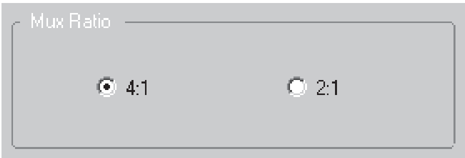
4.5.1 Settings

Figure 4-11. Settings Window



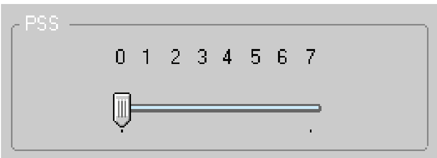
The software allows choosing between the MUX ratio 2 to 1 or 4 to 1.

Figure 4-12. MUX Ratio



The software allows adjusting the "PSS" (Phase Shift Select) delay to avoid a forbidden timing area between the data input and the clock input.

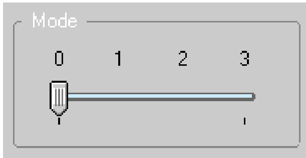
Figure 4-13. Clock Shift Select



Mode:

The MODE Function allows choosing between NRZ, reshaped NRZ, RTZ and RF functions.

Figure 4-14. DAC Output Mode

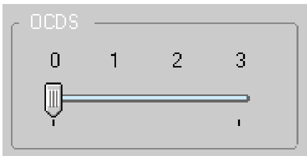


Label	Value	Description	Default setting	Position (IHM)
MODE[1:0]	00	NRZ mode	00	0
	01	Narrow RTZ (NRTZ)		1
	10	RTZ Mode (50%)		2
	11	RF		3

OCDS Function:

The software allows changing the DSP clock internal division factor from 1 to 2, 4 or 8.

Figure 4-15. OCDS Mode



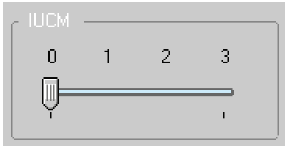
Label	Value	Description
OCDS [1:0]	00	DSP clock frequency is equal to the sampling clock divided by 2N
	01	DSP clock frequency is equal to the sampling clock divided by 2N*2
	10	DSP clock frequency is equal to the sampling clock divided by 2N*4
	11	DSP clock frequency is equal to the sampling clock divided by 2N*8

Note: For more details see Erratasheet on OCDS.

IUCM Function:

An input underclocking mode has been added to the DAC in order to allow for a specific use where the input data are applied to the DAC at half the nominal rate with respect of the DAC sampling rate.

Figure 4-16. IUCM Mode



Label	Value	Description
IUCM	0	Input Underclocking ode inactive
	1	Input Underclocking ode active

Note: Position 2 and 3 are not used.

Status:

The polling function allows scanning the FPGA to known the FGPA version and the PLL state. Setup time violation flag and Hold time violation flag can't be used at this time with this evaluation board. There are used to know if DAC are sampling correctly datas which are sent by the FPGA.

Figure 4-17. PLL Disable

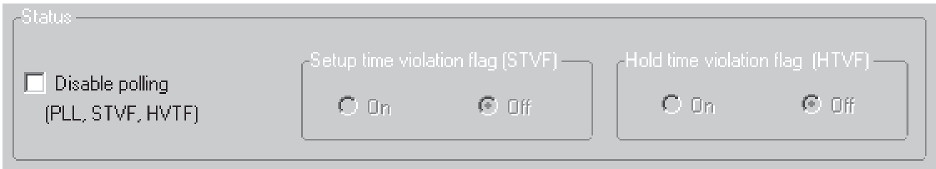


Figure 4-18. PLL Locked

4.5.2 Loading

This module allows to send the pattern to the MUXDAC. You can choose to send a ramp pattern or to send a dedicated pattern.

For ramp pattern:

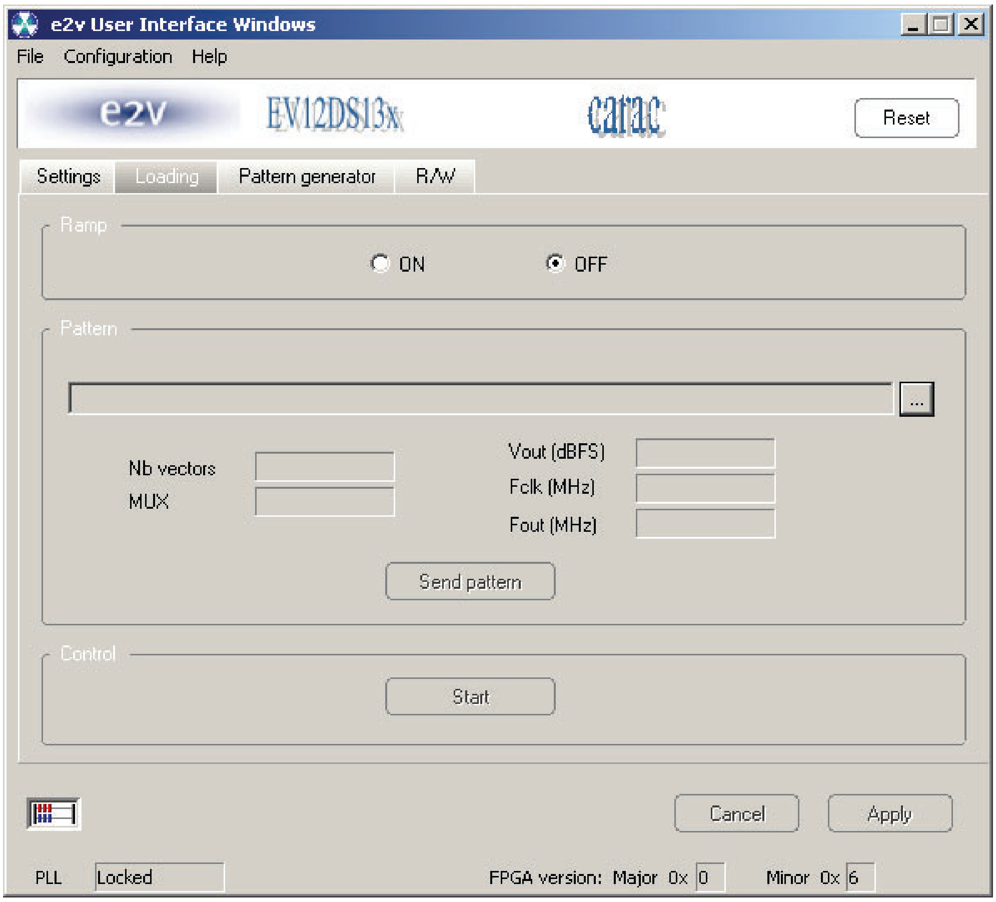
- Active *Ramp* ON
- Press **Start** (for stop press **Stop**)

For dedicated pattern:

- Find the pattern file in the folders' architecture
- Check the information (nb vectors, MUX etc.)
- Press **Send** pattern
- Press **Start**
- For stop pattern press **Stop**

Note: Before loading new pattern press *Stop*

Figure 4-19. Loading Process Window

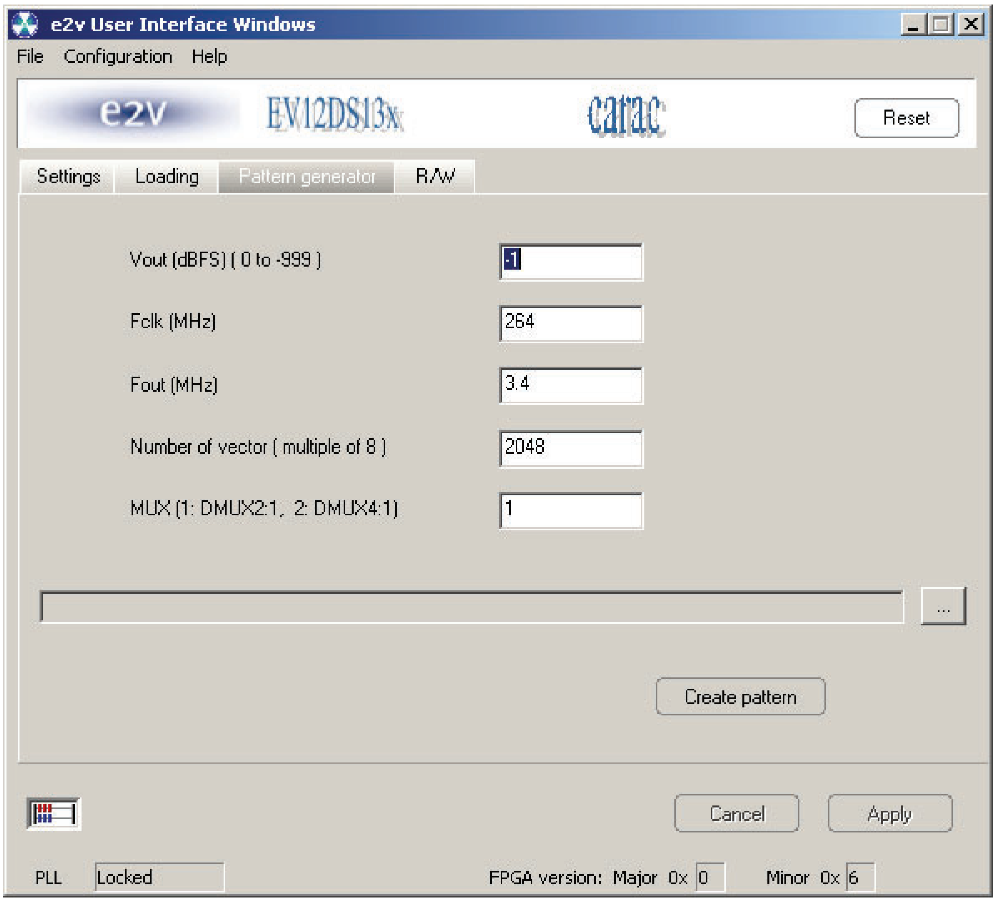


4.5.3 Pattern Generator

This module allows creating sinewave pattern file only in order to send the data to the MuxDac.

Pattern generator procedure:

- Put information for each field.
- Put the way of the target folder to save the pattern
- Push "create pattern"



Note: Not to exceed 4096 vectors with this generator otherwise pattern generates spurs in the FFT spectrum.

If you wish to create your own pattern file, please make sur to follow the below example.

For FFT minimum vector is : 2048

Maximum Vector = 16384

Minimum Vector = 8

The number of vector must be a multiple of 8

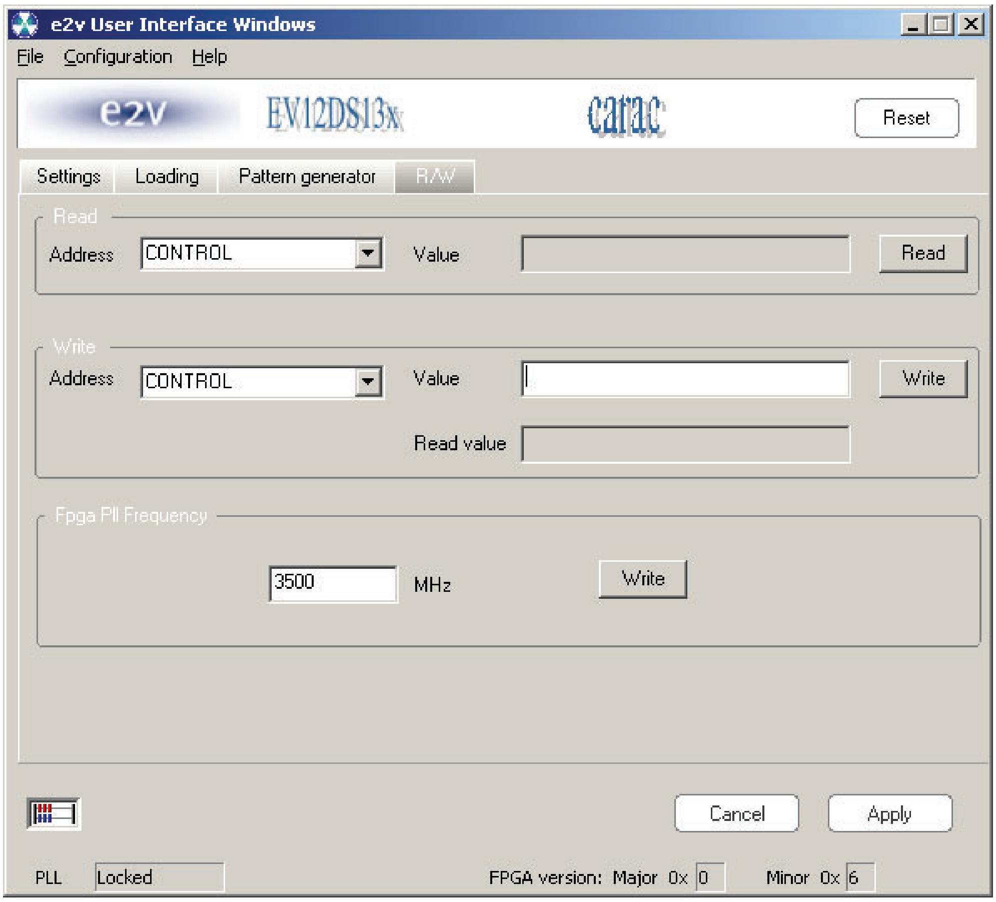
Example of Pattern file

```
# Vout (dBFS)     0
# Fclk (MHz)      3000
# Fout (MHz)      998.108
# MUX             2    DMUX4:1
# Nb vectors      4096
#
Vector 0:    100000000000  111011110001  000100011010  011111100111
Vector 1:    111011111101  000100100111  011111001111  111100001001
Vector 2:    000100110011  011110110110  111100010100  000101000000
Vector 3:    011110011110  111100011111  000101001101  011110000110
Vector 4:    111100101010  000101011011  011101101110  111100110101
Vector 5:    000101101001  011101010101  111101000000  000101110110
………………………………………………………………………………………..
………………………………………………………………………………………..
……………………………………………………………………………………etc…….
Vector 4092:    000011010101  100001110111  111010110011  000011100001
Vector 4093:    100001100100  111010111101  000011101010  100001001011
Vector 4094:    111011001011  000011110101  100000110001  111011011000
Vector 4095:   000100000010  100000011000  111011100101  000100001110
```

Your file must be terminated by an “Enter”.

4.5.4 R / W

This module is used only for debug and just available with hotline support.



4.6 Configuration and Software of the FPGA Memory

The EV12DS130AGS used a Altera Stratix II FPGA Reference.

4.6.1 PROG FPGA

The configuration of the FPGA memory is done via the connector *PROG FPGA* already soldered on the evaluation board.

The schematic is shown in Figure 4-20.

Figure 4-20. FPGA Configuration in AS Mode (Serial Configuration Device Programmed Using Download Cable)

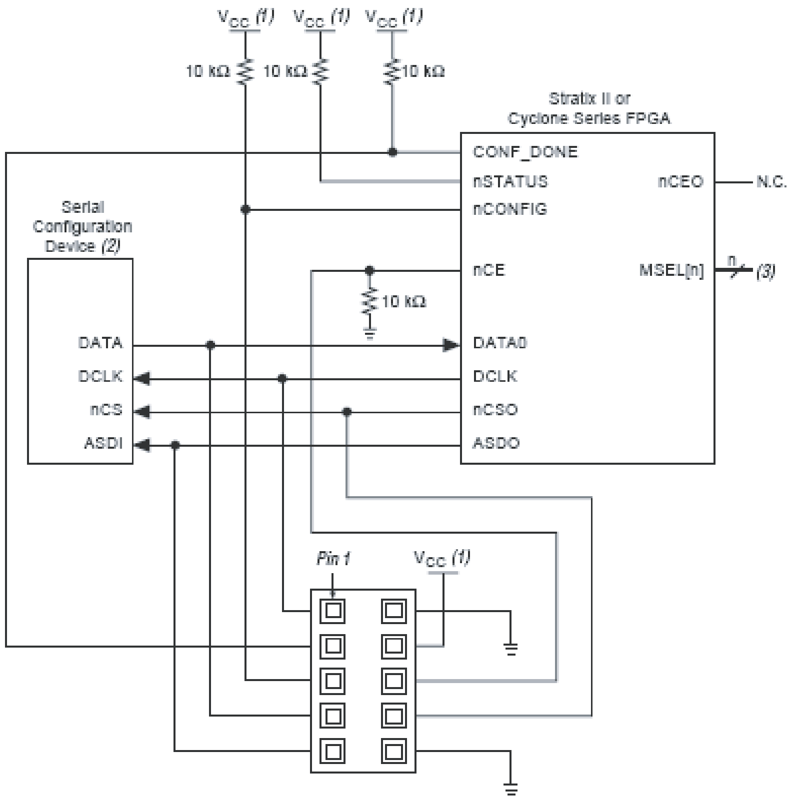


Table 4-1. Connector Type HE10 Male 2x5 points

Pin	Name	Pin	Name
1	DCLK (Serial clock)	2	GND (ground)
3	CONF-DONE (pull-up VCC)	4	VCC = 3.3V
5	nCONFIG (pull-up VCC)	6	nCE (pull-down)
7	DATA0 (data prog FPGA)	8	nCSO (Chip select)
9	ASDO	10	GND (ground)

For the configuration of the serial memory, there is a 4-bit configuration (MSL0-3).

In this application note that we use the FAST AS (40 MHz) mode:

- MSEL3: jumper out
- MSEL2: jumper in
- MSEL1: jumper in
- MSEL: jumper in

Table 4-2 shows the MSEL pin settings when using the AS configuration scheme.

Table 4-2. STRATIX II and STRATIX II gx MSEL Pin Settings for AS Configuration

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSLE0
Fast AS (40 MHz)(1)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)(1)	1	1	0	1
Remote system upgrade AS (20 MHz)(1)	1	1	1	0

Note: 1. Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz.

4.6.2 FPGA Configuration with JTAG

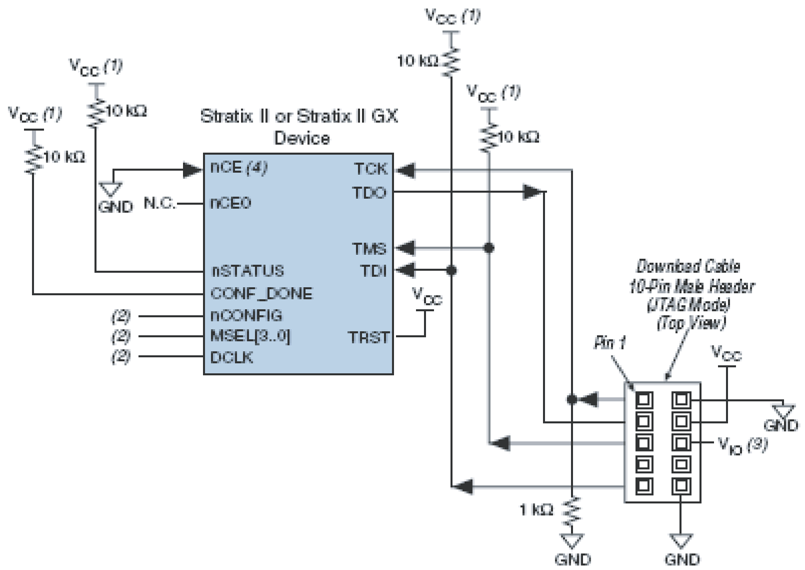
FPGA configuration with JTAG is used on debug mode.

Note: If the evaluation is powered off, the FPGA loses its configuration

The programming is implemented via JTAG connector. This connector is not on the evaluation board.

The schematic is shown in Figure 4-23.

Figure 4-21. Configuration of a Single Device Using a Download Cable



Notes: 1. The pull-up resistor should be connected to the same supply voltage as the USB Blaster, MasterBlaster V_{10} pin byteBlasterII or ByteBlasterMV cable.
2. The jumper configuration (MSEL) has no effect in this mode.

Connector type HE10 male 2x5 points

Table 4-3.

Pin	Nom	Pin	Nom
1	TCK (pull down)	2	GND (ground)
3	TDO	4	VCC (3.3V)
5	TMS (pull up)	6	NC
7	NC	8	NC
9	TDI (pull up)	10	GND (ground)

We use JTAG USB for the FPGA programmation in JTAG mode.

4.6.3 Configuration of the FPGA on EV12DS130AGS Evaluation Board

This sequence is correct for the serial memory configuration and JTAG configuration.

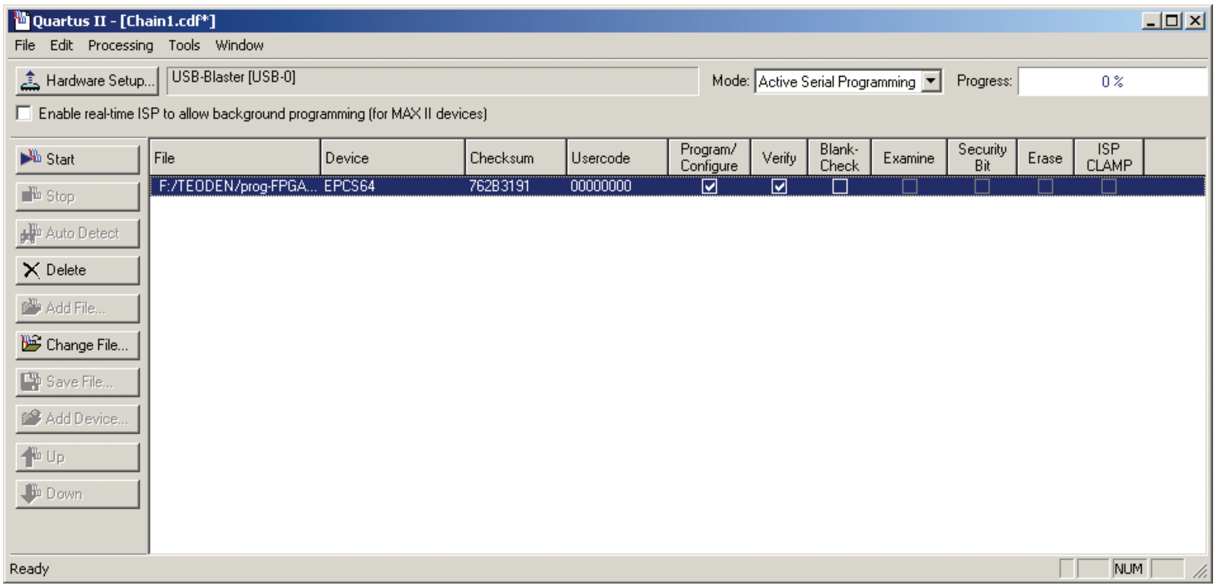
Sequence:

1. Setup the power supplies +5V
2. Connect the jumper MSEL (only for the serial memory)
   – MSEL3: Jumper off (signal to 3.3V)
   – MSEL2, MSEL1, MSEL0: jumper on (signal to GND)
   – RAMP _PATTERN: no jumper
3. Connect the USB BLASTER ALTERA cable on the evaluation board
   – PROG FPGA: for serial memory configuration
   – JTAG: For the JTAG configuration
4. Switch ON the supplies
5. Launch ALTERA QUARTUS II 8.0 software
6. Click on **Program**.

The window shown in Figure 4-22 is displayed:

7. Check that the *USB blaster [USB-0]* is selected, or click on *Hardware Setup* to perform this.
8. Select the mode *Active Serial Programming* for the serial memory programming.
9. Select the mode JTAG for programming via JTAG
10. Choose the program file (teoden_top.pof design 3 GHz) via *Add file*. The information must be indicated.
11. Click on **Start** to launch the program.

Figure 4-22. Sequence Serial Memory Configuration and JTAG Configuration



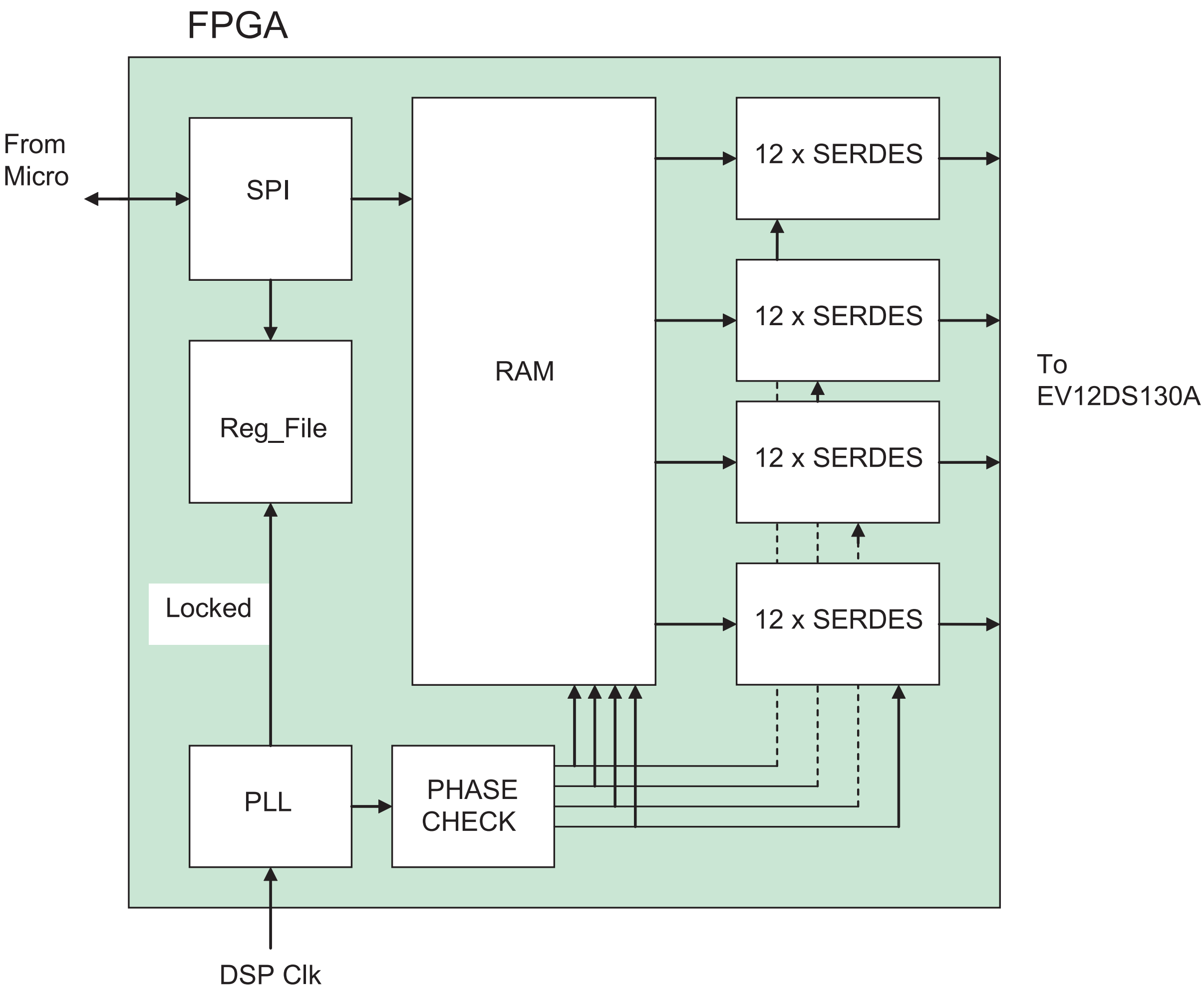
The FPGA configuration is complete when the *Progress* status shows 100%. For the serial memory mode, switch off the 5V supply.

12. Disconnect the USB BLASTER ALTERA cable, then power up the evaluation board to load the software via the external serial memory.

4.6.4 FPGA Block Diagram

The following figure represents the block Diagram of the FPGA :

Figure 4-23. FPGA Block Diagram



SPI	: SPI interface block
Reg File	: Control and Status registers and IO control
PLL	: Stratix PLL black box
RAM	: Startix MRAM and DPRAM instantiations
PHASE CHECK	: Process to ensure readout clock are in phase
SERDES	: 1 per output bit, so 12 per channel. Each SERDES is 8bits deep.

Section 5

Application Information

5.1 Analog Outputs

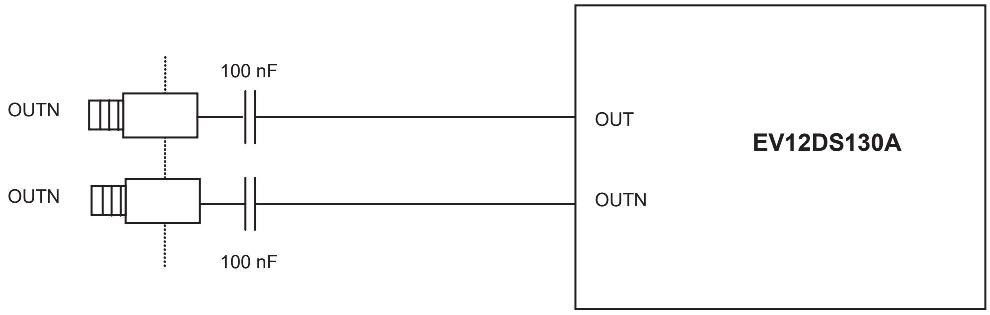
The analog output is in differential AC coupled mode as described in Figure 5-1.

The single-ended operation for the analog output is allowed but it may degrade the DAC performance significantly. It is therefore recommended to use a differential via an external balun or differential amplifier.

Note: References of differential amplifiers and external baluns:

- M/A-COM H9 balun
- M/A-COM TP101 1:1 transformer
- ANAREN 3A0056 3 dB coupler 2G-4G
- KRYTAR double arrow 180° hybrid 2G-8G

Figure 5-1. Differential Analog Output Implementation

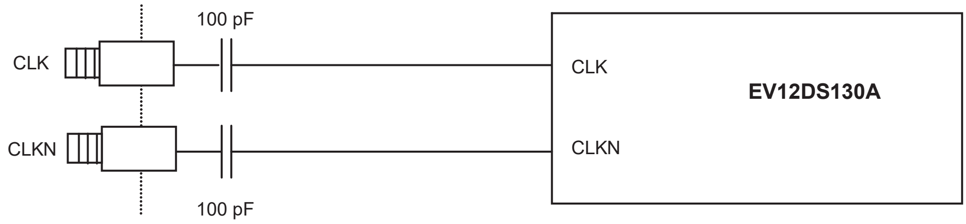


For further application information refer to application note 1087.

5.2 Clock Inputs

The clock input can be entered indifferently in single-ended or differential mode with no performance degradation. The clock is AC coupled via 100 pF capacitors as described in Figure 5-2.

Figure 5-2. Clock Input Implementation



If used in single-ended mode, CLKN should be terminated to ground via a 50Ω resistor. This is physically done by shorting the SMA on CLKIN with a 50Ω cap.

The jitter performance on the clock is crucial to obtain optimum performance from the DAC. We thus recommend to use a very low phase noise clock signal if a fixed frequency is used.

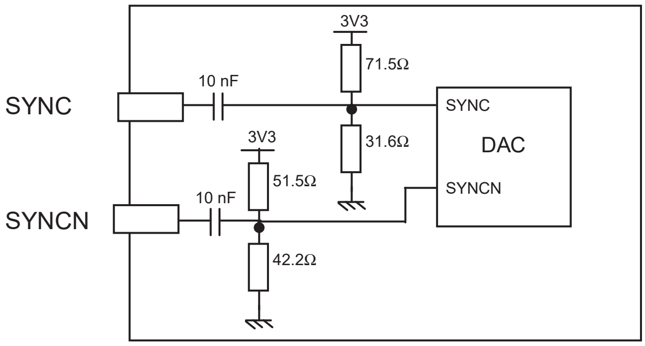
5.3 SYNC Inputs

The SYNC, SYNCN is necessary to start the DAC after power up.

The reset signal is implemented as illustrated in Figure 5-3. We recommend to apply a square LVDS signal.

For customer application, it is recommended to implement a DC coupled SYNC signal without the AC coupling capacitor and pull-up/down resistor shown in Figure 5-3. This setup was implemented on the evaluation board as it made our characterization easier using periodic pulse generator for the SYNC. While the pull-up/down resistors were implemented to characterize and work around a bug of the revA of the EV12DS130. Both this AC coupling capacitor and pull-up/down resistor are not recommended implementation for the SYNC input. Refer to the datasheet for recommendation.

Figure 5-3. SYNC, SYNCN Inputs Implementation

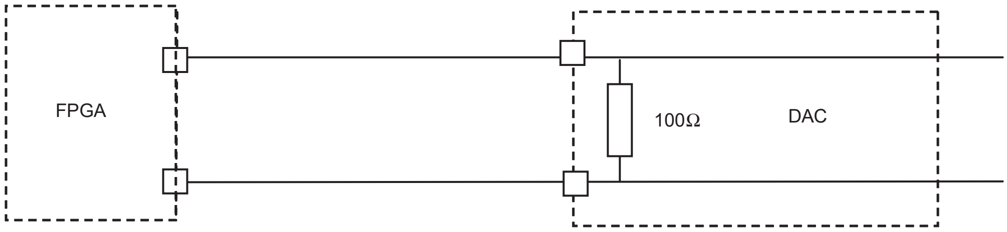


5.4 Input Data

The input data are LVDS differential and are 100Ω on chip terminated to ground as shown in Figure 5-4.

The input data of DAC is generated by the FPGA.

Figure 5-4. Input Data on-board Implementation



5.5 Diode for Junction Temperature Monitoring

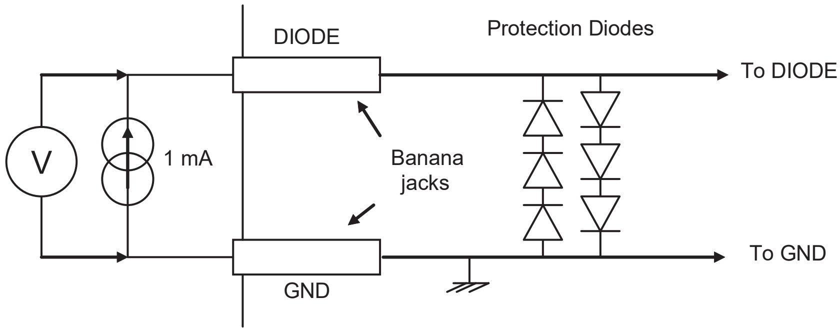
Two 2 mm banana jacks are provided for the die junction temperature monitoring of the DAC.

One banana jack is labeled DIODE and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to GND.

The DAC diode is protected via 2 x 3 head-to-tail diodes.

Figure 5-5 describes the setup for the die junction temperature monitoring using a multimeter.

Figure 5-5. Die Temperature monitoring Test Setup



Note: Protection diodes: NC

Section 6

Ordering Information

Table 6-1. Ordering Information

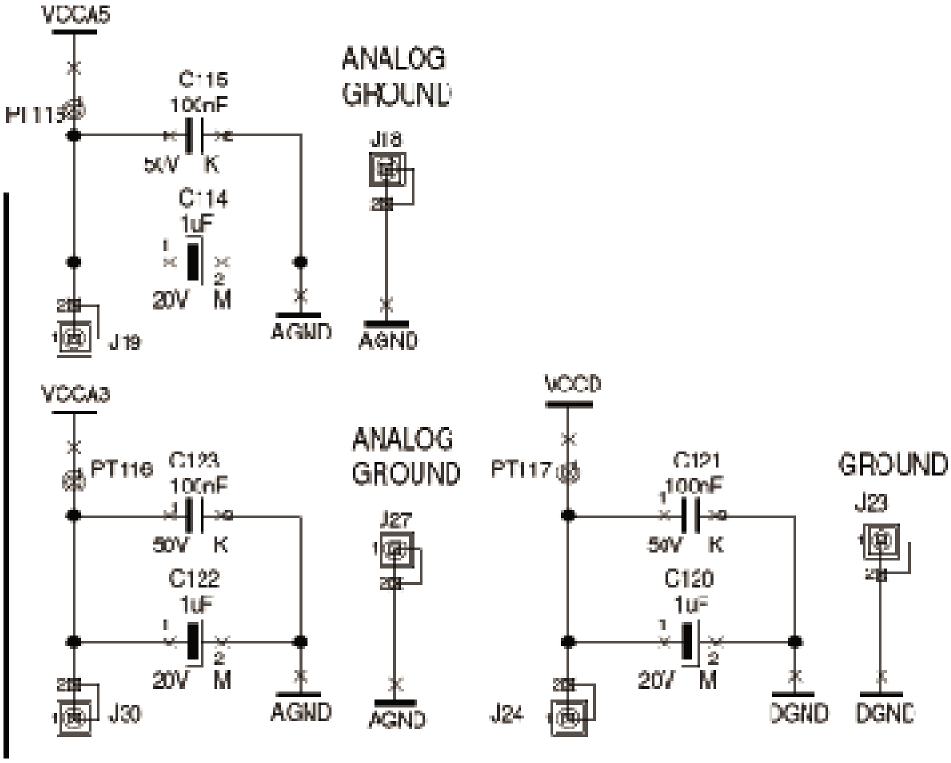
Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS130AGS	CI CGA 255	Ambient	Prototype	
EV12DS130AGS-EB	CI CGA 255	Ambient	Prototype	Evaluation board

Section 7

Appendices

7.1 EV12DS130AGS-EB Electrical Schematics

Figure 7-1. Power Supplies Bypassing



UG 60S 225243(E)–BDC–10/24

Figure 7-2. Power Supplies Decoupling (J = ±5% tolerance)

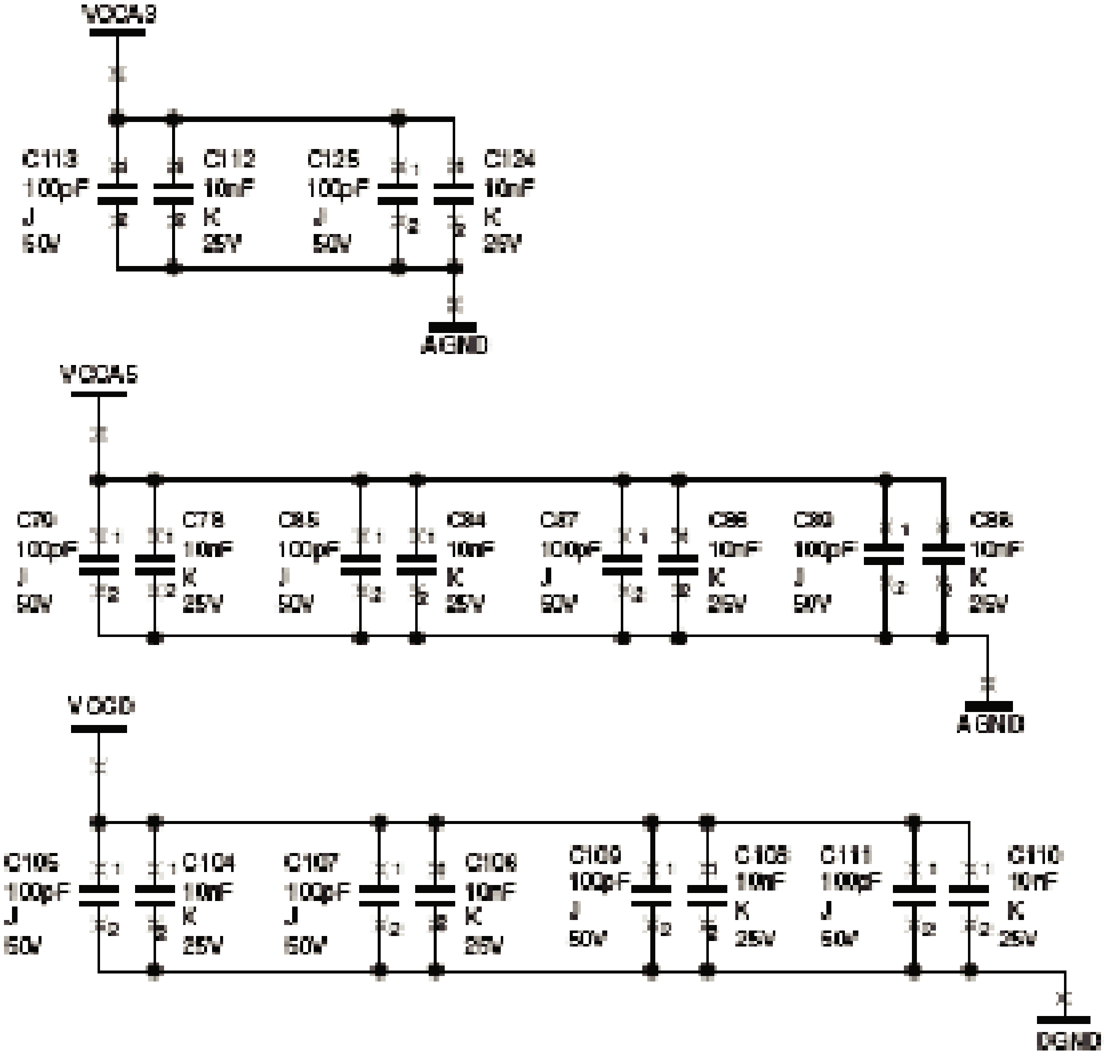
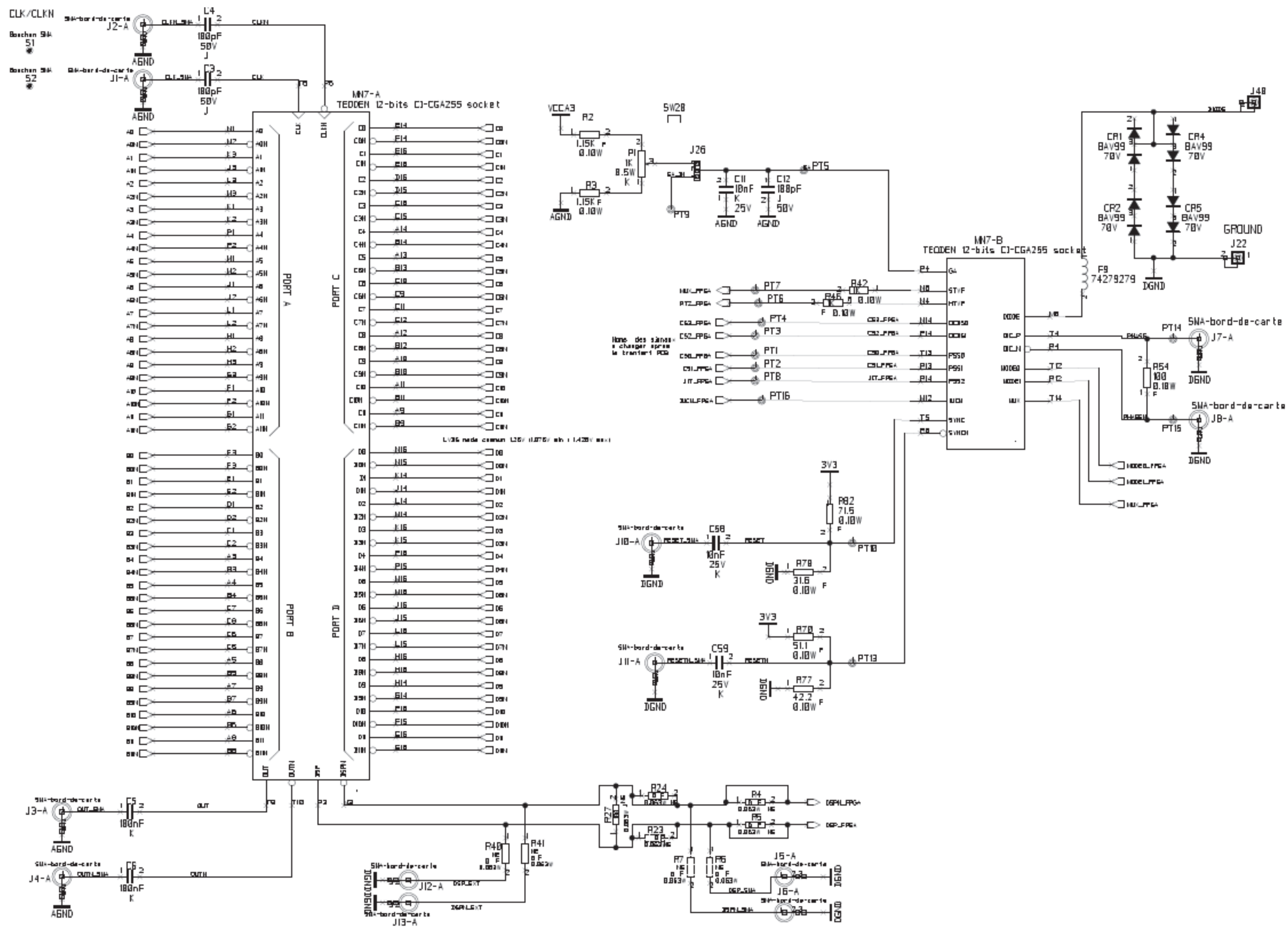


Figure 7-3. Electrical Schematics (DAC)



7.2 EV12DS130AGS-EB Board Layers

Figure 7-4. Top Layers

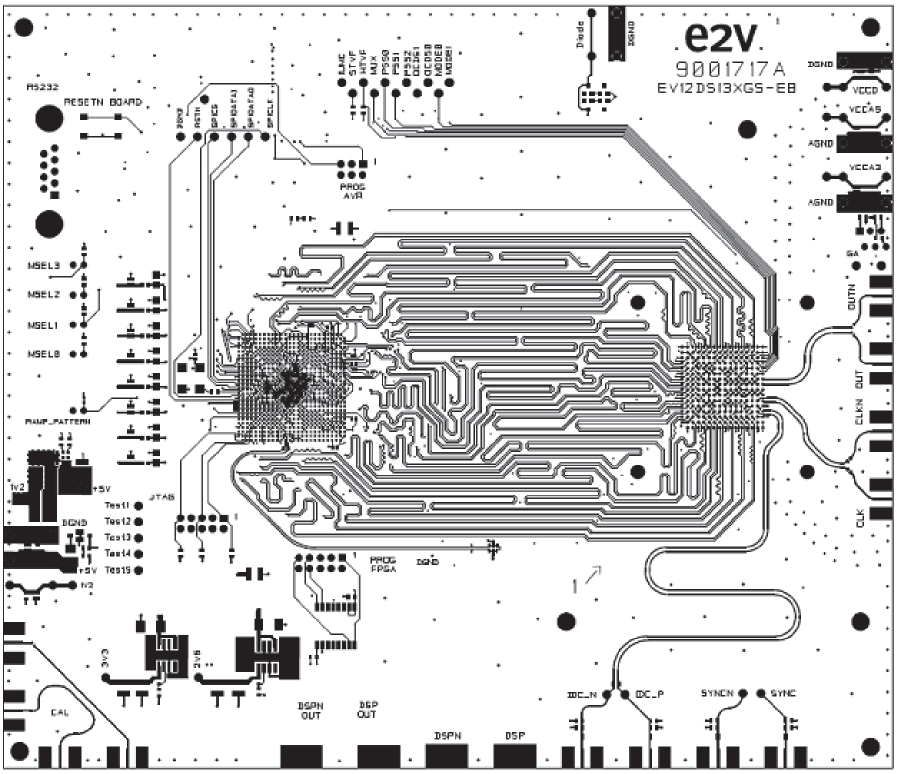


Figure 7-5. Bottom Layer

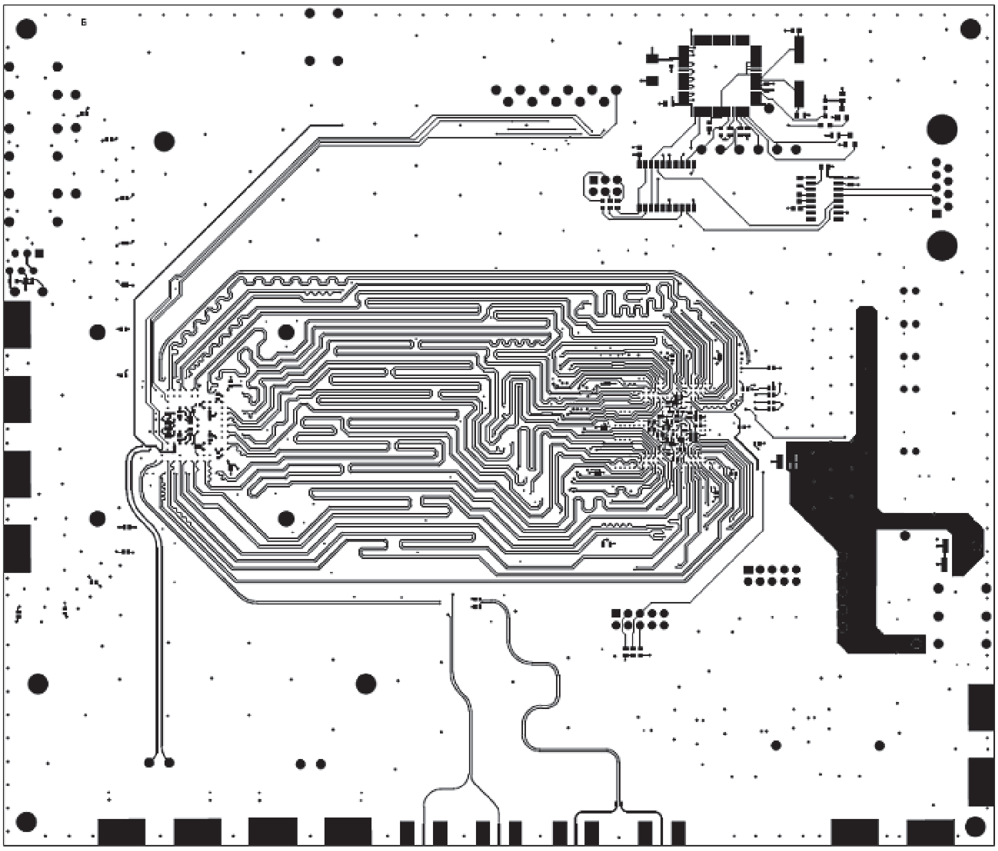


Figure 7-6. Layer 2 GND Plane

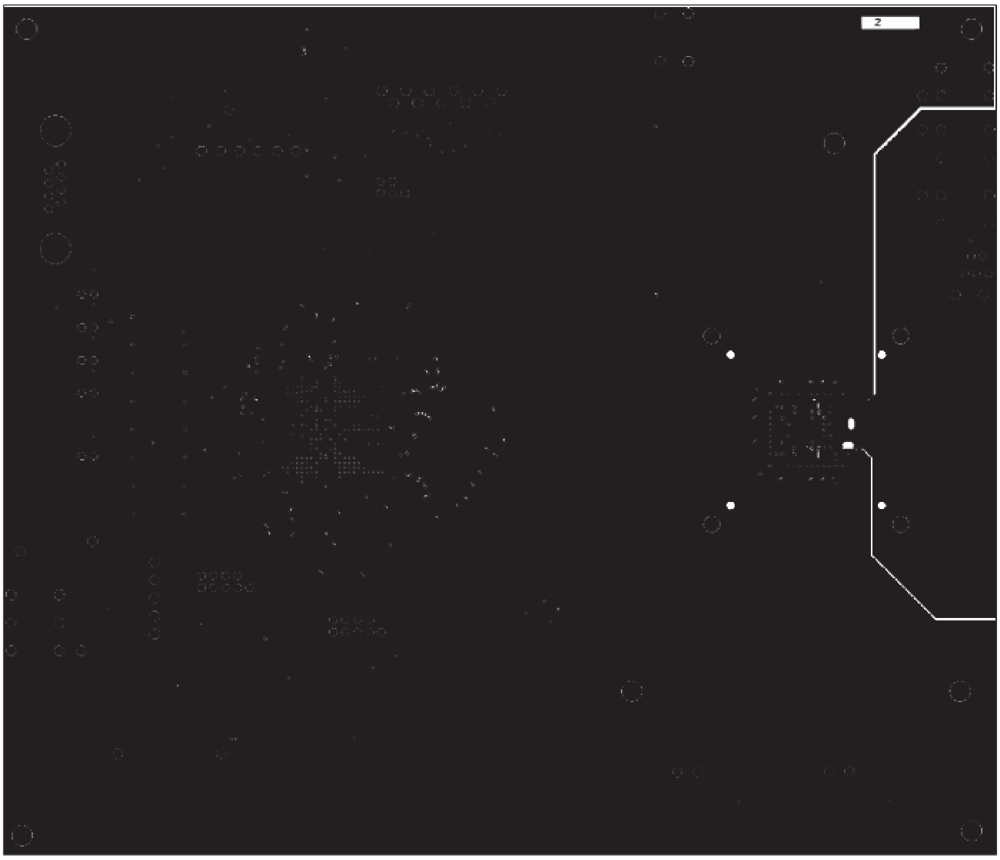
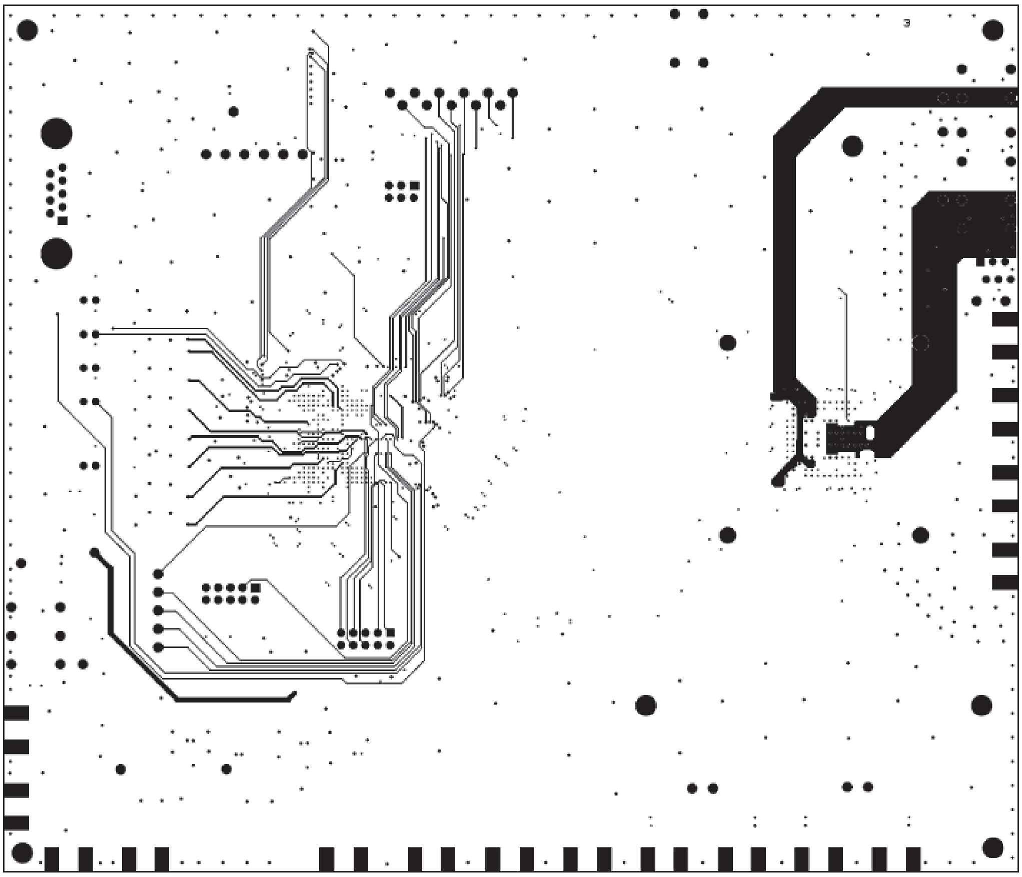


Figure 7-7. Layer 3 Power Supplies



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