1. INTRODUCTION

The EV1xDS130B has been developed in order to have simpler implementation than the EV1xDS130A.

This application note aims at providing you a comparison of the two versions and some recommendations in order to migrate from the EV1xDS130A to the EV1xDS130B.

Despite the two products are fully pin to pin compatible and have the same performance, we strongly recommend EV1xDS130A user's to check the impact of each of the modifications described in this document on their applications before replacing EV1xDS130A with EV1xDS130B.

This document applies to all EV10DS130BG, EV10DS130BZP, EV12DS130BG, and EV12DS130BZP product families and must be read with the latest datasheet version of the product available on www.e2v.com.

For further assistance please contact hotline-bdc@e2v.com.

2. DIFFERENCES BETWEEN EV1XDS130A AND EV1XDS130B

2.1 Power Supply Improvement

2.1.1 Specific Power-up on Vcca5 no more necessary

With EV1xDS130A, it is necessary to raise Vcca5 power supply within the range of 5.2-5.6V during 1 to 500 ms at power-up in order to reduce the noise floor.

With EV1xDS130B, it is no more necessary to apply this sequence in order to have the nominal noise floor.

2.1.2 Power-up sequence no more necessary

With EV1xDS130A, we recommend to respect the following power supply sequence: Vcca5, Vcca3 and finally Vccd to avoid any issue.

With EV1xDS130B, any power sequence can be applied without any risk of issue. In case the power-up sequence is Vccd, Vcca3 and Vcca5, a power-up SYNC pulse is internally and automatically generated.

e2v technologies (uk) limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Holding Company: e2v technologies plc

Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492

Contact e2v by e-mail: enquiries@e2v.com or visit www.e2v.com for global sales and operations centres.

2.2 SYNC Improvement

For the EV1xDS130A only, the errata 1125 is applicable.

2.2.1 External SYNC biasing no more necessary

With EV1xDS130A, it is necessary to bias the SYNCN pin to Vcca3 via an external 1500Ω pull-up resistor, and to bias the SYNCP pin to DGND via an external 910Ω pull-down resistor.

With EV1xDS130B, the SYNC pins are internally biased without any external component needed.

2.2.2 Voltage dependency between Vccd and Vcca no more necessary

With EV1xDS130A, in case the SYNC function is required by the application, it is mandatory to ensure that Vcca3 is 150mV higher than Vccd.

With EV1xDS130B, the SYNC function is available as soon as power supplies are within specification without any dependency.

2.2.3 No more SYNC timing constraints

With EV1xDS130A, a lot of caution should be taken in order to ensure a good SYNC: power sequence or difference in voltage between Vcca3 and Vccd, SYNC rising edge…

With EV1xDS130B, to ensure the synchronization of several DACs, the only constraints are the timing T1 and T2 specified in the datasheet to avoid metastable zone.

2.3 DSP Clock Modification

2.3.1 DSP clock always stops on a low level

With EV1xDS130A, when a SYNC is applied, in case the PSS value is not 0, the DSP clock could stop at any logical level (high or low).

With EV1xDS130B, when a SYNC is applied, the DSP clock always stops at a high level, ensuring a deterministic restart of the DSP clock whatever the PSS value is.

2.3.2 DSP clock functionality available up to 2.1 Gsps

With EV1xDS130B, as a side effect of all the corrections mentioned above, the DSP clock is only ensured up to 2.1 Gsps in MUX4:1, while there is no limitation in MUX2:1.

In case clock frequency is higher than 2.1GHz, some jitter could appear on the DSP so that we recommend the use of an external PLL in order to recreate a DSP clock signal from the clock frequency (See Application Note 1141).

For any question, please contact hotline-bdc@e2v.com.

3. REVISION HISTORY

This table provides revision history for this document.

Table 3-1. Revision History

Rev. No	Date	Substantive Change(s)
1140B	10/2015	Section 2.2.3. error corrected concerning EV1xDS130B
1140A	10/2014	Initial revision