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EV10DS130AZPY-EB Evaluation Board 10-bit DAC with 4/2:1 MUX

User Guide

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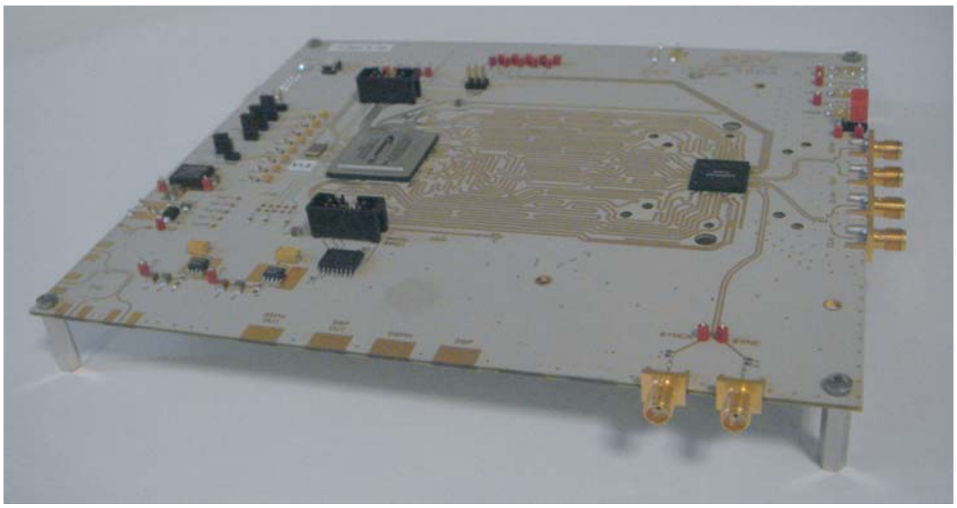
Section 1

Introduction

1.1 Scope

The EV10DS130AZPY-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the EV10DS130A 10-bit DAC with 4/2:1 MUX in fpBGA package.



The EV10DS130AZPY-EB Evaluation Kit includes:

- 1 MUXDAC evaluation board,
- A cable for connection to the RS-232 port,
- 1 CD-ROM that contains the software Tools necessary to use the SPI.

The evaluation system of the EV10DS130A MUXDAC device consists in a configurable printed circuit board, including the soldered MUXDAC device, a FPGA, a serial interface and a user interface running on that platform.

This user guide should be read in parrallel of the product datasheet and the relative application note.

1.2 Description

The EV10DS130AZPY Evaluation board is very straightforward as it implements e2v EV10DS130A 10-bit MUXDAC device, ALTERA FPGA, SMA connectors for the sampling clock, analog outputs and reset inputs accesses.
Thanks to its user-friendly interface, the EV10DS130AZPY-EB Kit enables to test all the functions of the EV10DS130A 10-bit MUXDAC.

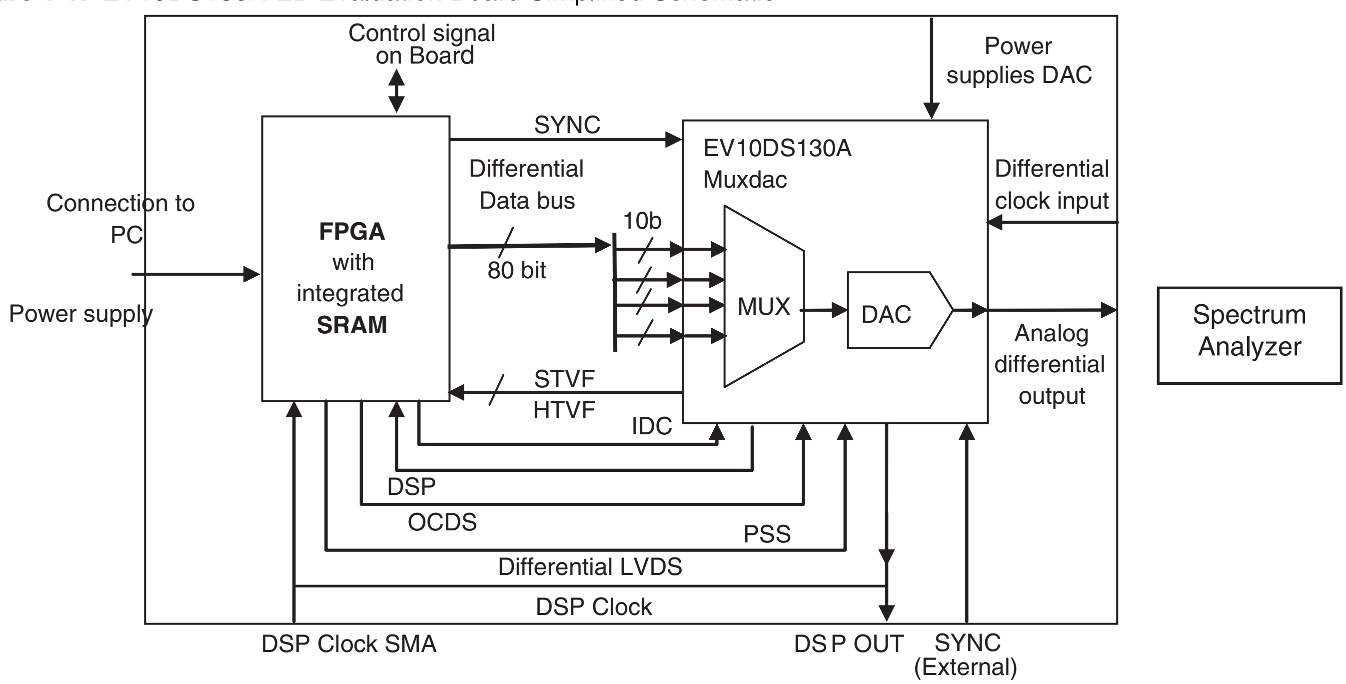
To achieve optimal performance, the EV10DS130AZPY-EB designed in a 6-metal-layer board using RO4003 epoxy dielectric material. The board implements the following devices:

- The EV10DS130AZPY 10-bit MUXDAC Evaluation board with the EV10DS130AZPY 10-bit MUXDAC soldered,
- SMA connectors for CLK, CLKN, OUT, OUTN, SYNC, SYNCN, DSP, DSPN, DSP OUT, DSPN OUT and CAL,
- ALTERA FPGA soldered to generated the logical pattern,
- Banana jacks for the power supply accesses, the Die junction Temperature monitoring functions, reference resistor,
- An RS-232 connector for PC interfaces.

The board dimensions are 180 mm × 210 mm.

The board comes fully assembled and tested with the EV10DS130A installed.

Figure 1-1. EV10DS130A-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CCA5} = 5V analog positive power supply,
- V_{CCD} = 3.3V digital positive power supply,
- V_{CCA3} = 3.3V analog output power supply,
- 5V FPGA.

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Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full speed operation of the EV10DS130AZPY-EB 10-bit MUXDAC, a multi-layer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in RO4003 dielectric material.

The following table gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
RO4003 / dielectric layer	Layer thickness = 200 µm
Layer 2 Copper layer	Copper thickness = 18 µm Ground plane = AGND – DGND plane
RO4003 / dielectric layer	Layer thickness = 350 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power plane = FPGA supplies, V_{CCD}, $V_{CCA3,}$ Signals
RO4003 / dielectric layer	Layer thickness = 350 µm
Layer 4 Copper layer	Copper thickness = 18 µm Reference plane = ground and power plane
RO4003 / dielectric layer	Layer thickness = 350 µm
Layer 5 Copper layer	Copper thickness = 18 µm Power planes = DGND, $V_{CCA5,}$ GA plane
RO4003 / dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces

The board is 1.6 mm thick.

2.2 Analog Outputs

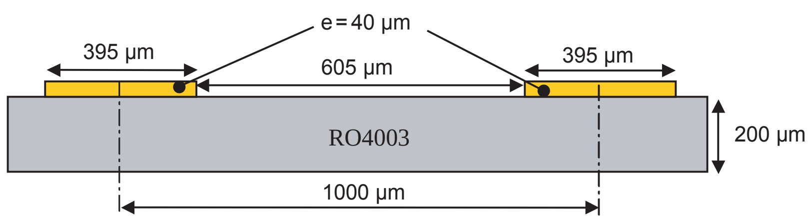
The differential analog output is provided by SMA connectors (Reference: VITELEC 142-0701-8511).

Both pairs are AC coupled using 100 nF capacitors. (Reference ATC545L Series UBC).

Special care was taken for the routing of the analog output signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between OUT and OUTN,
- 605 µm pitch between the differential traces,
- 1000 µm between two differential pairs,
- 395 µm line width,
- 40 µm thickness,
- 850 µm diameter hole in the ground layer below the OUT and OUTN ball footprints.

Figure 2-1. Board Layout for the Differential Analog and Clock Inputs



Note: The analog output is AC coupled with 100 nF very close to the SMA connectors.

2.3 Clock Inputs

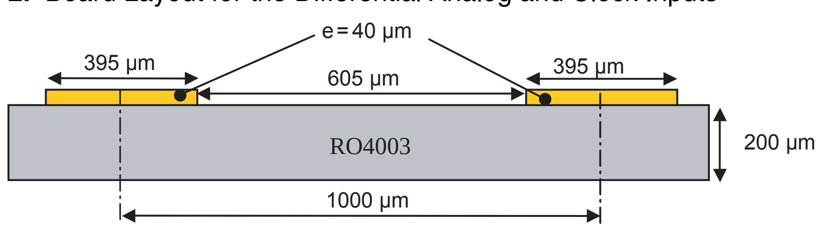
The differential clock inputs is provided by SMA connectors (Reference: VITELEC 142-0701-8511).

Both pairs are AC coupled using 100 pF capacitors.

Special care was taken for the routing of the clock input signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between CLK and CLKN,
- 605 µm pitch between the differential traces,
- 1000 µm between two differential pairs,
- 395 µm line width,
- 40 µm thickness,
- 850 µm diameter hole in the ground layer below the CLK and CLKN ball footprints.

Figure 2-2. Board Layout for the Differential Analog and Clock Inputs



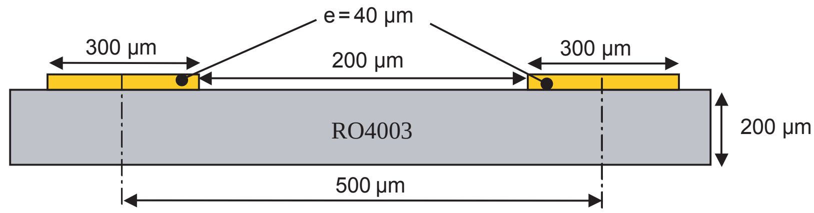
Note: The clock input is AC coupled with 100 nF very close to the SMA connectors.

2.4 Digital Inputs

The digital input lines were designed with the following recommendations:

- 50Ω lines matched to ±2.5 mm (in length) between signal of the same differential pair,
- ±1 mm line length difference between signals of two differential pairs,
- 500 µm pitch between the differential traces,
- 650 µm between two differential pairs,
- 300 µm line width,
- 40 µm thickness.

Figure 2-3. Board Layout for the Differential Digital Outputs



The digital inputs are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

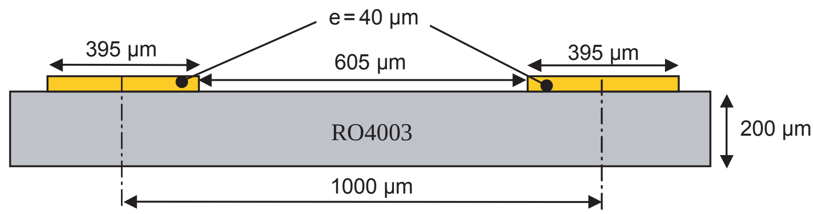
2.5 SYNC Inputs

The hardware reset signals are provided; SYNC, SYNCN corresponds to the reset of the output of the DAC (analog reset).

The differential reset inputs are provided by SMA connectors (Reference: VITELEC 142-0701-8511).The signals are AC coupled using 10 nF capacitors and pulled up and down resistors.

- 50Ω lines matched to ±0.1 mm (in length) between SYNC and SYNCN,
- 605 µm pitch between the differential traces,
- 1000 µm between two differential pairs,
- 395 µm line width,
- 40 µm thickness.

Figure 2-4. Board Layout for the SYNC Signal



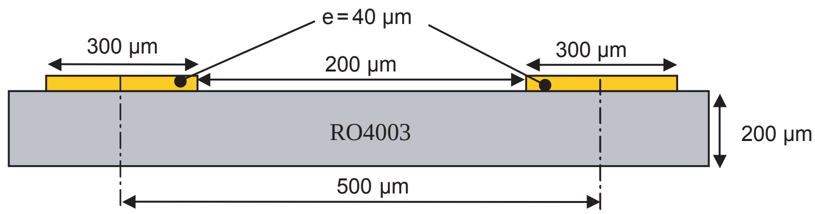
2.6 DSP, DSPN Signals Inputs

The differential DSP and DSPN signals can be provided by the SMA connectors (not connected).

Special care was taken for the routing of DSP, DSPN signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between DSP and DSPN,
- 500 µm pitch between the differential traces,
- 650 µm between two differential pairs,
- 300 µm line width,
- 40 µm thickness.

Figure 2-5. Board Layout for the DSP Signal



These signals are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

DSP, DSPN are not used for normal operation. They can be left open.

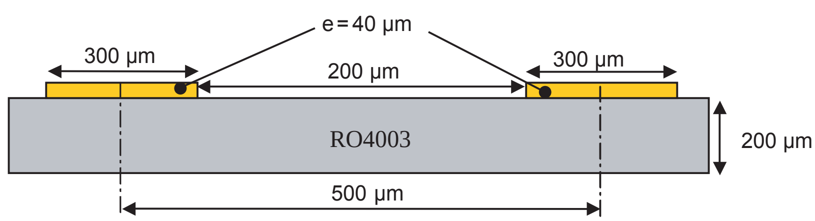
2.7 DSP OUT, DSPN OUT Signals Outputs

The differential DSP OUT and DSPN OUT signals can be provided by the SMA connectors (not connected).

Special care was taken for the routing of DSP OUT, DSPN OUT signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between DSP OUT and DSPN OUT,
- 500 µm pitch between the differential traces,
- 650 µm between two differential pairs,
- 300 µm line width,
- 40 µm thickness.

Figure 2-6. Board Layout for the DSP OUT Signal



These signals are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

DSP, DSPN are not used for normal operation. They can be left open.

2.8 CALIBRATION Lines

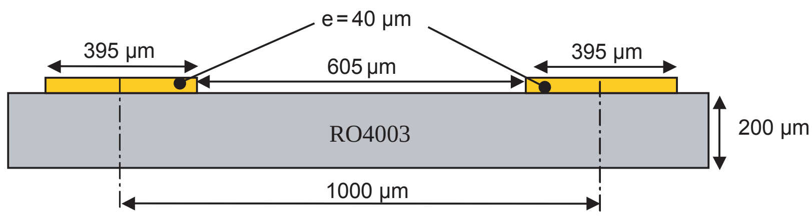
Both pairs are AC coupled using 100 nF capacitors. (Reference ATC545L Series UBC).

Calibration lines have exactly the same length than Analog Outputs.

Special care was taken for the routing of the analog output signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between CAL and CALN,
- 605 µm pitch between the differential traces,
- 1000 µm between two differential pairs,
- 395 µm line width,
- 40 µm thickness,
- 850 µm diameter hole in the ground layer below the CAL and CALN ball footprints.

Figure 2-7. Board Layout for the Differential Analog and Clock Inputs



Note: The calibration lines are AC coupled with 100 nF very close to the SMA connectors.

2.9 Power Supplies

Layers 3, 4 and 5 are dedicated to power supply planes (V_{CCA3}, V_{CCD}, V_{CCA5} and 5V FPGA)

The supply traces are low impedance and are surrounded by two ground planes (layer 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply is decoupled as close as possible to the EV10DS130A device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the EV10DS130A 10-bit MUXDAC.

The analog output signal and the sampling clock signal should be in a differential fashion.

Note: The analog outputs and clock are AC coupled on the board.

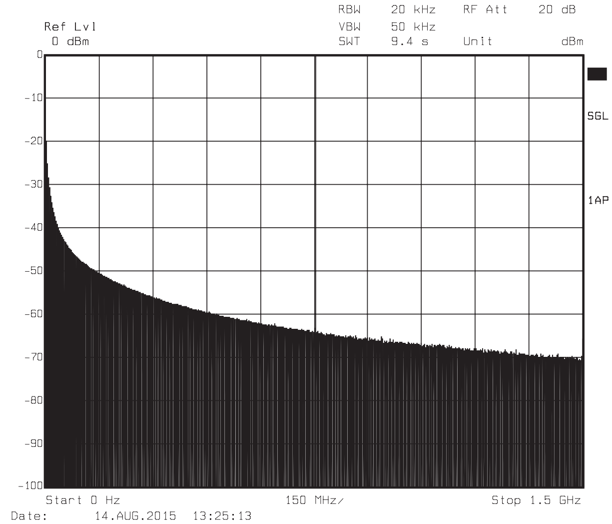
3.2 Operating Procedure

1. Install the SPI software as described in section 4 "Software Tools".
2. Connect the power supplies and ground accesses through the dedicated banana jacks.
   V_{CCA3} = 3.3V, V_{CCD} = 3.3V, V_{CCA5} = 5V and for the FPGA +5V
3. Connect the clock input signals.
   The clock input level is typically 3 to 10 dBm and should not exceed 12 dBm (into 50Ω).
4. Connect the analog output signals (the board has been designed to allow only AC coupled analog outputs). The analog output signals must be used in differential via differential-to-single transformer.
5. Connect the PC's RS-232 connector to the Evaluation Board's serial interface.
6. Switch on the DAC power supplies: for optimum noise performance follow power on sequence for Vcca5 described on datasheet.
7. Turn on the RF clock generator.
8. Switch on the FPGA power supply
9. Perform an analog reset on the device.
10. Launch software. (software must be lunch with evaluation board power ON)

The EV10DS130AZPY-EB evaluation board is now ready for operation.

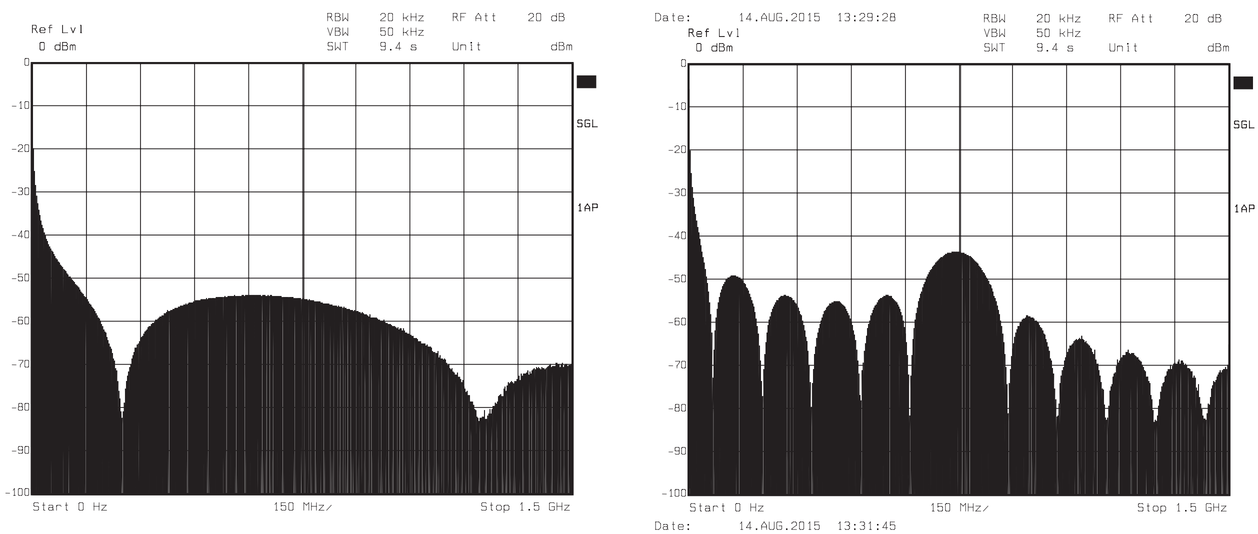
Note: To use the software, you should be in Administrator mode.

Figure 3-1.
The following graph shows a good synchronization.



If you have not ramp (cf: graphs below) on the output, push reset board or turn off power and restart.

Figure 3-2.



When using patterns, clock can be set at any value from 300 Msps up to 3 Gsps in the initial configuration [OCDS: 00 and PSS: 0]. However one may loose FPGA-DAC synchronization upon clock frequency change. For resynchronization, a hard reset (board reset button) followed by a pattern reload will be required.

3.3 Electrical Characteristics

For more information, please refer to the device datasheet. See section 3.2 of datasheet.

Table 3-1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RESOLUTION			10		bit	
ESD CLASSIFICATION			Class 1B			
POWER REQUIREMENTS						
Power Supply voltage - Analogue - Analogue - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	 V V	
Power Supply current (4:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 83.7 106 186.9	 mA mA mA	
Power Supply current (2:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 83.7 106 159.6	 mA mA mA	
Power dissipation (4:1 MUX)	P_D		1.38		W	
Power dissipation (2:1 MUX)	P_D		1.29		W	

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Section 4

Sofware Tools

4.1 Overview

The MUXDAC 10-bit Evaluation user interface software is a Visual C++ compiled graphical interface that does not require a licence to run on a Windows NT and Windows 2000/98/XP PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Configuration

The advised configuration for Windows 98 is:

- PC with Intel Pentium Microprocessor of over 100 MHz,
- Memory of at least 24 Mo.

For other versions of Windows OS, use the recommended configuration from Microsoft.

Note: Two COM ports are necessary to use two boards simultaneously.

4.3 Getting Started

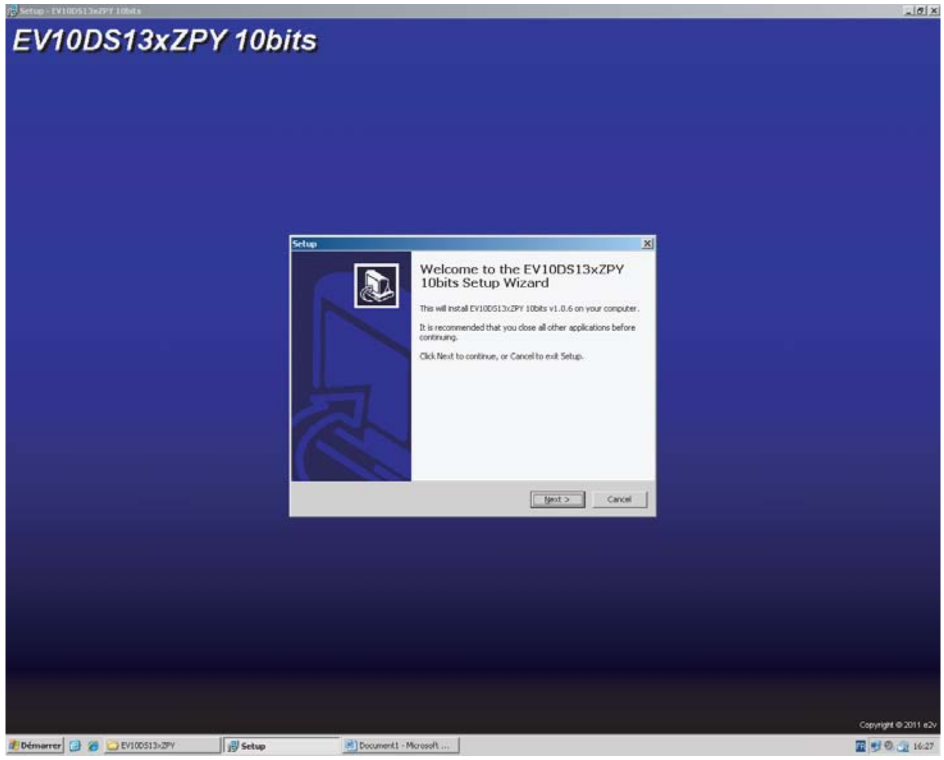
1. Install the 10-bit MUXDAC application on your computer by launching the Setup_EV10DS13xZPY.exe install (please refer to the latest version available).

The screen shown in Figure 4-1 is displayed:

Figure 4-1. Application "Setup wizard" window

Setup process will start with this first information screen.

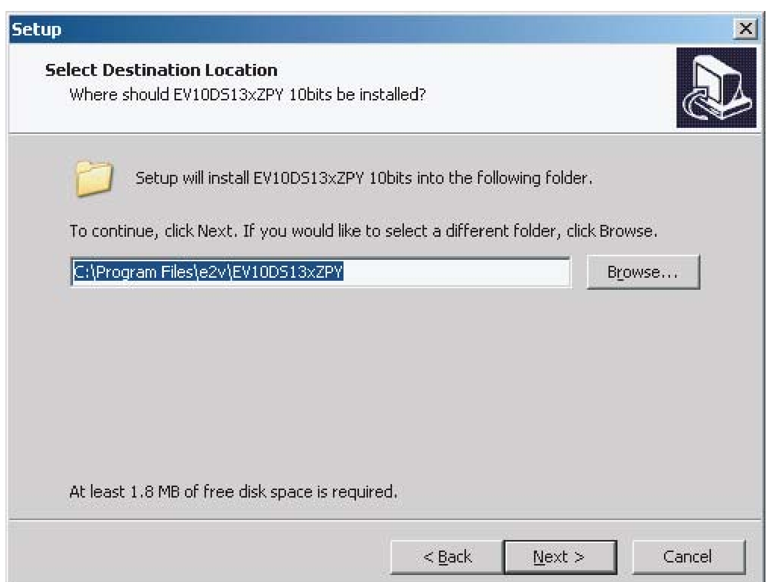
Click on **Next** to step to the next screen



2. Select Destination Location

Figure 4-2. "Select Destination Location" Window

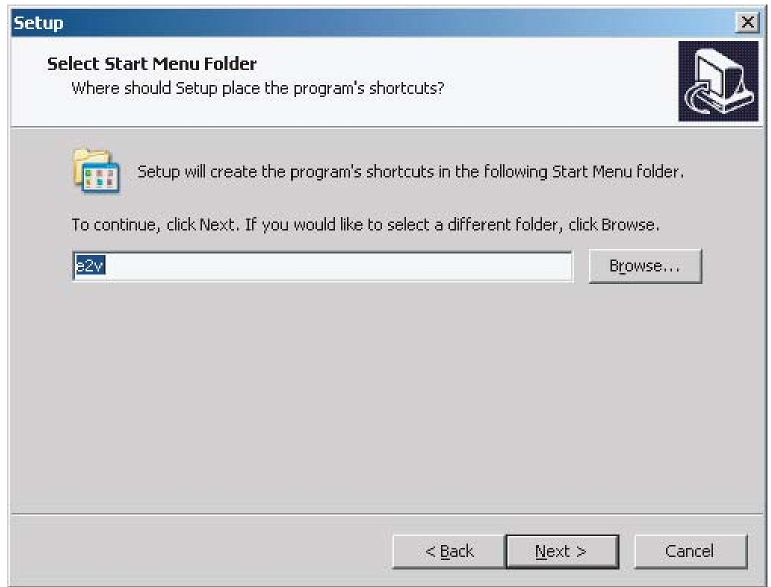
This dialog displays destination Location of application. Change it to your convenience, or choose it by clicking on **Next** button.



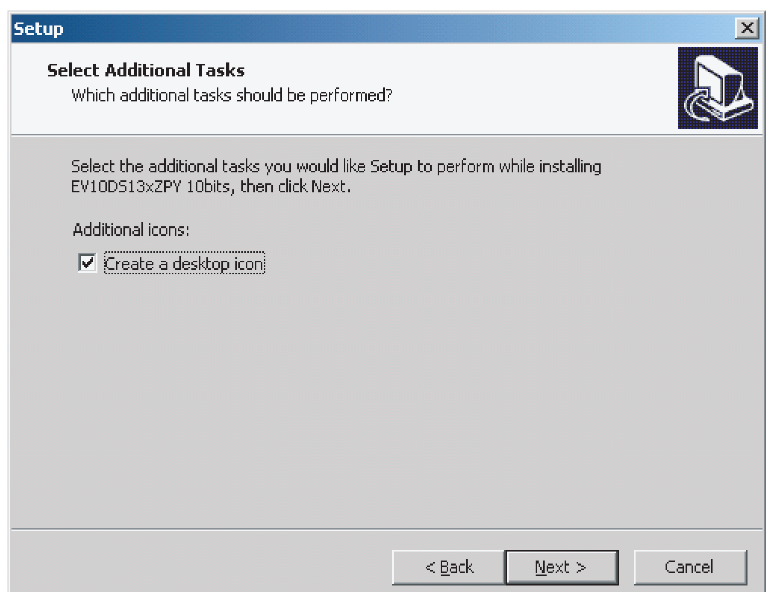
3. Select Start Menu Folder

Figure 4-3. "Select Start Menu Folder" window

Next dialog displays Start Menu entry to store application shortcut. Change it to your convenience, or choose it by clicking on **Next** button.



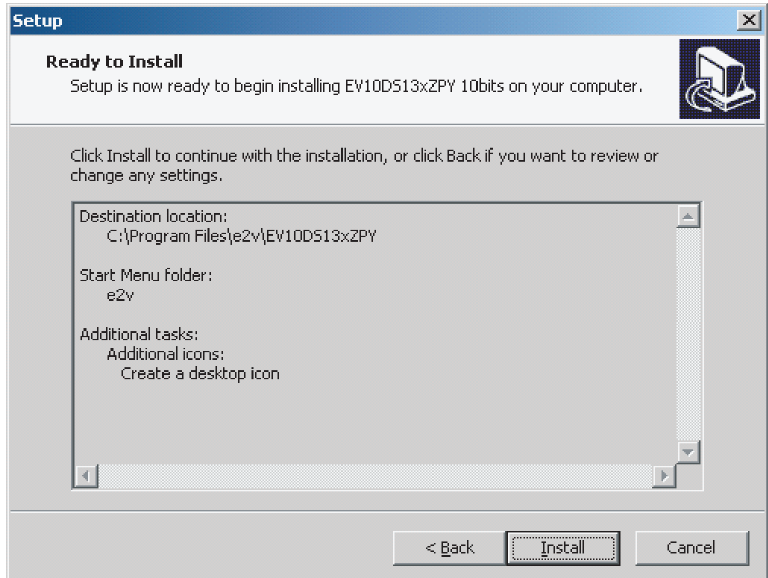
Next dialog asks you if you want an application shortcut on your desktop. Change it to your convenience, or choose it by clicking on **Next** button.



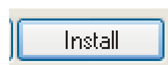
4. Ready to install

Figure 4-4. "Ready to Install" window

Next dialog shows a resume about operations setup that will be performed to complete installation.



If you're agreeing, click on **Install** to start it.



At the end of the installation, the dialog box below appears. Click on **OK** to end the installation.

Note: If this dialog box does not appear please install the setup vcredist_x86.exe available in the "My program dependencies" file of the CD.

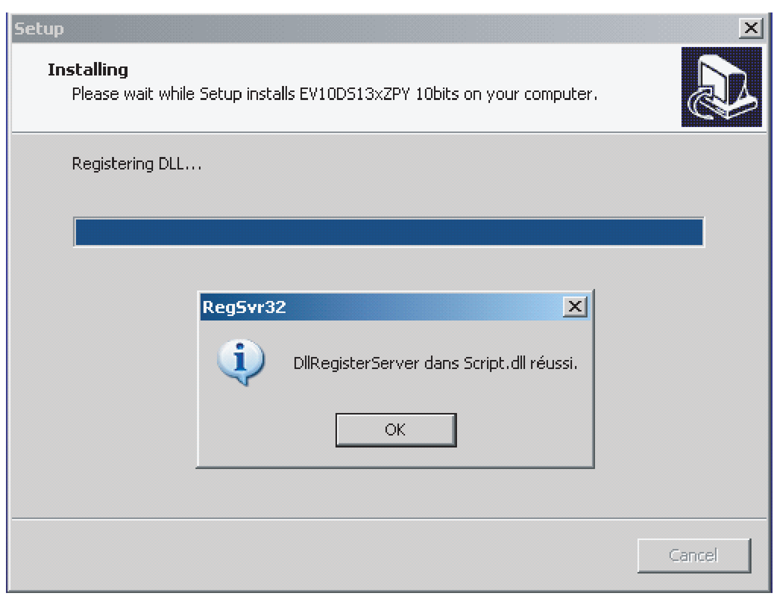
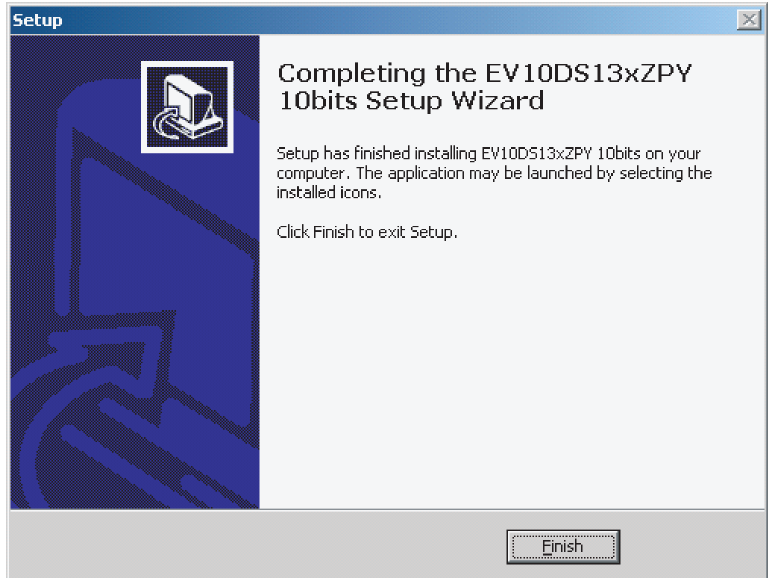


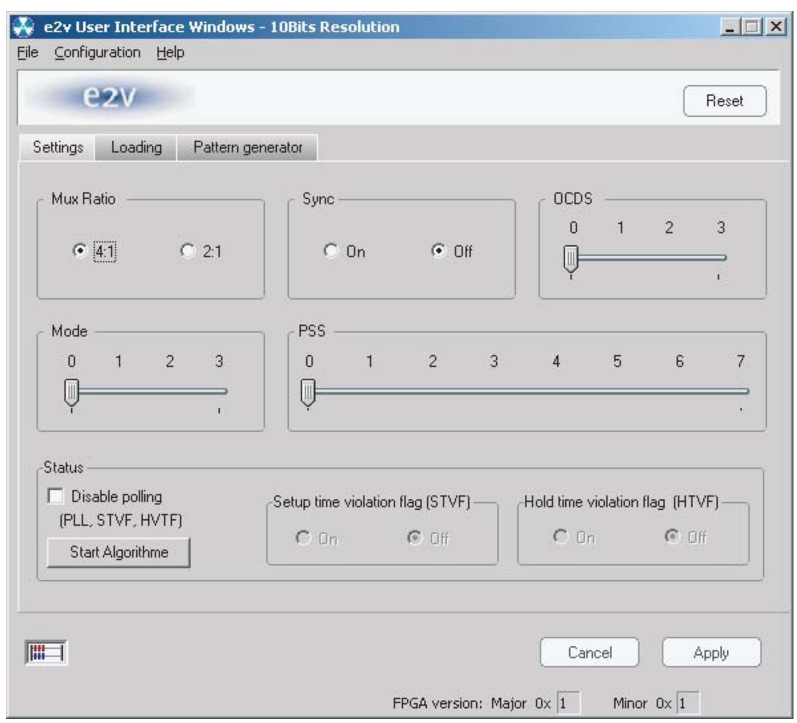
Figure 4-5. "Completing Setup wizard" window



Setup is now completed successfully. You can start application by double clicking on the following icon on your desktop.

The window shown in Figure 4-6 will be displayed.

Figure 4-6. "User Interface" Window



4.4 Troubleshooting

1. check that you own rights to write in the directory
2. check for the available disk space
3. check that at least one RS-232 serial port is free and properly configured
4. check that the serial port and DB9 connector are properly connected
5. check that all supplies are properly powered on

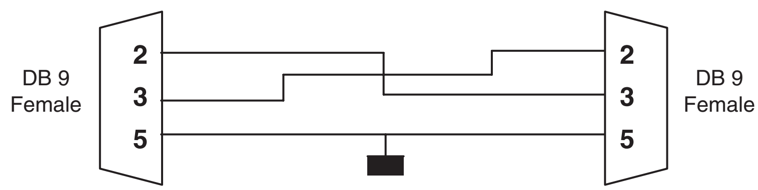
The serial port configuration should be as fallows:

- bit rate: 19200
- Data coding: 8 bits
- 1 start bit, 1 stop bit
- No parity check

Figure 4-7. User Interface Hardware Implementation

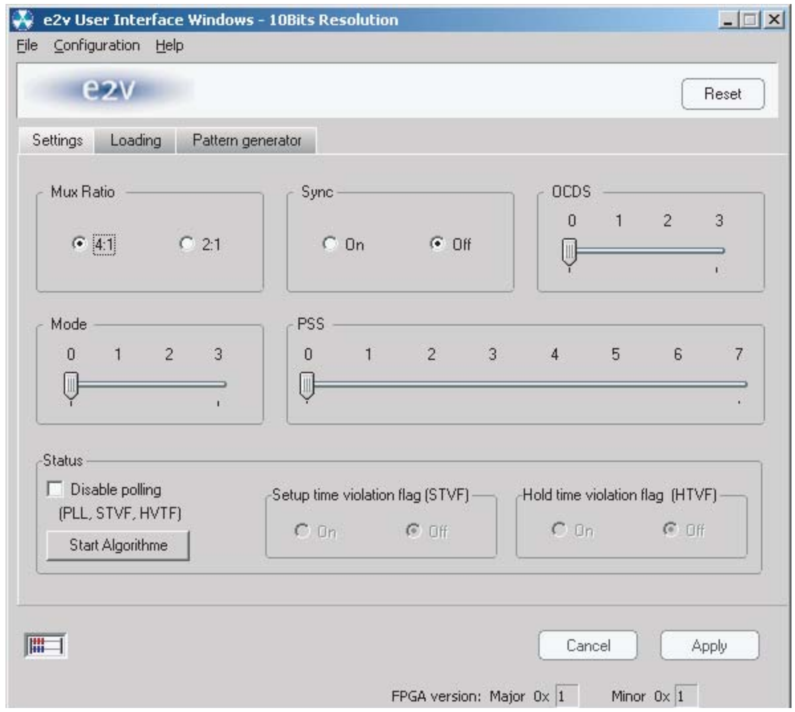
1. use an RS-232 port to send data to the DAC
2. connect the crossed DB9 (F/F) cable between your PC and your evaluation board as illustrated in Figure 4-8.

Figure 4-8. Crossed Cable

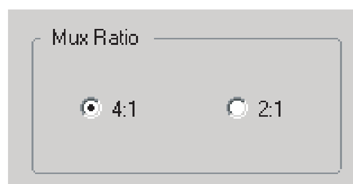


4.5 Operating Modes

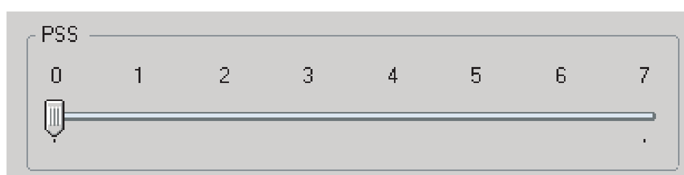
4.5.1 Setting



The software allows choosing between the Mux Ratio 2 to 1 or 4 to 1

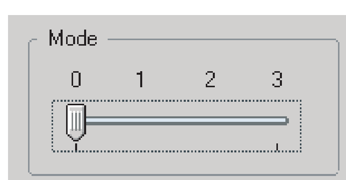


The software allows adjusting the "PSS" (Phase Shift Select) delay to avoid a forbidden timing area between the data input and the clock input. The PSS step is 0.5*Tclk.



Mode Function:

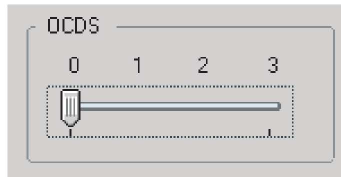
The MODE Function allows choosing between NRZ, reshaped NRZ, RTZ and RF functions.



Label	Value	Description	Default setting	Position (IHM)
MODE[1:0]	00	NRZ mode	00 NRZ mode	0
	01	Narrow RTZ (NRTZ)		1
	10	RTZ Mode (50%)		2
	11	RF		3

OCDS Function:

The software allows changing the DSP clock internal division factor from 1 to 2, 4 or 8.

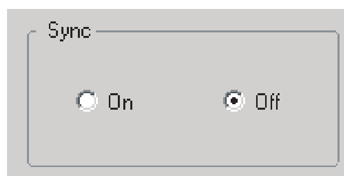


Label	Value	Description	Default setting	Position (IHM)
OCDS[1:0]	00	DSP clock frequency is equal to the sampling clock divided by 2N	00	0
	01	DSP clock frequency is equal to the sampling clock divided by 2N*2		1
	10	DSP clock frequency is equal to the sampling clock divided by 2N*4		2
	11	DSP clock frequency is equal to the sampling clock divided by 2N*8		3

Note: For more details see Erratasheet on OCDS.

SYNC Function:

The SYNC function allows reseting DAC

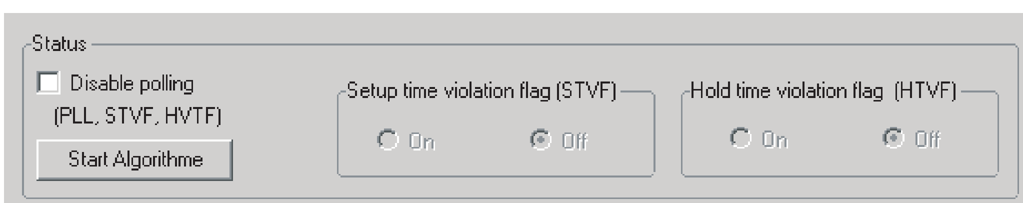


Note: Use function when DAC is not synchronizes.

Status Function:

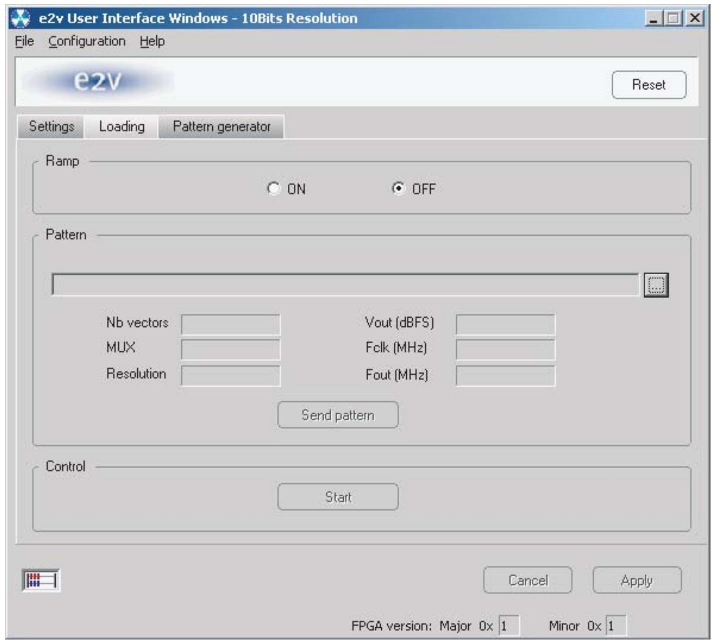
The polling function allows scanning the FPGA to known the FGPA version and the PLL state. Setup time violation flag and Hold time violation flag used allow knowing if DAC are sampling correctly datas which are sent by the FPGA.

Press "Start Algorithm" for automatic function. Algoritm allow avoiding a forbidden timing but this is not optimum position.



4.5.2 Loading

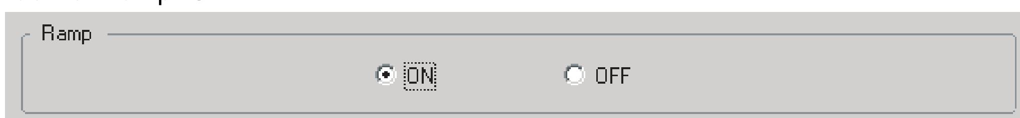
This module allows to send to pattern to the MUXDAC.



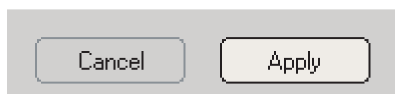
We can choose to send a ramp pattern or to send a dedicated pattern.

For ramp pattern:

- active "Ramp" ON

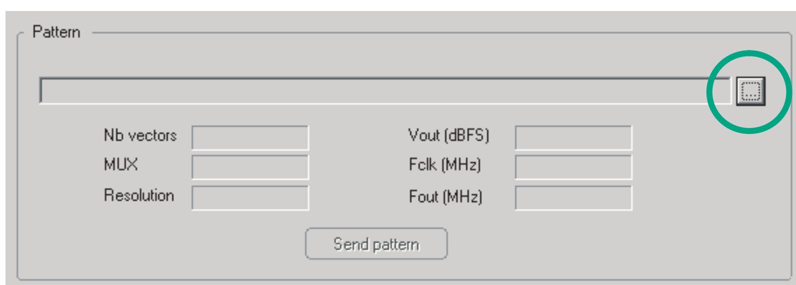


- Press Apply

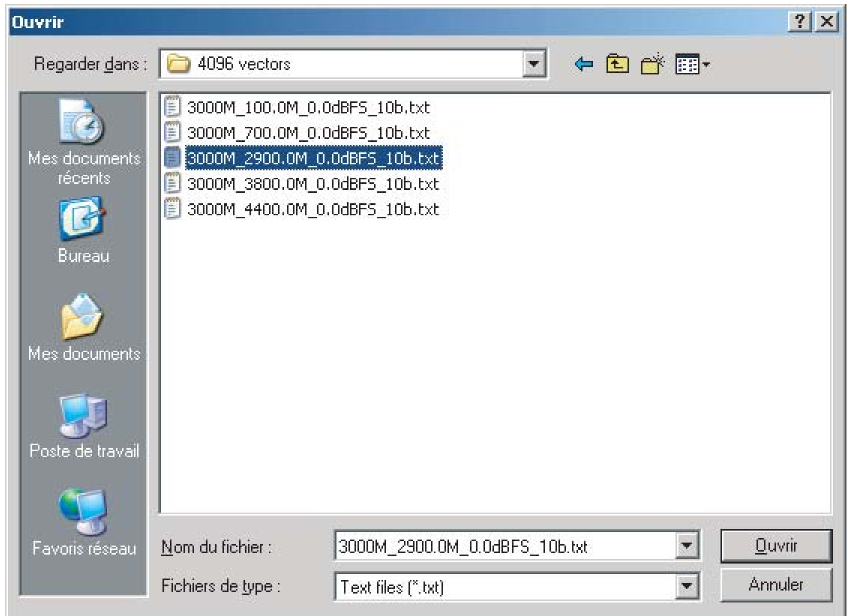


For dedicated pattern:

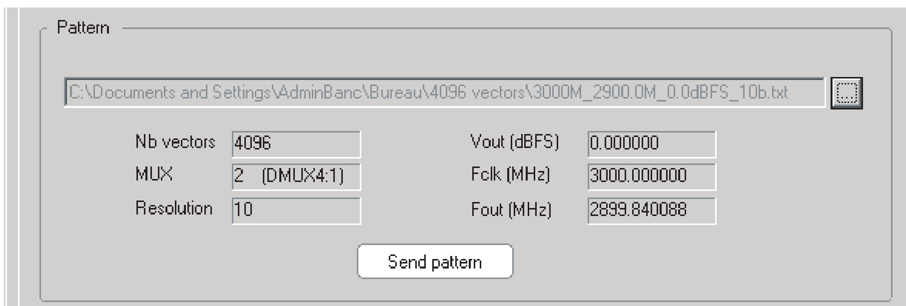
- Find the pattern file in the Folders architecture



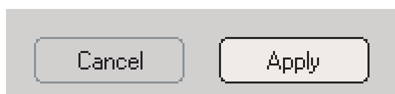
- Check the information (nb vectors, Mux …)



- Press Send pattern

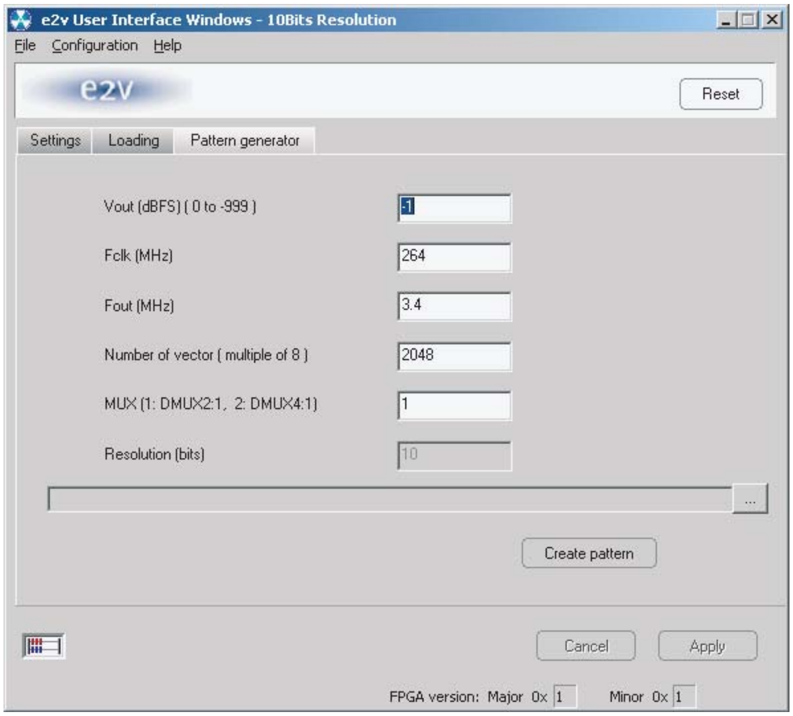


- Press Start



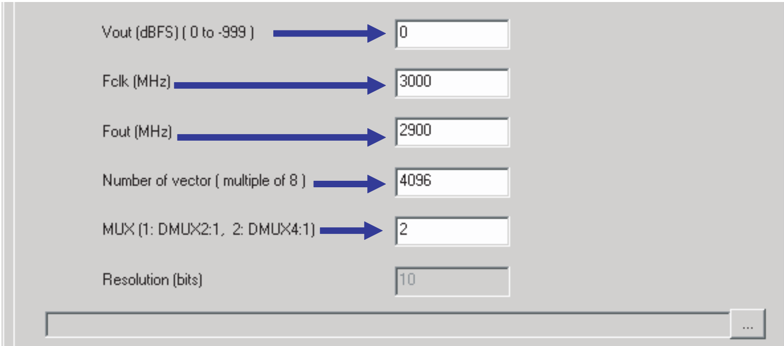
4.5.3 Pattern Generator

This module allows creating sinewave pattern file only in order to send the data to the MuxDac.



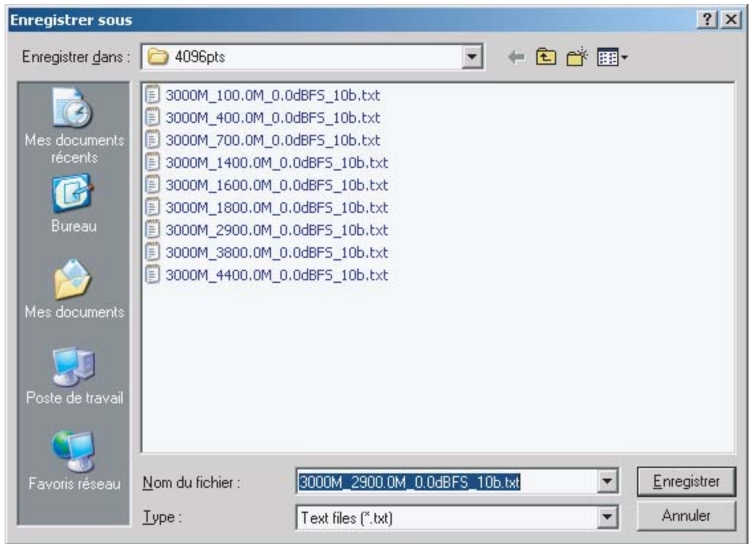
Pattern generator procedure:

- Put information for each field.



Note: Not to exceed 4096 vectors with this generator otherwise it generates spurs in the FFT spectrum.

- Put the way of the target folder to save the pattern



- Push "create pattern"

If you wish to create your own pattern file, please make sure to follow the below example.

<u>Example of Pattern file</u>

Vout (dBFS) 0

Fclk (MHz) 3000

Fout (MHz) 998.108

MUX 2 DMUX4:1

Nb vectors 4096

#

Vector 0:	1000000000	1110111101	0001000010	0111100111
Vector 1:	1110111101	0001000111	0111111111	1111000001
Vector 2:	0001000011	0111101110	1111000100	0001010000
Vector 3:	0111101110	1111001111	0001011101	0111100110
Vector 4:	1111001010	0001010011	0111011110	1111001101
Vector 5:	0001011001	0111010101	1111010000	0001011110

………………………………………………………………………… …..
……………………………………………………………… ……………..
……………………………………………………………… ……etc…….

Vector 4092:	0000110101	1000010111	1110110011	0000100001
Vector 4093:	1000010100	1110111101	0000111010	1000001011
Vector 4094:	1110111011	0000111101	1000001001	1110011000
Vector 4095:	0001000010	1000011000	1110100101	0001001110

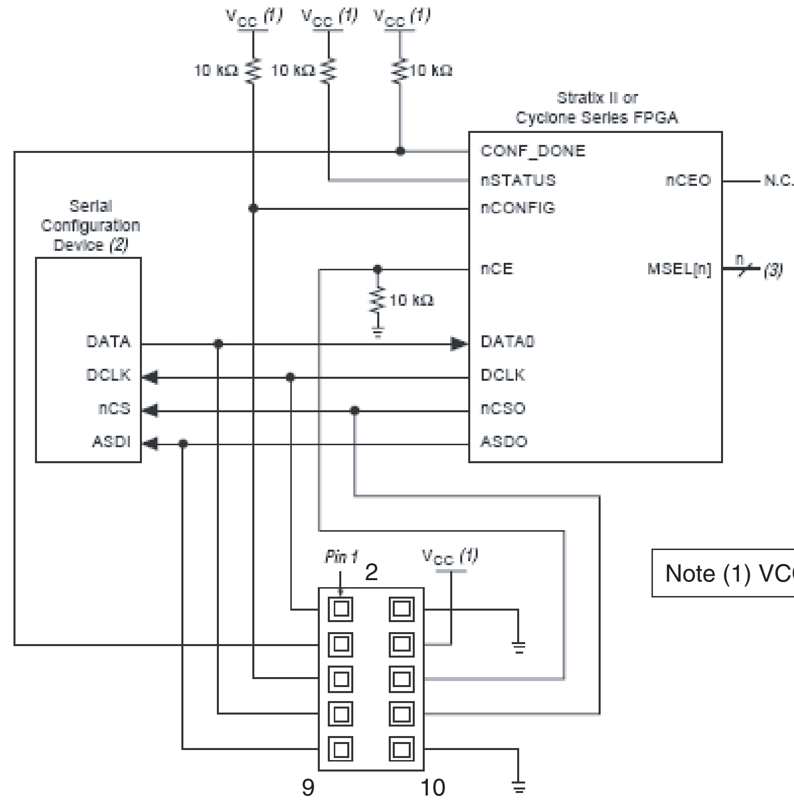
↵

4.6 Configuration and Software of the FPGA Memory

4.6.1 PROG FPGA

The configuration of the FPGA memory is done via the connector "PROG FPGA" already solder on the evaluation board.

This is the scheme below:



Note (1) VCC = 3.3V

Connector type HE10 male 2x5 points

Pin	Name	Pin	Name
1	DCLK (Serial clock)	2	GND (ground)
3	CONF-DONE (pull-up VCC)	4	VCC = 3.3V
5	nCONFIG (pull-up VCC)	6	nCE (pull-down)
7	DATA0 (data prog FPGA)	8	nCSO (Chip select)
9	ASDO	10	GND (ground)

For the configuration of the serial memory, there is 4 bit of configuration (MSL0-3).

In this application note we use the FAST AS (40 MHz) mode.
MSEL3: jumper out
MSEL2: jumper in
MSEL1: jumper in
MSEL0: jumper in

Table 4-1. Stratix II & Stratix II GX MSEL Pin Settings for AS Configuration Schemes

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)[(1)]	1	0	0	0
Remote system upgrade fast AS (40 MHz)[(1)]	1	0	0	1
AS (20 MHz)[(1)]	1	1	0	1
Remote system upgrade AS (20 MHz)[(1)]	1	1	1	0

Note: 1. Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock ; other EPCS devices support a DCLK up to 20 MHz. Refer to the Serial Configuration Devices Data Sheet for more information.

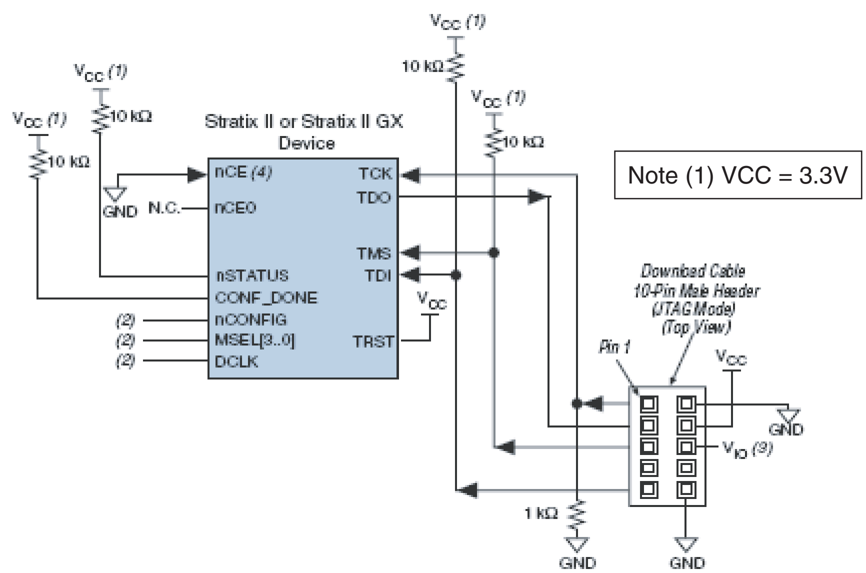
4.6.2 FPGA Configuration with JTAG

FPGA configuration with JTAG is use on debug mode.

Note: if the evaluation board is power off, the FPGA lose the configuration

The program is done via JTAG connector. This connector is not on the evaluation board.

This is the schema below:



Notes: 1. The pull-up resistor should be connected to the same supply voltage as the USB Blaster, Master Blaster (V_{10}pin), ByteBlaster II, or ByteBlasterMV cable.
2. The jumper configuration (MSEL) has no effect in this mode.

Connector type HE10 male 2x5 points

Pin	Name	Pin	Name
1	TCK (pull down)	2	GND (ground)
3	TDO	4	VCC = (3.3V)
5	TMS (pull up)	6	NC
7	NC	8	NC
9	TDI (pull up)	10	GND (ground)

We use JTAG USB for the FPGA program in JTAG mode.

4.6.3 Configuration of the FPGA on EV10DS130AZPY evaluation board

This sequence is correct for the serial memory configuration and JTAG configuration.

Sequence:

Setup the power supplies +5V

Connect the jumper MSEL (only for the serial memory)

MSEL3: jumper off (signal to 3.3V)

MSEL2, MSEL1, MSEL0: jumper on (signal to GND)

RAMP _PATTERN: no jumper

Connect the USB BLASTER ALTERA cable on the evaluation board.

PROG FPGA: for serial memory configuration

JTAG: for the JTAG configuration

Power on the Supplies

+5V

Lunch ALTERA QUARTUS II 8.0 software (or update version)

Click on " Program"

The window below is openning:

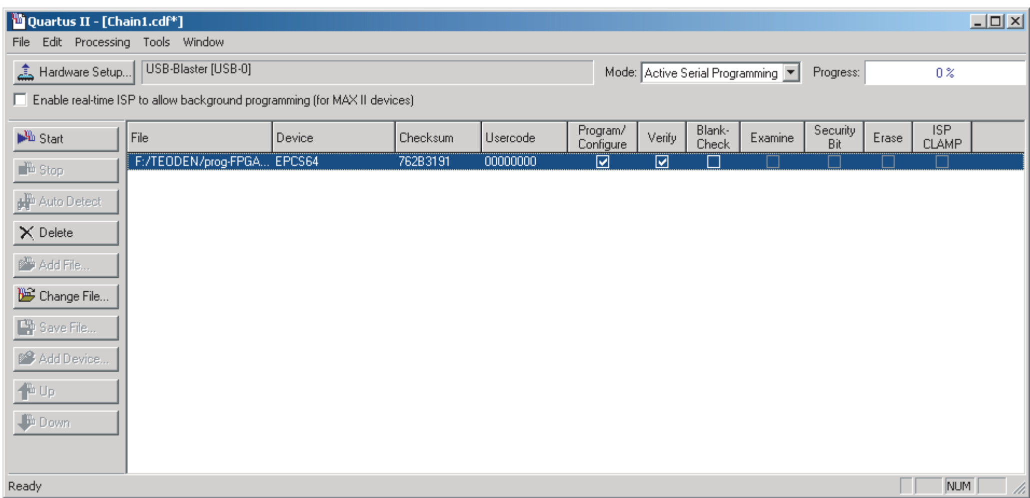
Check that the USB blaster is select, else click on Hardware Setup to do it.

Select the mode Active Serial Programming for the serial memory program.

Select the mode JTAG for program via JTAG

Choose the program file (teoden_top.pof design 3GHZ) via " Add file ". The information must be note.

click on " Start " to lunch the program.



The FPGA configuration is done when the indicator shows 100%

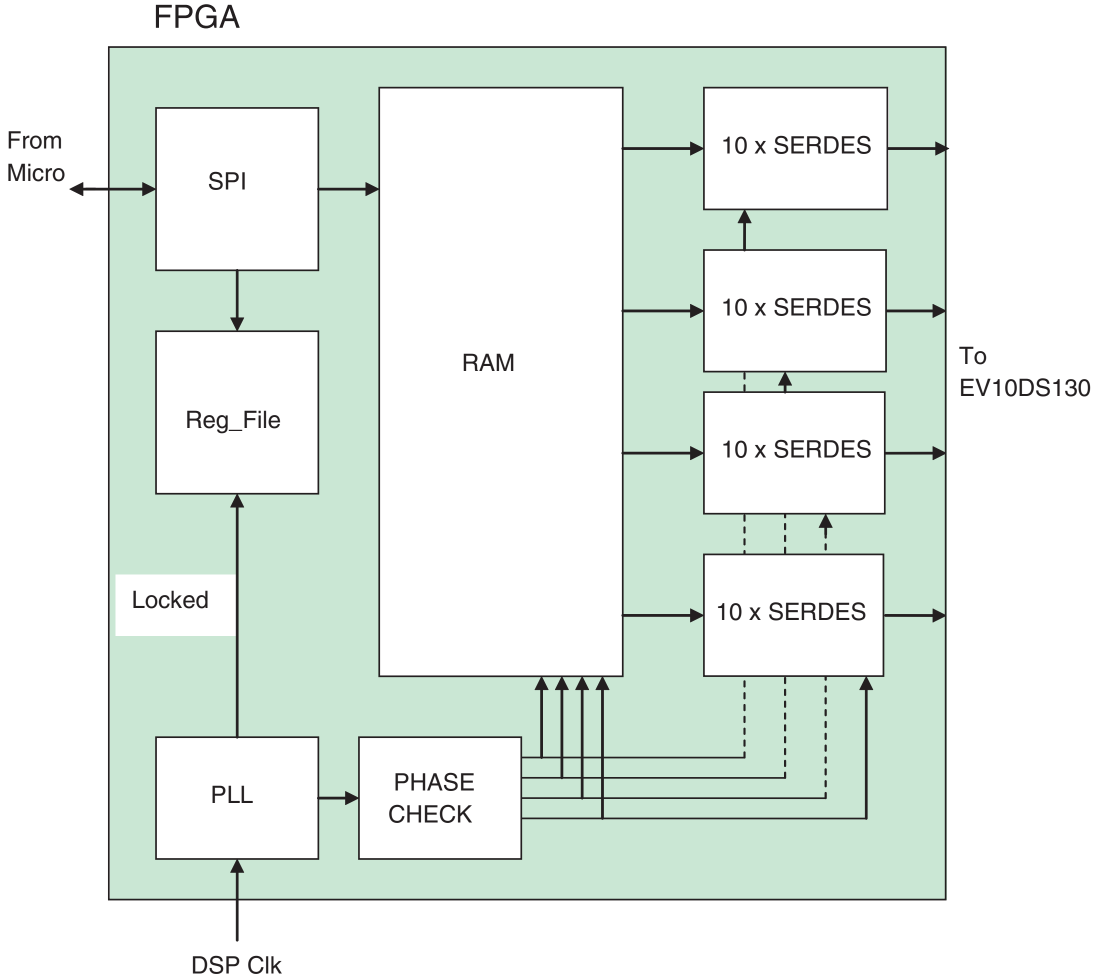
For the serial memory mode, power off: 5V supplies.

Disconnect the USB BLASTER ALTERA cable, then power up the evaluation to load the software via the external serial memory.

4.6.4 FPGA Block Diagram

The following figure represents the block Diagram of the FPGA:

Figure 4-9. Block Diagram



SPI	: SPI interface block
Reg File	: Control and Status registers and IO control
PLL	: Stratix PLL black box
RAM	: Startix MRAM and DPRAM instantiations
PHASE CHECK	: Process to ensure readout clock are in phase
SERDES	: Stratix black box, 1 per output bit, so 10 per channel. Each SERDES is 8 bits deep.

Note: FPGA block diagram is the same between CICGA and fpBGA.

e2v

Section 5

Application Information

5.1 Analogue Input

The analogue output is in differential AC coupled mode as described in Figure 5-1.

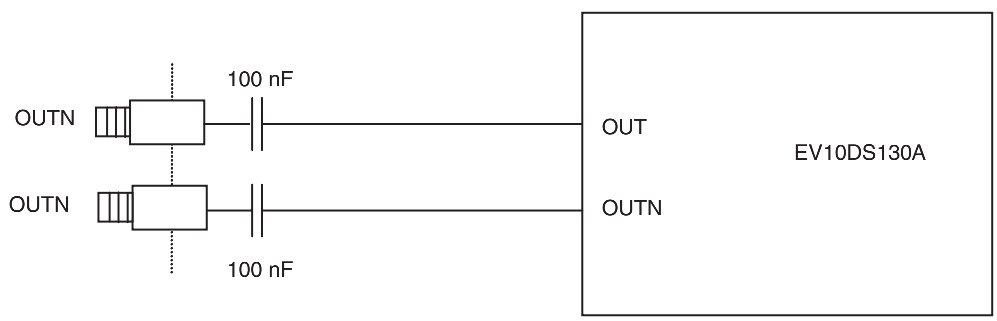
The single-ended operation for the analog output is allowed but it may degrade the DAC performance significantly. It is thus recommended to use a differential via an external balun or differential amplifier.

Ultra-broadband capacitors are used for analogue output. This capacitor is ultra-low loss, flat frequency response and an excellent match over multiple octaves of frequency spectrum.

Note: References of differential amplifiers and external baluns:

- M/A-COM H9 balun (1 Nyquist zone)
- M/A-COM TP101 1:1 transformer (1 Nyquist zone)
- ANAREN 3A0056 3dB coupler 2G-4G (2 and 3 Nyquist zone)
- KRYTAR double arrow 180° hybrid 0.5G-8G (2 and 3 Nyquist zone)

Figure 5-1. Differential Analogue Output Implementation

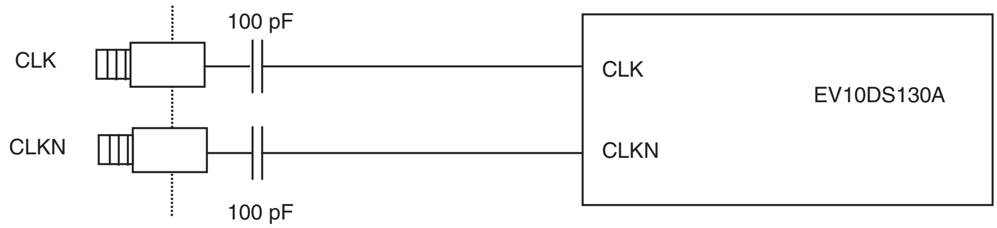


For further applications information refer to application note 1087

5.2 Clock Inputs

The clock input can be entered indifferently in single-ended or differential mode with no performance degradation. The clock is AC coupled via 100 pF capacitors as described in Figure 5-2.

Figure 5-2. Clock Input Implementation



If used in single-ended mode, CLKN should be terminated to ground via a 50Ω resistor. This is physically done by shorting the SMA on CLKIN with a 50Ω cap.

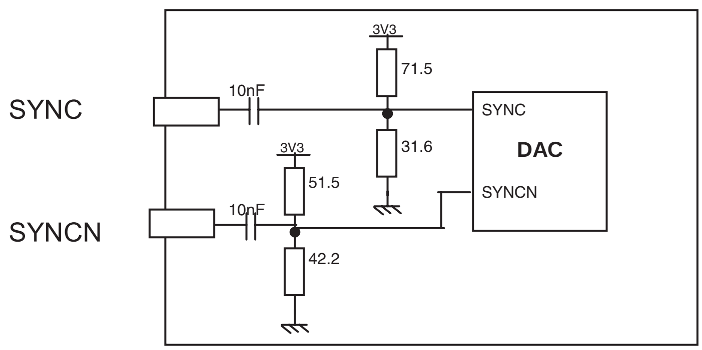
The jitter performance on the clock is crucial to obtain optimum performance from the DAC. We thus recommend using a very low phase noise clock signal if a fixed frequency is used.

5.3 SYNC Inputs

The SYNC, SYNCN is necessary to start the DAC after power up.

The reset signal is implemented as illustrated in Figure 5-3. We recommend applying a square LVDS signal.

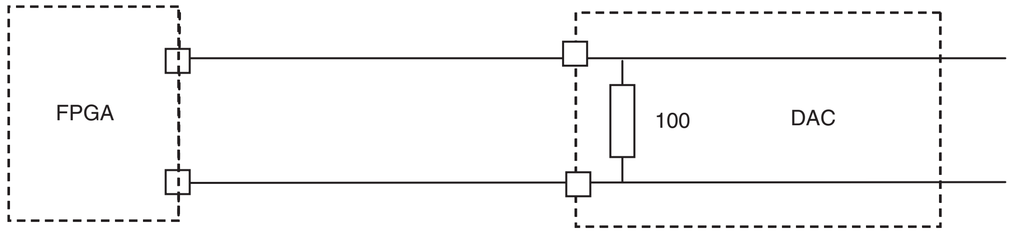
Figure 5-3. SYNC, SYNCN Inputs Implementation



5.4 Input Data

The output data are LVDS and are 100Ω on chip terminated to ground as shown in Figure 5-4.

Figure 5-4. Output Data On-Board Implementation



5.5 Diode for Junction Temperature Monitoring

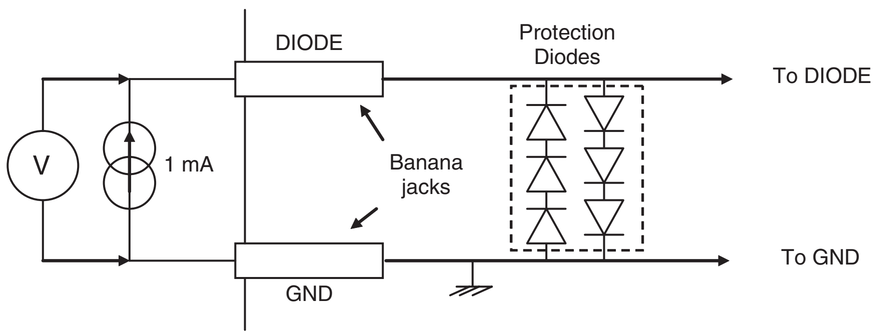
Two 2 mm banana jacks are provided for the die junction temperature monitoring of the DAC.

One banana jack is labeled DIODE and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to GND.

There is possibility to protect the DAC diode via 2 × 3 head-to-tail diodes.

Figure 5-5 describes the setup for the die junction temperature monitoring using a multimeter.

Figure 5-5. Die Temperature monitoring Test Setup



Note: Protection diodes are not connected.

1088AX–BDC–10/12

Section 6

Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EV10DS130ACZPY	fpGBA196RoHS	0°C <Tc, Tj< 90°C	Commercial « C » Grade	
EV10DS130AVZPY	fpGBA196RoHS	–40°C <Tc, Tj < 110°C	Industrial « V » Grade	
EV10DS130AZPY-EB	fpGBA196RoHS	Ambient	Prototype	Evaluation board

Section 7

Appendix

7.1 EV10DS130AZPY-EB Electrical Schematics

Figure 0-1. Power Supplies Bypassing

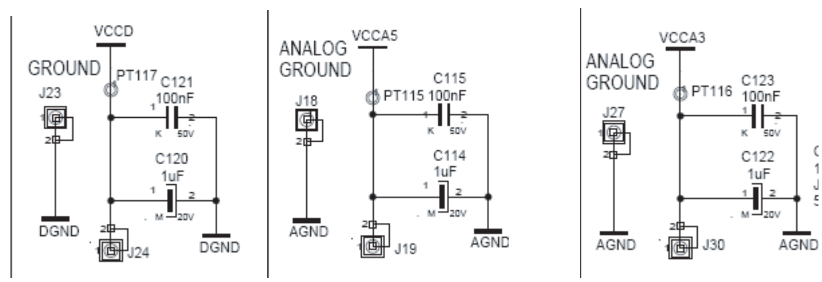


Figure 7-1. Power Supplies Decoupling (J = ±5% Tolerance)

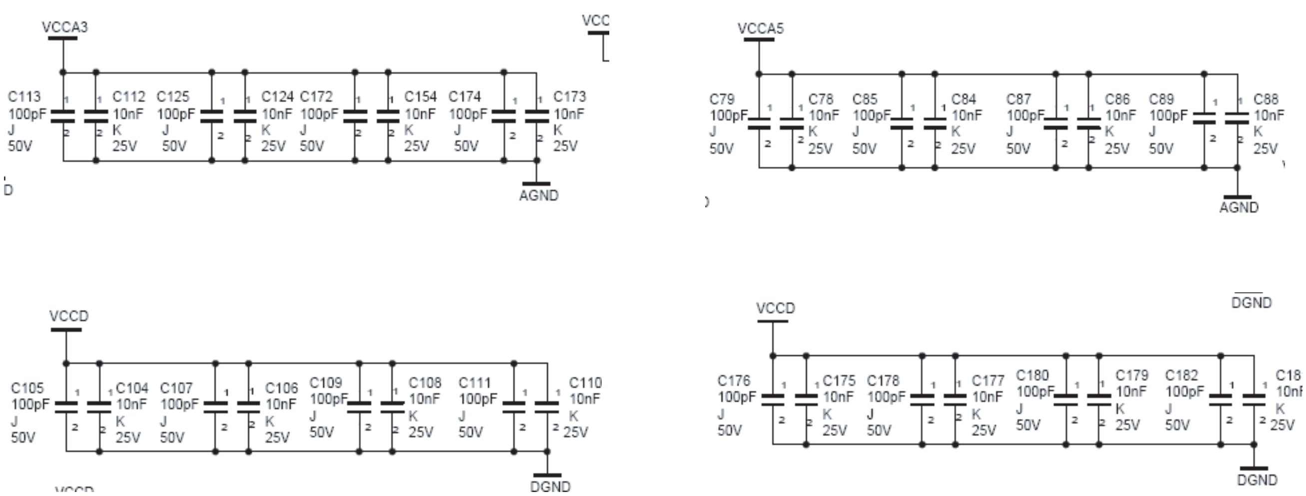


Figure 7-2. Electrical Schematics (DAC)

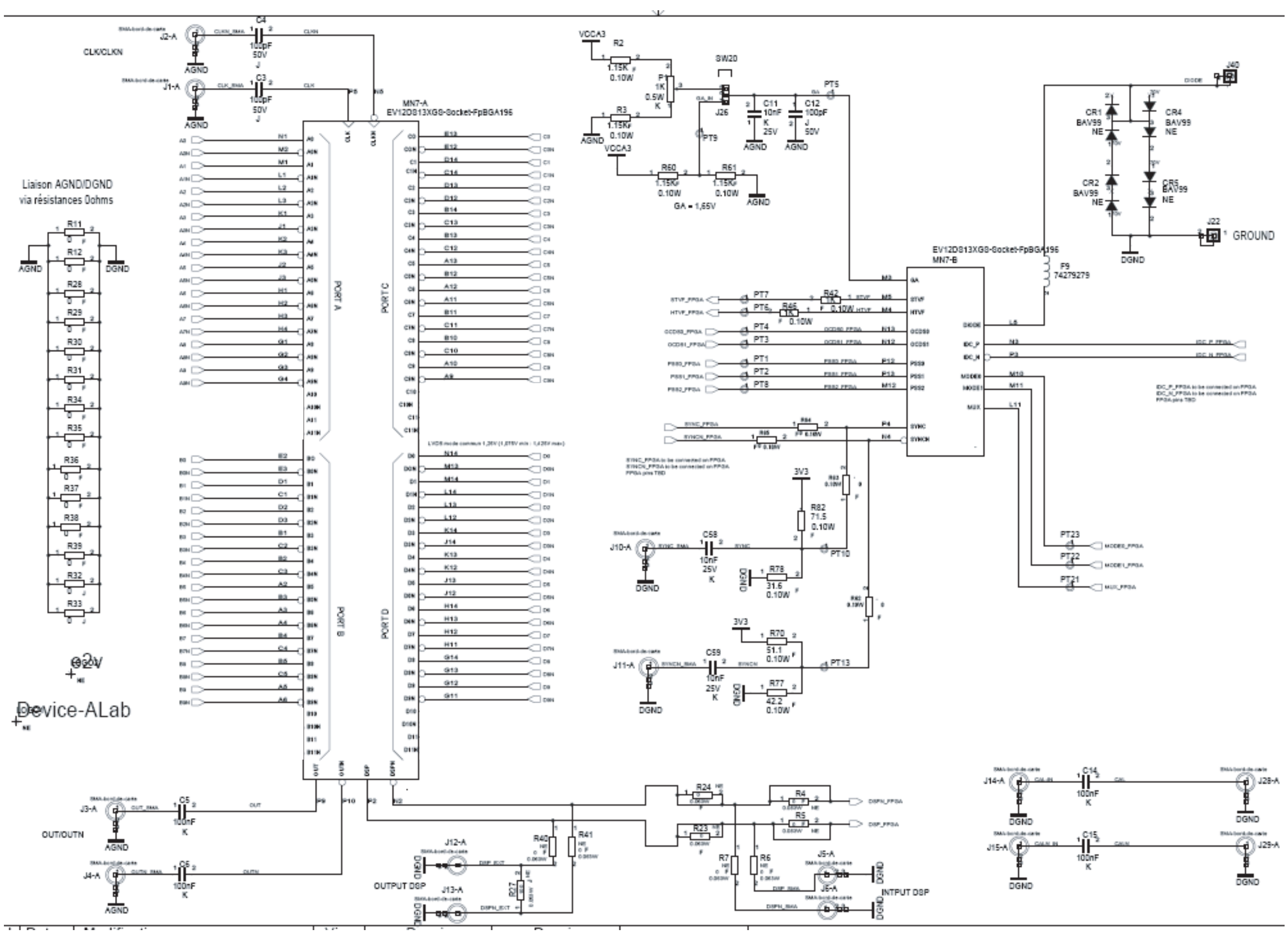


Figure 7-3. Bloc Control

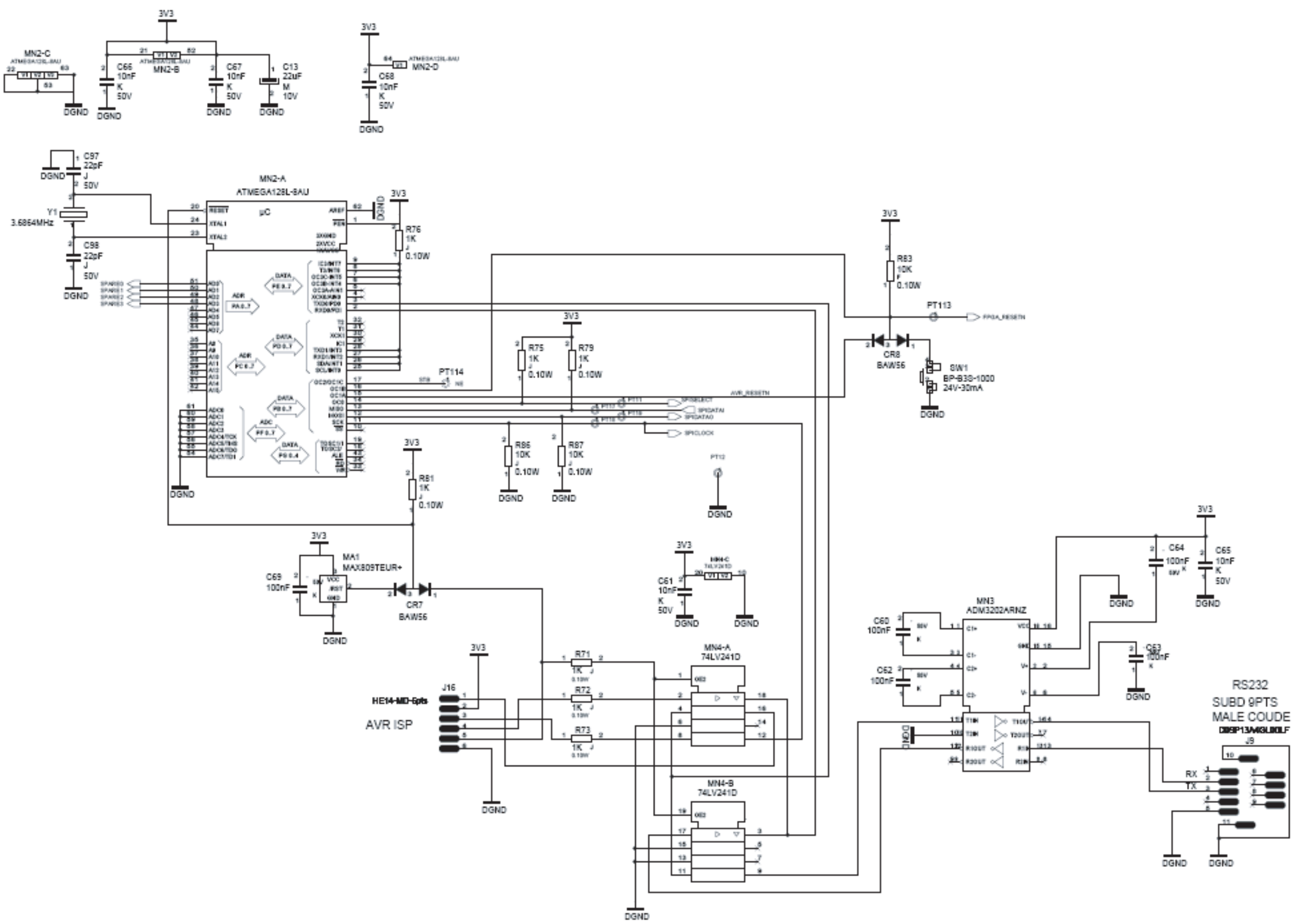


Figure 0-2. FPGA

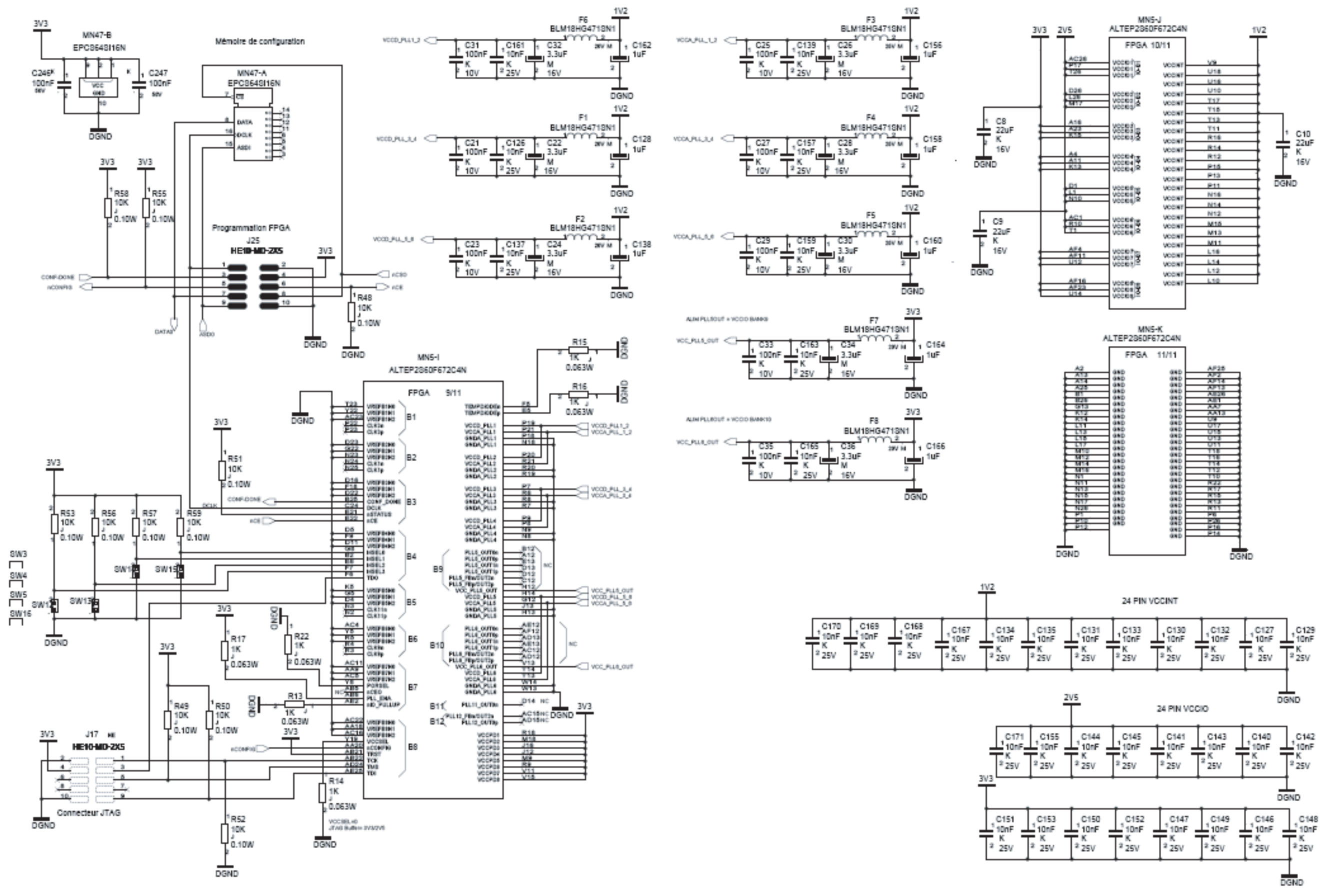
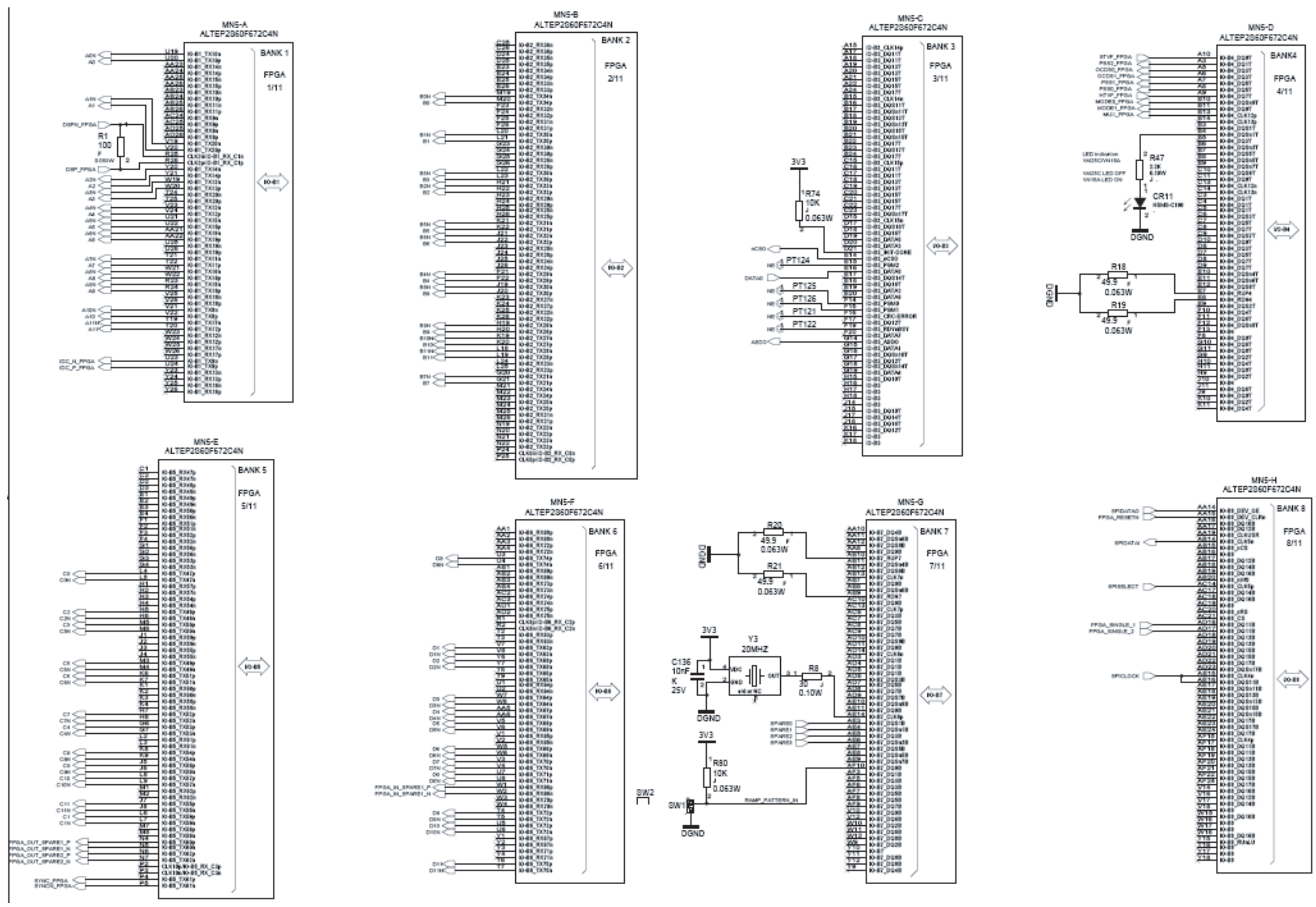


Figure 7-4.


MN5-A
ALTEP2060F672C4N
BANK 1
FPGA
1/11
MN5-B
ALTEP2060F672C4N
BANK 2
FPGA
2/11
MN5-C
ALTEP2060F672C4N
BANK 3
FPGA
3/11
MN5-D
ALTEP2060F672C4N
BANK4
FPGA
4/11
MN5-E
ALTEP2060F672C4N
BANK 5
FPGA
5/11
MN5-F
ALTEP2060F672C4N
BANK 6
FPGA
6/11
MN5-G
ALTEP2060F672C4N
BANK 7
FPGA
7/11
MN5-H
ALTEP2060F672C4N
BANK 8
FPGA
8/11
3V3
DGND
20MHZ

7.2 EV10DS130AZPY-EB Board Layers

Figure 7-5. SIG 1 Top Layer

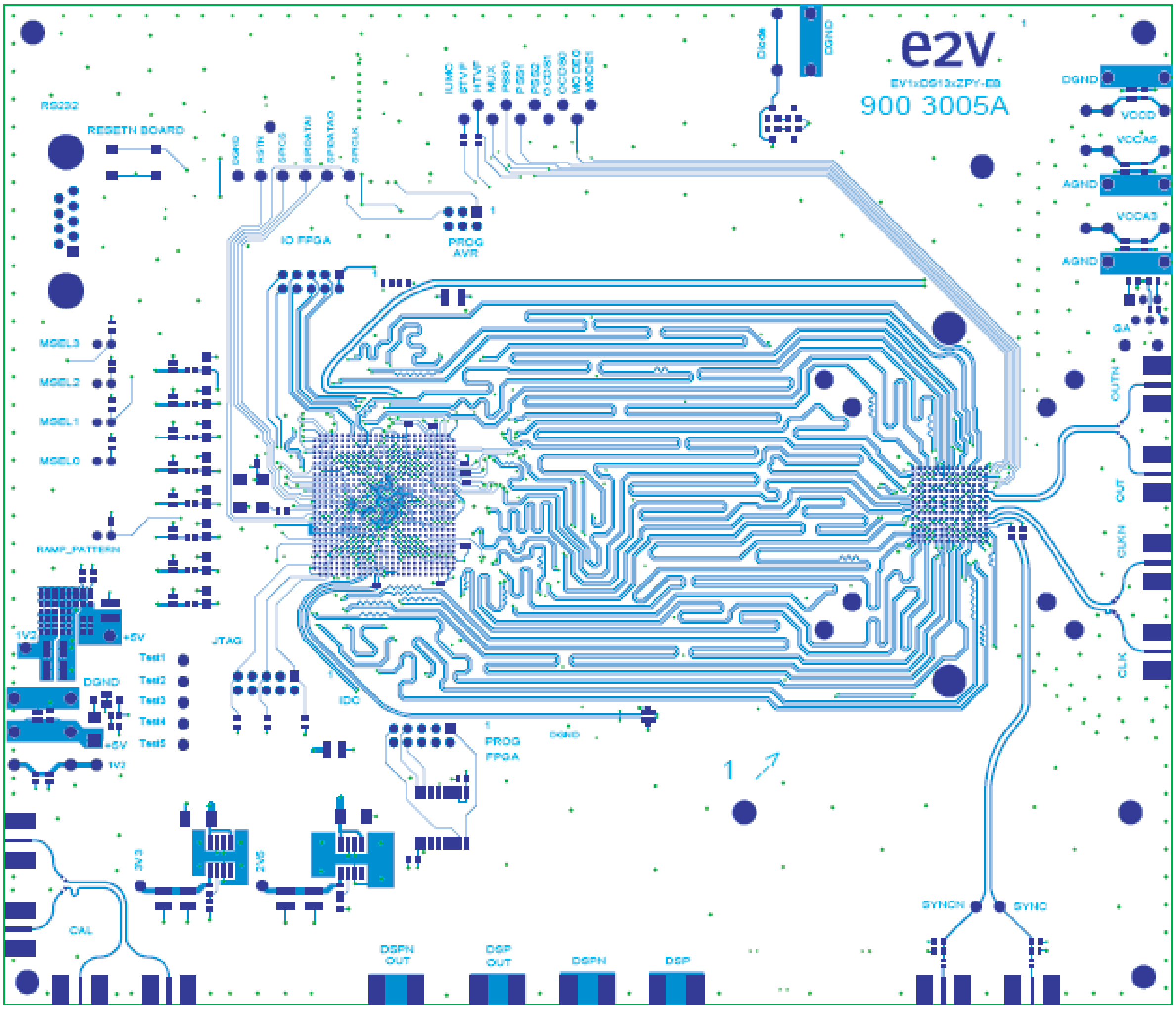


Figure 7-6. SIG 6 Bottom Layer

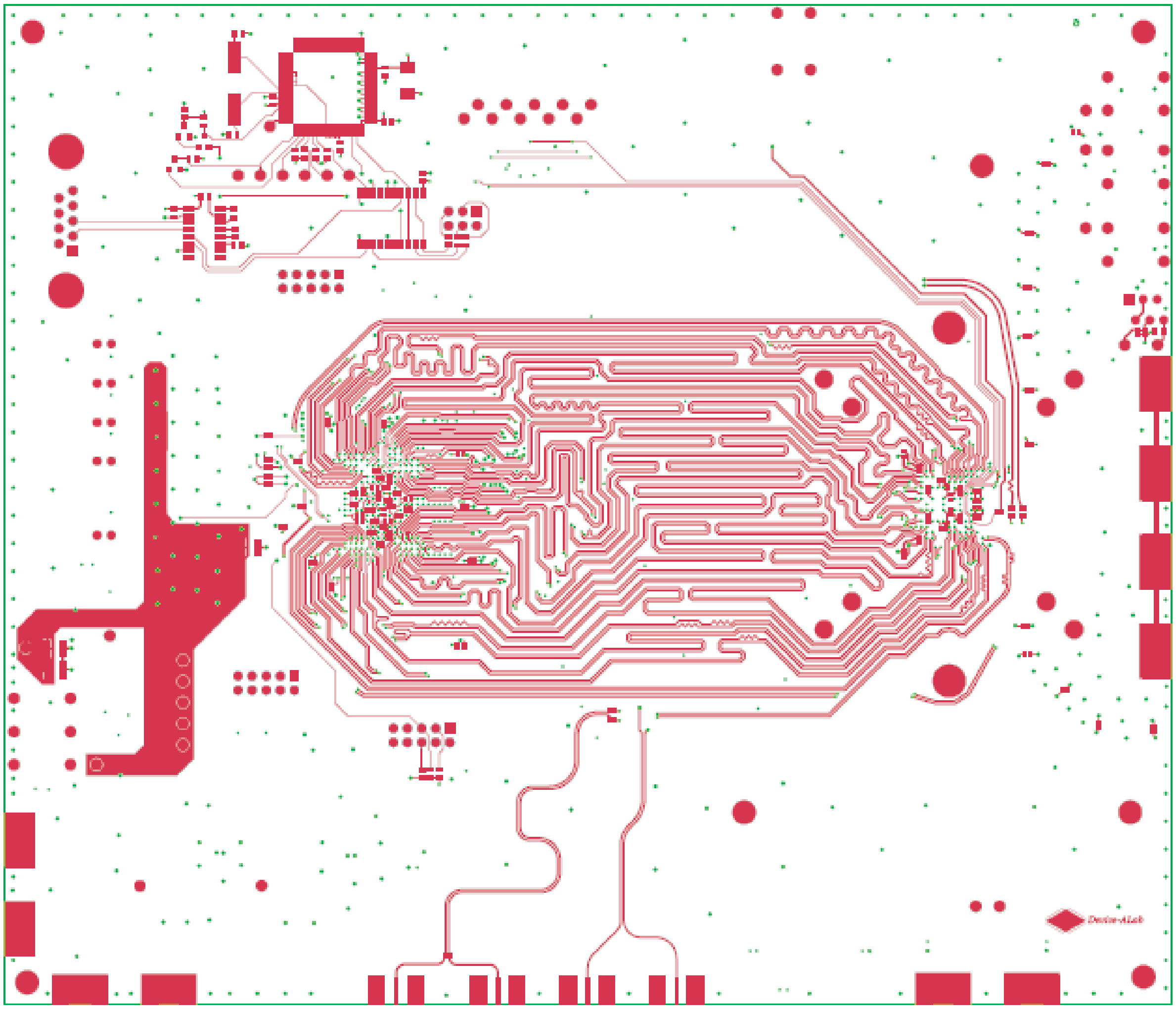


Figure 7-7. **SIG2** AGND + DGND Plane

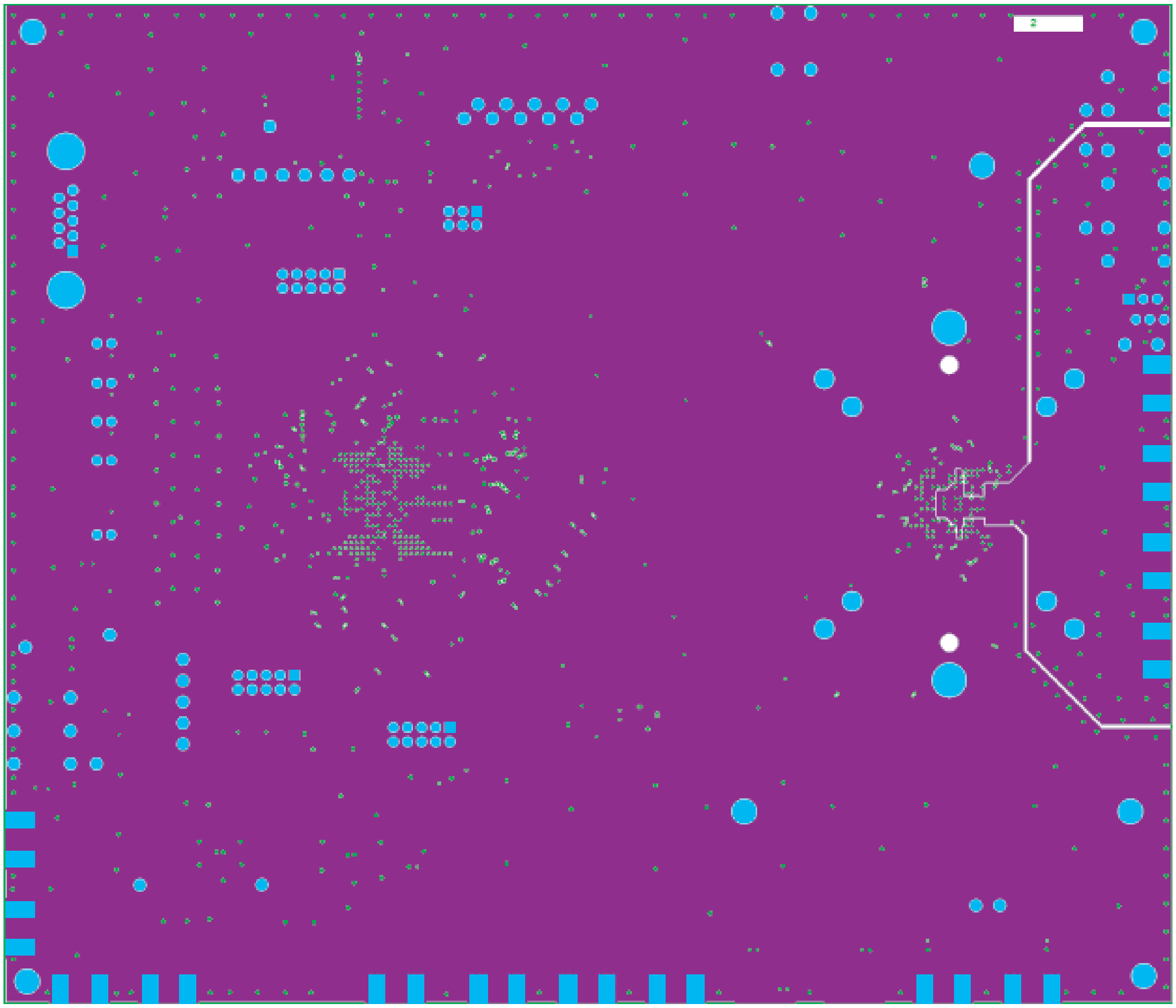


Figure 7-8. **SIG3** Signal + Power Supplies

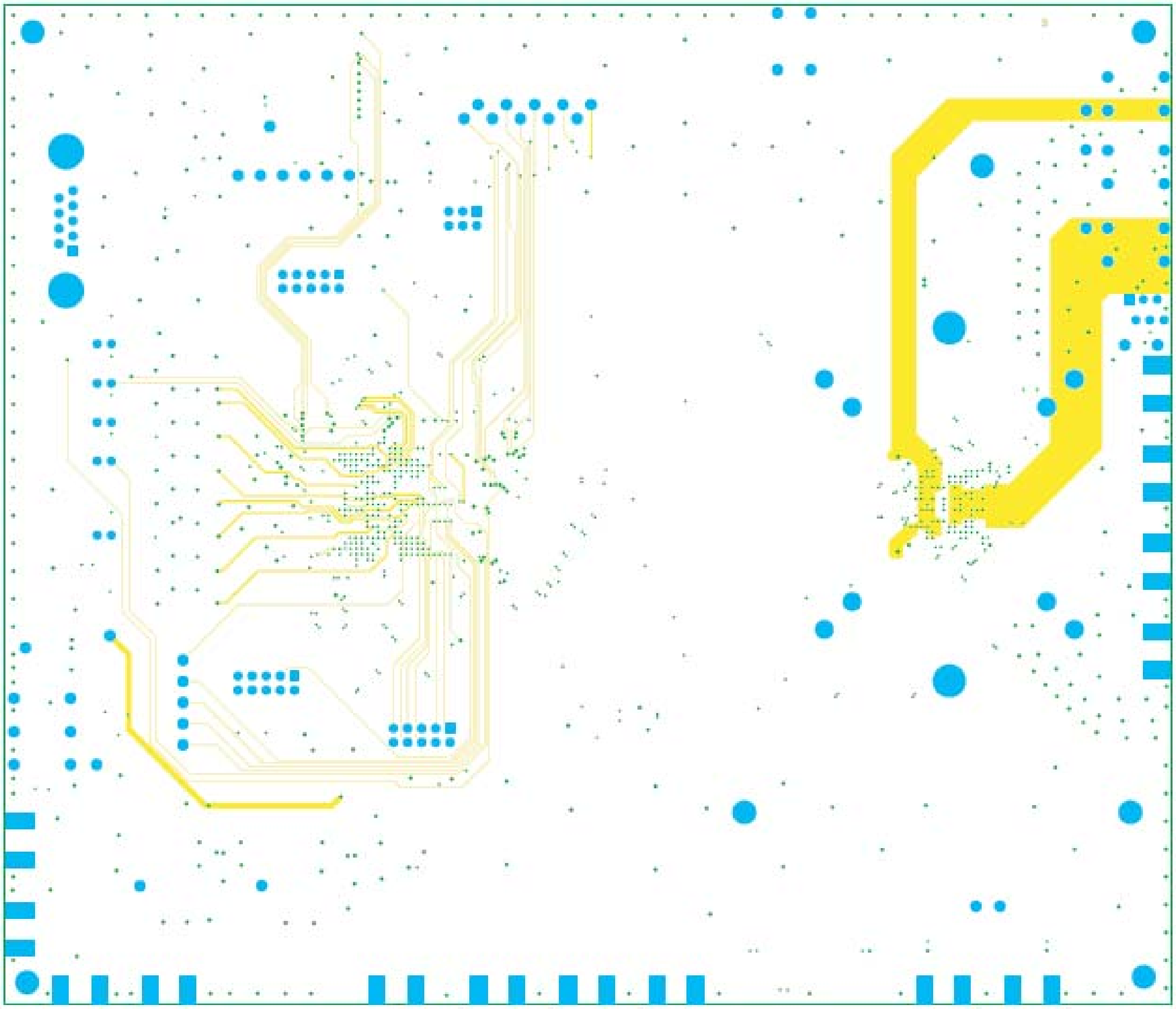


Figure 7-9. **SIG4** AGND + Power Supplies

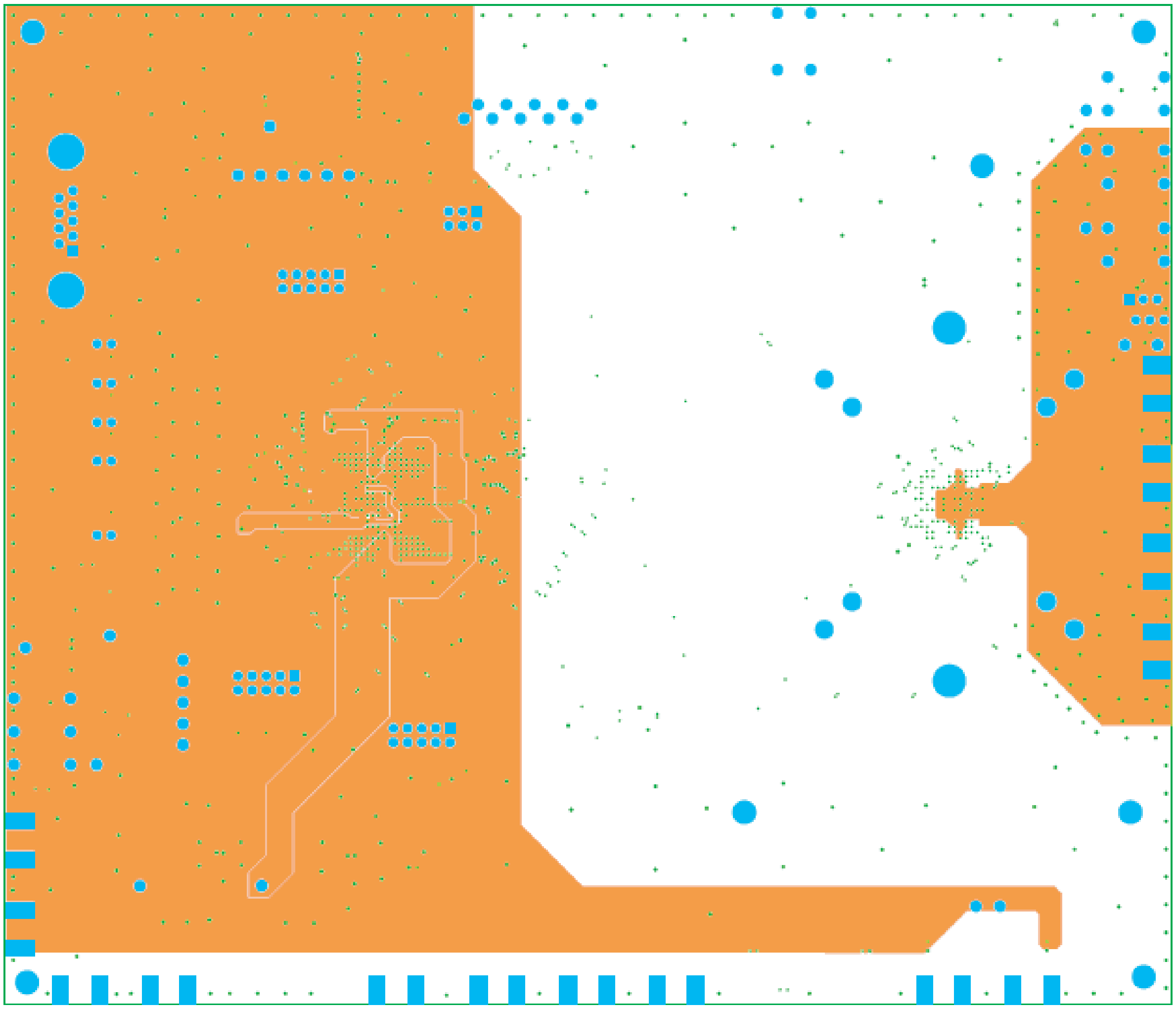


Figure 7-10. **SIG5** DGND + VccA5 + GA

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