WHITE PAPER

Making History: Advanced System in a Package Technologies Enable Direct RF Conversion

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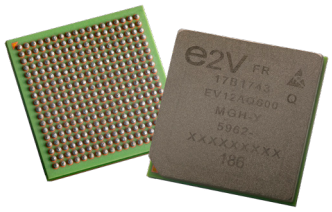
ABSTRACT

RF data conversion systems are experiencing rapid changes as ADC and DAC performance specifications and form factors, along with new sensor technologies (Rx & Tx), continue to advance. One system level design problem has been consistent throughout—balancing the implementation tradeoffs between the analog and digital circuitry for maximum software/system flexibility (from sensor to the digital processing units' input/output). This fundamental problem requires the system designer to partition (or combine) the data conversion circuit components, along with analog and digital signal routing, that would allow for maximum softwarization for multiple implementation services. Now, as the future of advanced SiP (System-in-Package) assembly technologies accelerate data conversion system design implementations from hardware to software centricity; Teledyne e2v's SiP design, development, and assembly expertise revolutionizes system level design for maximum flexibility and multi-mission capability. Using state-of-the-art technologies (flip chip, organic packages, etc.) for RF, Mixed-Signal, Digital Processing applications for use in: industrial, medical, avionic, instrumentation, telecommunication, military, and space applications are realized. Teledyne e2v's 40+ years of experience in advanced SiP design and assembly technologies gives system designers the highest performance and value for advanced data conversion system platforms.

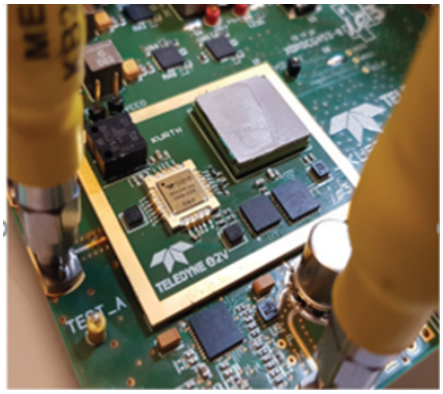
ADVANCED DATA CONVERSION COMPONENTS FOR SIP DESIGNS

High frequency data conversion systems require high-performance (and reliable) semiconductor devices which address the critical functions of the complete signal chain. Selecting the appropriate semiconductors that meet the overall system performance requirements is essential for SiP implementation. Teledyne e2v provides high-speed data converters, microprocessors, memory, and various analog and logic functions for SiP implementations.



Of course, the centerpiece of data conversion receiver (Rx) systems is the ADC. Teledyne e2v has been innovating data converter technologies for over 20 years and offers multi-channel, low noise and distortion ADCs that operate at microwave frequencies (such as the EV12AQ600 shown above). These types of data converters allow system designers the ability to eliminate analog stages (by direct RF conversion) that have been needed in traditional architectures for frequency down conversion. Along with reducing analog stages with Te2v's high-end ADCs, and utilizing advanced SiP design technology with license free, standard and custom solutions; enables designers the ability to realize many standardized products and customized solutions that can be realized in order to meet specific performance qualifications and/or environmental requirements.

At the center of future high-speed SiP Direct RF data conversion receiver (Rx) solutions is the EV12AQ600. Combined with the RTH120 Track and Hold Amplifier (THA), the PS620 experimental SiP RF front-end receiver board (shown below) yields state-of-the-art performance (see Key parameters of active device page 2),). The EV12AQ600 is a quad core ADC that features a Cross Point Switch (CPS) front-end which allows the four ADC cores to operate simultaneously, independently, or paired. Operating in quad-channel at 1.6 GSps, dual-channel at 3.2 GSps, or single-channel at 6.4 GSps. Typical SFDR in quad channel mode (without H2 and H3 harmonics) is better than 70 dBFS at -1 dBFS up to 5980MHz.



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This device is offered in various grade classes from commercial, to industrial, to military grades; up to radiation-tolerant space-level quality. The EV12AQ600 is fit for various applications such as: High-Speed Data Acquisition, High-Speed Test Instrumentation, Automatic Test Equipment, Earth Observation SAR satellite payload, Telecommunication MIMO satellite payload, Ultra-Wideband Satellite Digital Receiver, C-band Direct RF Down Conversion, Microwave Software Defined Radio, Point-to-Point Microwave Receivers, Machine Condition Monitoring System, Time of Flight Mass-Spectrometry, LiDAR (Light Detection and Ranging), and High Energy Physics.

Key parameters of active devices

EV12AQ600 ADC:

- Quad 12-bit 1.6 GSps ADC cores support 1, 2 or 4 channel time interleaving
- Sample up to 6.4 GSps in fully intervealed mode
- 6.5 GHz input bandwidth (-3dB)
- Integrated broadband cross point switch
- Sync chain for multi-channel synchronization

RTH120 THA:

- 24GHz input bandwidth
- Dual THA enables output hold time for more than half a sample clock cycle
- Fully differential design

In regards to implementing high-speed state-of-the-art SiP data conversion transmitter (Tx) solutions, the key enabling technology is the EV12DD700 (shown right). This dual channel 12 Bit DAC can operate up to 12 GSps and features: Direct RF output signal generation up to 21 GHz, full scale step response times as low as 15 ps, with the lowest noise and performance on the market at microwave frequencies. The EV12DD700 dual-channel DACs are also capable of operating into Ka-band frequencies and support beamforming applications. The DAC has a 25GHz, 3dB output bandwidth, and is capable beyond 25GHz with just a little over 3dB attenuation (see Figure 1 below). Built into each DAC is an array of sophisticated signal processing functionality. This encompasses a programmable anti-sinc filter for direct digital synthesis (DDS) capabilities, as well as a programmable complex mixer. Also included, is a digital up-converter with four interpolation stages. Digital Processing Functions include: Interpolation (4X, 8X, and 16X ratios), Digital Up Conversion (DUC) with a Numerically Controlled Oscillator (32-bit NCO), Direct Digital Synthesis (DDS), Digital beamforming and beam-hopping. Main features for the DAC include: Programmable output mode (NRZ, RF, 2RF), Gain adjust, Programmable SINC compensation function, and Multi-device synchronization.

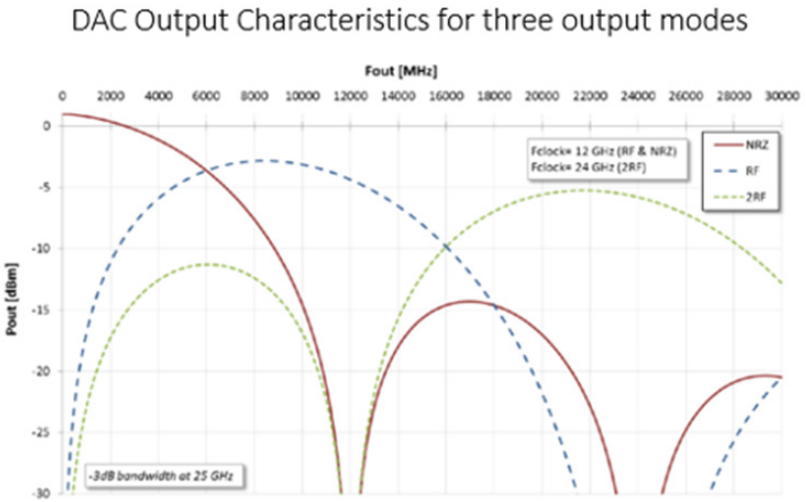
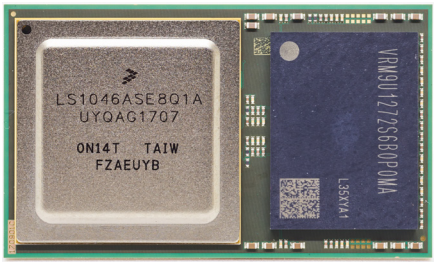


Figure 1

Of course, all high-speed data conversion systems also require advanced digital processing capabilities. For example, Teledyne e2v, has qualified and released an up-screened microprocessor from NXP's new Layerscape® Series, the LS1046A, that can operate at -55°C to 125°C (the LS1046-Space will also be released soon). The LS1046A is part of NXP's 64-bit Arm® Layerscape portfolio that utilizes a quad-core Arm® Cortex® A72 design.



This design provides unparalleled performance in the smallest form factor possible; while enabling access to the vast ecosystem of software services, applications, and tools compatible with Arm® technology. The LS1046A is a 1.8GHz processor, integrating packet processing acceleration, with high-speed peripherals, and is recognized for its high-performance architecture and market-leading compute density. Offering more than 45,000 CoreMarks® of compute performance (also 30K DMIPS @ 1.8 GHz), paired with dual 10Gb Ethernet, 3 PCIe Gen3, and 1 SATA Gen3 is suitable for a range of high reliability mil-aero (and space) applications. The LS1046A is also the chosen device to be embedded into Teledyne e2v's latest Qormino® computing module, which also includes a 4GB DDR4 memory (see photo left). In addition, as part of Teledyne e2v's Semiconductor Lifecycle Management program, SLiM™, the lifetime of this device can be supported for 15+ years, avoiding common and costly obsolescence issues.

PEAK SYSTEM PERFORMANCE FOR DATA CONVERSION SIP IMPLEMENTATIONS: FOR ALL MARKET SEGMENTS

Data conversion systems are experiencing rapid changes from industrial, to medical, to avionics, to instrumentation, telecommunications military, and space applications. The overarching system level design problem, for all market segments, is balancing the implementation tradeoffs between the analog and digital circuitry for maximum software/system flexibility (from sensor to computer input or computer output to sensor). This fundamental problem requires the system designer to partition (or combine) the data conversion circuit components, along with analog and digital signal routing, that would allow for maximum softwarization for multiple implementation services.

System design engineers understand their markets, applications, and their circuit performance specification requirements; but their design parameters such as risk, technology choices, form factors, development schedules (including schedule synchronization), reliabilities, and costs associated with high performance data conversion systems, is highly variable. These design parameters, coupled with continually changing system performance specification requirements, ultimately result in narrower design implementation "intersection" options (see Figure 2). Of course, making mistakes within any design parameter is extremely costly. Therefore, any flexibilities that can be built into the design development, that actually adds an overall value to the project, and doesn't devalue, is a worthy investment.

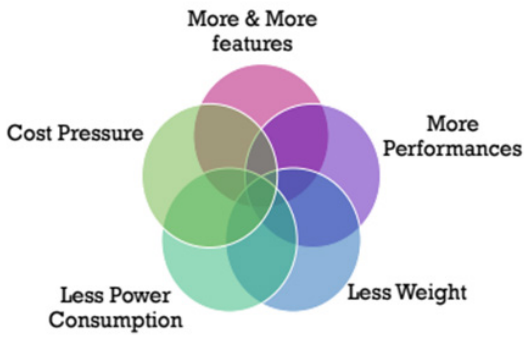


Figure 2 - Increasing design parameters, AND system level performance requirements, yields narrower implementations of "intersection" options

One design parameter that can increase flexibility for both the development phase, and ultimately achieving necessary market performance requirements, particularly for data conversion systems, is implementing the function utilizing SiP (System-in-Package) technology. In the past, continual advances in semiconductor process technologies have enabled system level designers to implement complete circuit functions within the SoC (System-on-Chip) environment. Particularly, SoC applications that require heavy digital computing, have been realized using semiconductor technology as gate lengths approach 10nm and smaller. Unfortunately, as semiconductor feature sizes decrease, the cost of chip development increases exponentially (see Figure 3).

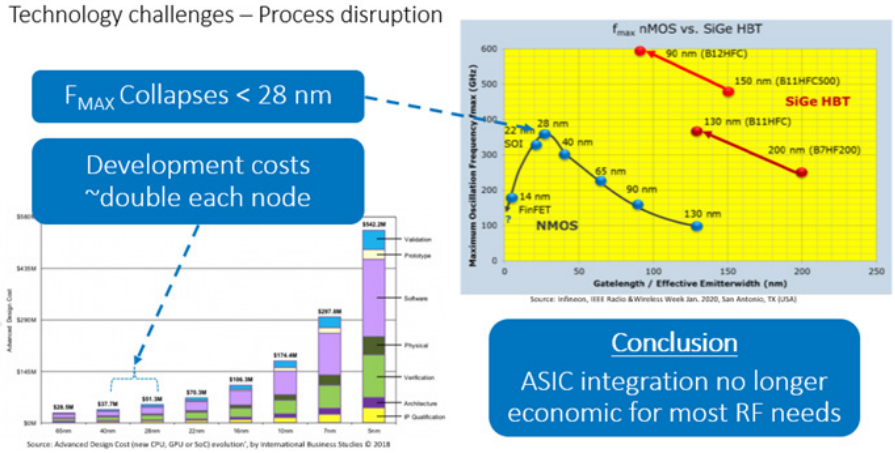


Figure 3

Figure 3 also shows the correlation between minimum geometry gate lengths versus maximum device oscillation frequencies. As shown, Fmax collapses at gate lengths <28 nm. Correspondingly, development costs increase exponentially as gate lengths decrease (i.e. G=28nm (average development cost $51.3M), G=16nm (average development cost $106.3M), G=7nm (cost $297M), G=5nm (cost greater than $500M).

Therefore, the cost for SoC developments, as more functions are included on-chip, requiring smaller gate lengths, becomes prohibitive. For example, SoCs have been the driving technology for the cell phone industry, but increasing requirements for analog technology (such a MEMS sensors) create a migration from SoC to SiP implementations. Figure 4 represents the 3 co-existing design parameters that are currently driving the migration from SoC to SiP implementations: 1) Technologies: Choosing the right process technology for optimal system performance (i.e. Si, GaAs, GaN, SiGe, etc.), 2) Miniaturization, 3) Cost.

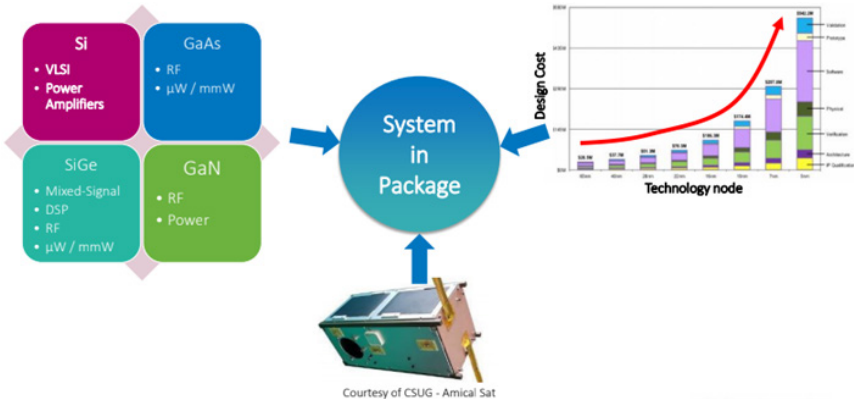


Figure 4

Another factor that is driving data conversion system developments from SoC towards SiP implementations is the requirement to partition (or combine) the data conversion circuit components, along with analog and digital signal routing, that would allow for maximum softwarization for multiple implementation services. Simply put, data conversion systems can be designed as a "centralized" or "distributed" systems (see Figure 5). Centralized data conversion systems require significant analog signal routing and is therefore subject to additional crosstalk and distortion. In contrast, distributed data conversion systems can place the ADC at the Rx sensor, and the DAC at the Tx sensor. The digital signals can be routed on board, on light, compact high data rate fiber connections.

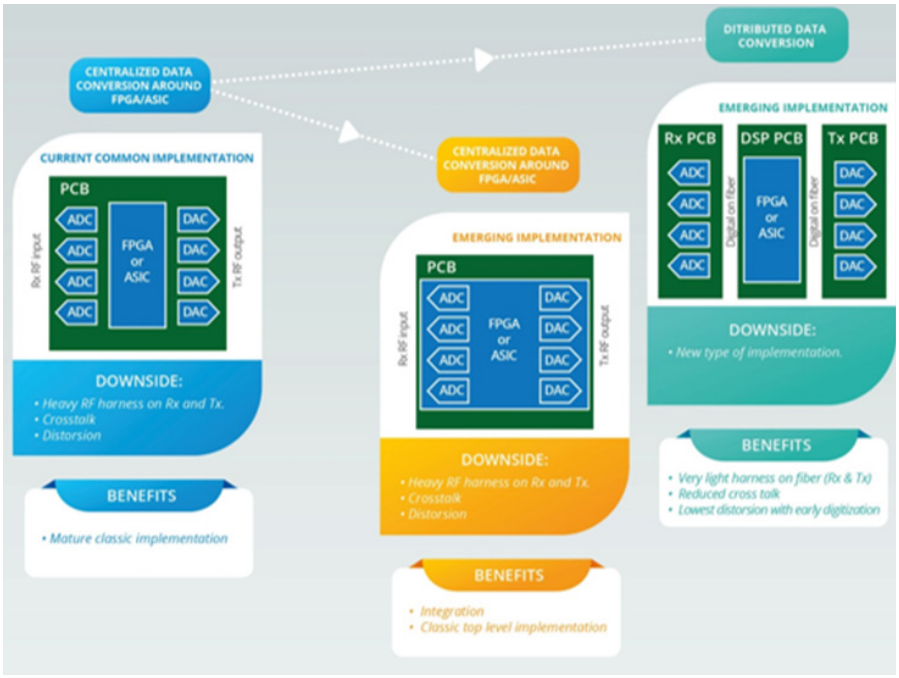


Figure 5

As a result, Teledyne e2v's advanced SiP design, development, and assembly expertise has revolutionized data conversion system developments for maximum design parameter flexibility (i.e. combining and partitioning) for multi-mission capability. By combining (or partitioning) RF, Mixed-Signal, and Digital Processing semiconductors using state-of-the-art technologies (wire-bond, flip-chip, etc.); advanced SiP design and assembly technologies give system designers the highest performance at the lowest cost for high frequency data conversion system platforms.

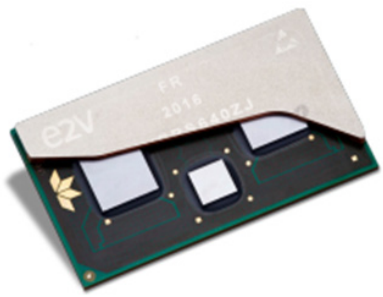


Figure 6a

For example, Figure 6 shows the PS640 which is a SiP implemented RF data conversion system that is currently being developed for future use as a L through Ka band frequency receiver (1GHz-40GHz).

The PS640 uses a new THA designed by Teledyne e2v in the STMicro BiCMOS055 process in conjunction with two interleaved EV12AAQ600 ADCs implemented as a "centralized" high-speed SiP data conversion receiver (Rx). Measured performance specifications are also shown in Figure 6. Figure 7 (below) depicts future concept of the same data conversion system implemented as a "distributed" data conversion receiver utilizing an optical engine (contained within the SiPs) that drives to a digital processor (FPGA) enabling maximum softwarization (software centricity).

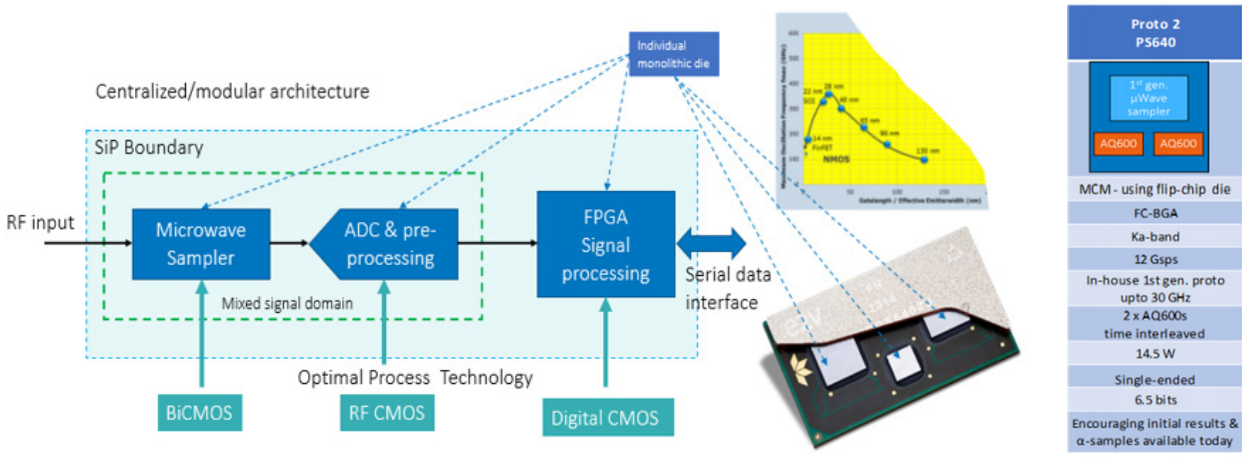


Figure 6b

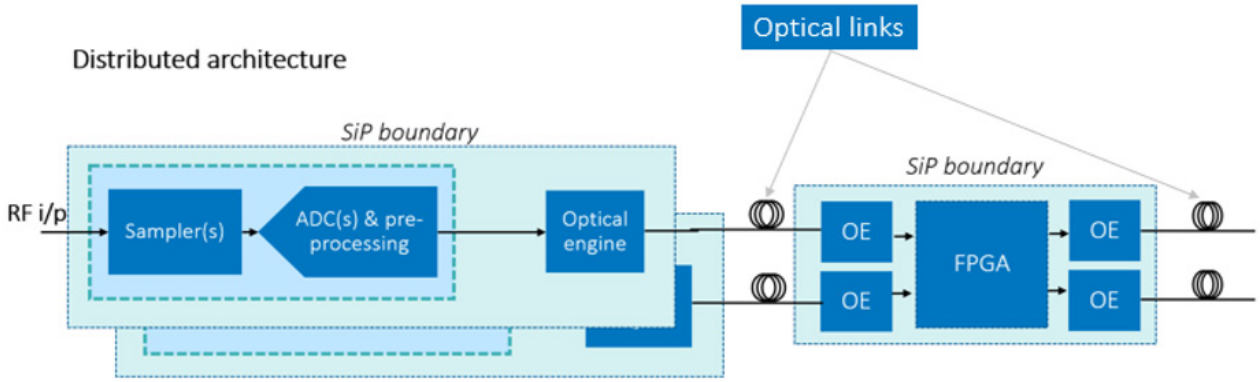


Figure 7

TE2V'S ADVANCED SIP ASSEMBLY TECHNOLOGIES

A SiP is a single device that connects multiple devices (passive and active) encased in one package. The SiP performs a range of functions at the electronic systems level. Semiconductor devices (including passive components) embedded within the SiP can be tiled horizontally and/or stacked vertically on a substrate and then packaged. Semiconductors can be connected to the substrate material either by wire bonds or solder bumps (that can also be used to stack dice together in a vertical configuration).

As previously mentioned, data conversion SiPs may contain multiple dies such a Preamps, Mixers, ADCs, DACs, as well as specialized processors and memory integrated circuits along with passive components such as resistors and capacitors. These are all mounted on the same substrate with varying mounting techniques. Utilizing SiP assembly technologies creates advances in all market segments, particularly in applications that involve: ultra-high RF (terrestrial and non-terrestrial), Internet of Things (IOT) requiring MEMs circuitry, mobile and wearable devices, etc. With a range of SiP technological products and package solutions, Te2v supplies design and assembly services to market segments such as industrial, medical, aerospace, military, scientific and space applications. Also, many of Teledyne e2v's products are developed through strategic partnerships with companies such as NXP, Everspin, Micron, and others.

Te2v offers a broad range of supply chain management services for SiP design developments including: die design, package design, high-reliability assembly, high performance at-speed testing and qualification services, including the Semiconductor Lifecycle Management under the SLiM™ brand (see Figure 8). With over 40+ years of space design experience with ADCs, DACs, Microprocessors, Memories, and In-house test and qualification services; Te2v is able to provide advanced SiP products and services to all market segments with any qualification level requirements. Te2v's advanced SiP assembly expertise includes: wire-bonding, flip-chip, organic and ceramic packaging (hermetic and non-hermetic), as well as heterogeneous assembly.

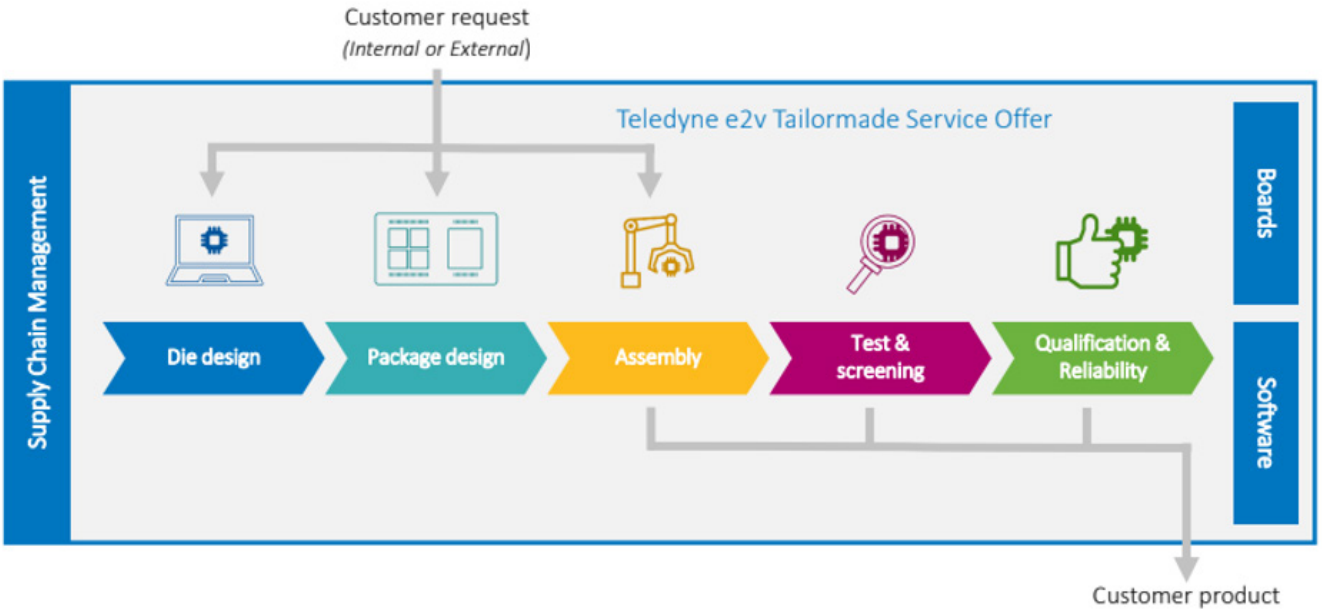


Figure 8

Of course, prior to assembly, advanced high-speed SiP developments require package simulations as well as measured package characterizations; for both thermal and reliability considerations. For instance, Figure 9

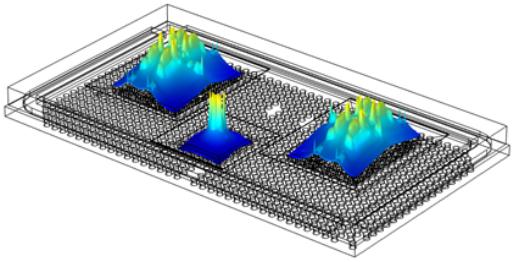


Figure 9 - Thermal Simulation of the PS640 SiP

shows a thermal simulation for the aforementioned PS640. Placing multiple die within close proximity to each other is challenging in terms of thermal design. Thermal simulations with maximum details are required in order to closely predict junction temperatures on the most critical areas of the components. Te2v uses boundary conditions, discussed with system designers and with customers as well, in order to simulate performance that will ultimately match with measured results (that would be required for the necessary components embedded within the SiP implementation). In addition, Te2v utilizes high-frequency 3D field solver (Ansys HFSS) for the simulation and design of RF SiP developments. HFSS is a commercial finite element method solver for electromagnetic structures and is used for the package design of complex RF electronic circuit/semiconductor elements, filters, transmission lines, contained within the SiP package (see Figure 10 at right). In this example, an RF analog front-end is co-designed at Te2v in collaboration between the package team and the semiconductor design team which accounts for Te2v's natural SiP process development flow.

Designing for SiP reliability is a significant engineering challenge due to the diverse silicon technologies that are embedded in a single organic substrate, with RoHS solder joints in C4 (controlled collapse chip connection - flip chip bumps) and C5 (solder balls) electro-mechanical interfaces. Te2v continually develops advanced techniques in order to quickly and precisely predict warpage and board level reliability with thermo-mechanical analysis, taking into account non-linear behavior such as solder creep and viscoplasticity (see Figure 11).

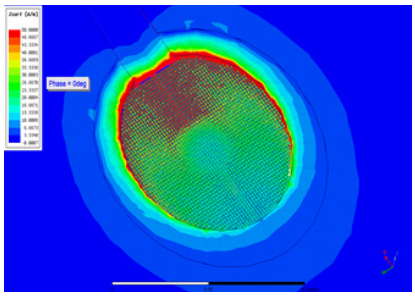


Figure 10 - Extract of a 3D field solver simulation (Ansys HFSS) of the 40GHz analog input for the PS640 showing the transition between the package and the silicon die of the THA, where signal propagation across the silicon metal filling is analyzed

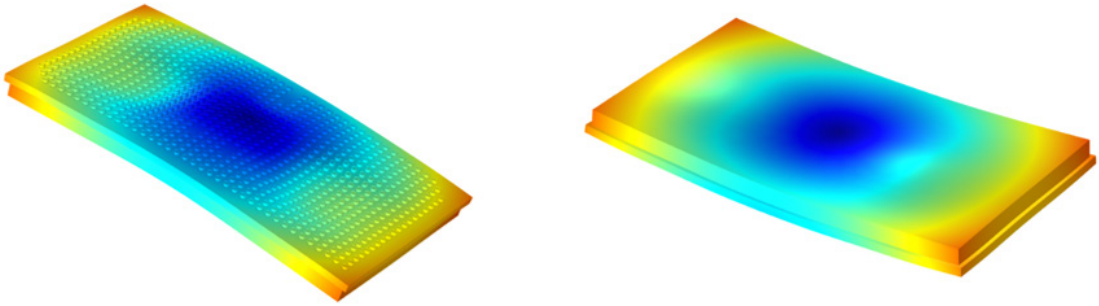


Figure 11 - 50x magnification of the PS640 packaging warpage after assembly at room temperature.

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Specific design and assembly services also include: custom products, low and medium volume, high-reliability/high-end, QML-V and QML-Y certifications, as well as space qualification (see also technology summaries in Figure 12 below):

Wafer back-end

- Full automatic : sawing and UV-exposure
- Advanced cleaning solution
- Visual inspection

Surface Mounted Devices

- Automatic printing machine, 3D screen technology
- Full automatic Chip Shooter for SMD attach
- Single package and panel process
- Multi Zone oven with controlled atmosphere

Assembly

- Very long dies
- Glass lid sealing
- Optical shield positionning
- Optical filters assembly
- Automated line for

Screening and qualification

- Burn-in, Temperature cycling and thermal chocks
- Mobile particles detection & visual inspection
- Seal test
- Lot Validation tests
- Space-grade or military qualification

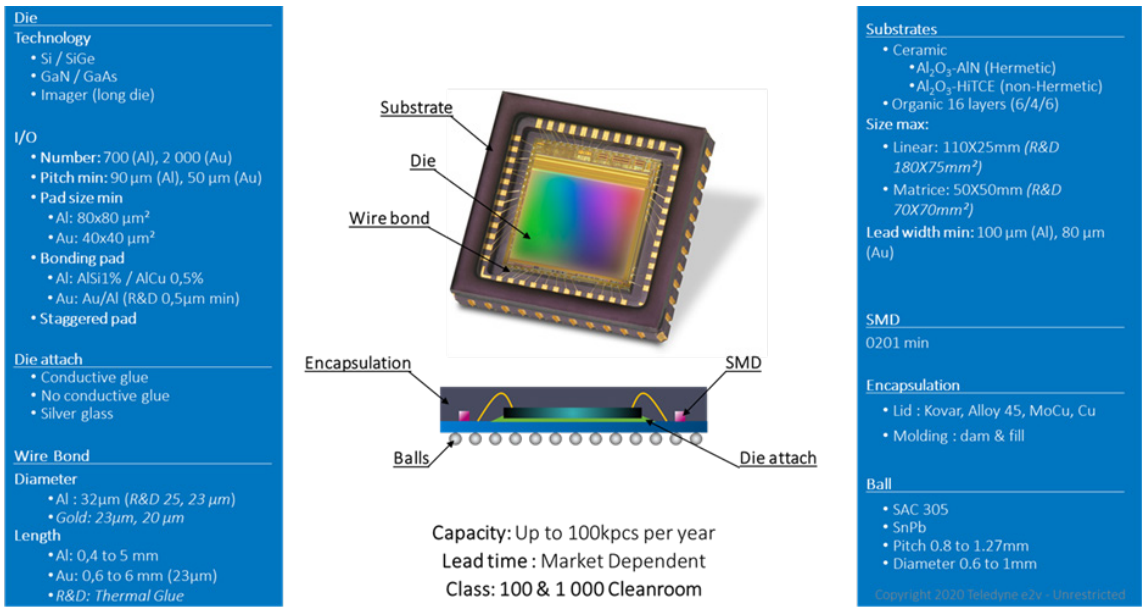
Test & Measure

- Wafer probe 6" and 8" and package test : Teradyne IP750
- CCD and CMOS
- Dedicated benches for complete electro-optical characterisation
- Geometrical measurements

Life-cycle management

- Dedicated secured storage areas
- Long term supply methodology
- Experience of deliveries from start of wafer storage : 20+ years

Figure 12 - Te2v's Advanced Assembly technology that can be used in SIP assembly



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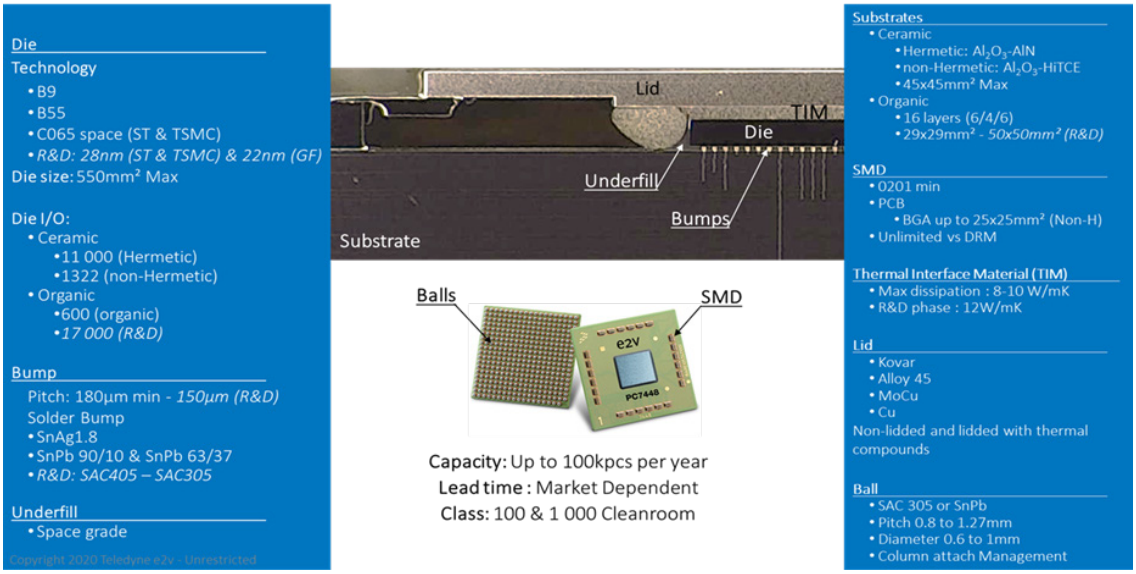


Figure 13 - Te2v's Advanced Wire-bond (top) and Flip-chip (bottom) Assembly Capabilities, that can be used in SIP assembly

Figure 13 shows Te2v's advanced SiP wire-bond and flip-chip assembly technologies. In regards to wire-bonding, Figure 13 (top) shows the multitude of technological assembly variations that are required in order to meet state-of-the-art developments for required semiconductor types (i.e. Si, GaN, GaAs etc.) as well as package types. As new generations of semiconductors and packages are released, new wire-bonding technologies must also be developed in order to meet performance demands. Wire-bonding accounts for approximately two-thirds of all electronic packaging assemblies (including flash memories and sensors, etc.). For some silicon nodes, utilizing advanced flip-chip interconnectivity is not feasible for components such as MEMS sensors, etc. In these cases, wire-bonding still has an advantage in terms of cost and reliability.

Flip-chip technology (also Figure 13 above) is based on an array of bumps or copper pillars that are formed on top of the semiconductor. Processing a flip-chip is similar to conventional IC fabrication, with a few additional steps. Near the end of the manufacturing process, attachment pads are metalized or prepared with solder finishing to make them more receptive to solder. Solder bumps are then deposited on the chip pads on the top side of the wafer during the final wafer processing. Chips are then cut out of the wafer as usual. In order to mount the chip to external circuitry (i.e. SiP circuit board and/or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is reflowed (typically using a thermosonic bonding or alternatively reflow soldering processes) in order to complete the interconnect. This also leaves a small space between the chip's circuitry and the underlying mounting. In many cases an electrically-insulating adhesive is then «underfilled» to provide a stronger mechanical connection, provide a heat bridge, and to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system. The underfill distributes the thermal expansion mismatch between the chip and the board, preventing stress concentration in the solder joints which would lead to premature failure. Flip-chip technology is utilized in contrast to wire bonding, in which the chip is simply mounted upright and wires are used to interconnect the chip pads to external circuitry.

TE2V: ONE-STOP SHOP FOR ADVANCED SIP DESIGN AND ASSEMBLY TECHNOLOGY SERVICES

SiPs reduce the overall cost of specific products and systems, during performance life-times, especially when compared to other design options (such as SoC, etc.) SiP has benefits that will save overall system development costs at every stage of a product lifecycle, such as:

1. Reduced Engineering Costs: Significantly reduces the effort to complete a design in regards to engineering development time, materials, and reducing time-to-market,
2. Reduced PCB Costs: Simplifies the development and use of specific components (utilizing either COTS or custom semiconductors),
3. Reduced Assembly Costs: Integrating multiple components into a single package saves significantly during the overall manufacturing process for a system,
4. Reduced Supply Chain Cost: Simplifies the supply chain. Multiple components from different manufacturers are replaced by a single SiP implementation. Managing fewer components with fewer suppliers simplifies the supply chain dramatically.
5. Verification: testing, and qualification at the sub-system and system level.

Te2v's advanced SiP design and assembly services becomes a "one-stop shop" for all market segments and product types (see Figure 14). Simply put, because Te2v provides design, assembly and qualification services for space-level applications, all other market segments, applications, and quality levels can also be realized as well.

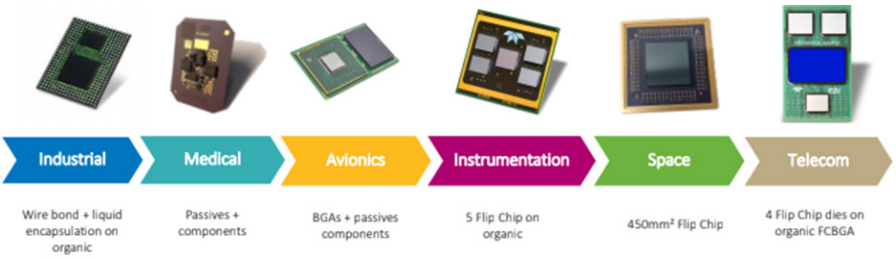
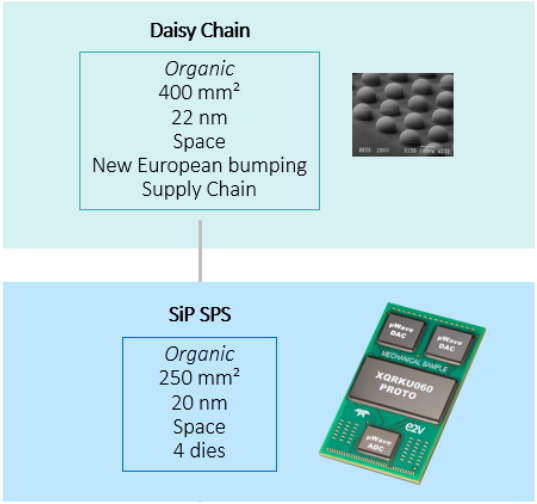


Figure 14

Finally, as the future of advanced system developments enter the next decade, utilizing SiP technologies, it becomes of paramount importance to be able to assemble devices with ever decreasing gate lengths which ultimately increase the area dimensions of the semiconductor. As larger and larger SoC's increasingly become one, of many, of the other components contained within a SiP, the requirement to reliably assemble (wire-bond or flip chip) utilizing organic substrates and packaging materials require significant technological investments. Currently, Te2v is preparing these types of technological advancements in the years to come (see Figure at right), with all technological developments being sponsored by ESA.



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CONCLUSION

Currently, data conversion system designers are experiencing crucial design parameter challenges in regards to semiconductor process choices (and geometries), circuit miniaturization requirements, along with increasing development costs. In addition, newer ADC, DAC, Microprocessor, and Memory components continue to become available for advanced system developments. From industrial, to medical, to avionics, to instrumentation, to telecommunications, to military, and space applications; one system level design problem has been consistent throughout—balancing the implementation tradeoffs between the analog and digital circuitry for maximum software/system flexibility (from sensor to computer input/output). Now, as the future of advanced SiP (System-in-Package) assembly technologies accelerate data conversion system design implementations from hardware to software centricity, for all advanced market segments and applications; Teledyne e2v's SiP design, development, and assembly expertise revolutionizes system level design for maximum flexibility and multi-mission capability. Utilizing 40+ years of package design experience with RF, Mixed-Signal and Digital Processing applications, using state-of-the-art technologies (wire-bond, flip chip, organic packages, etc.); Teledyne e2v's advanced SiP design and assembly technologies give system designers the highest performance and value for high frequency and direct RF data conversion system platforms.

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