e2v

ADC 8-bit 1 Gsps TSEV8388B Evaluation Board

User Guide

Table of Contents

Section 5

Section 6

e2v

Section 1
Overview

1.1 Description

The TSEV8388B Evaluation Board (EB) is a prototype board which has been designed in order to facilitate the evaluation and the characterization of the TS8388B device up to its 1.8 GHz full power bandwidth at up to 1 Gsps in the extended temperature range.

The high speed of the TS8388B requires careful attention to circuit design and layout to achieve optimal performance. This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8388B ADC performances over the temperature range.

The TS8388B Evaluation Board (EB) is very straightforward as it only implements the TS8388B ADC device, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with high frequency acquisition system probes.

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the inputs microstrip lines, and a die junction temperature measurement setting.

The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

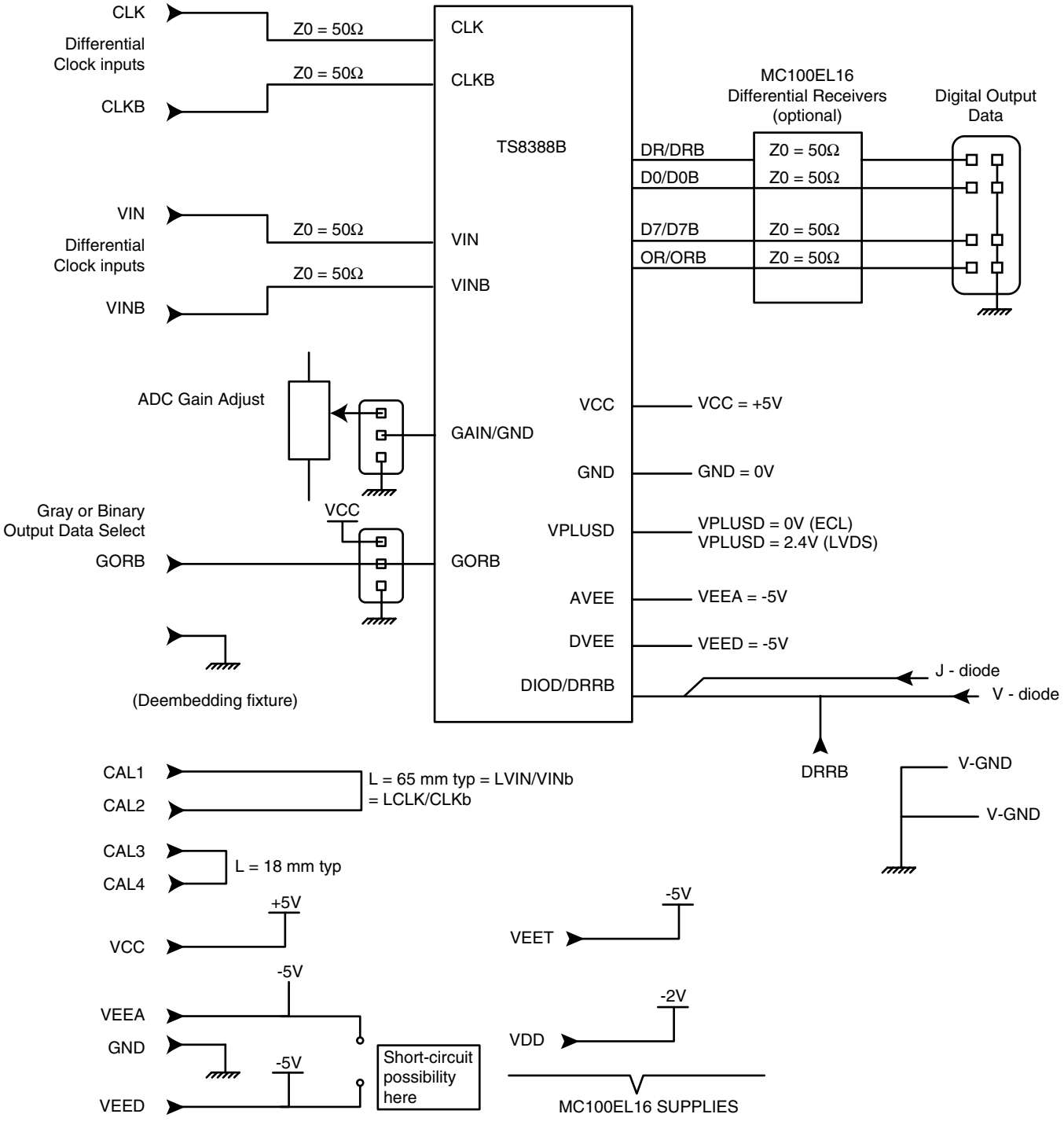
The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TS8388B installed and heatsink.

The 8-bit 1 Gsps ADC evaluation board is fully compatible with its companion device evaluation board (TSEV81102G0 DMUX).

1.2 TSEV8388B Evaluation Board

Figure 1-1. TSEV8388B Block Diagram



1.3 Board Mechanical Characteristics

The board layer's number, thickness, and functions are given below, from top to bottom.

Table 1-1. Board Layers Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 35 µm AC signals traces = 50Ω microstrip lines DC signals traces (GORB, GAIN, DIODE)
Layer 2 RO4003 dielectric layer (Hydrocarbon/Wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz –0.044 dB/inch insertion loss at 2.5 GHz –0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper ground plane = reference plane 50Ω microstrip return
Layer 4 BT/Epoxy dielectric layer	Layer thickness = 630 µm
Layer 5 Copper layer	Copper thickness = 35 µm Lower ground plane (board mechanical rigidity)
Layer 6 BT/Epoxy dielectric layer	Layer thickness = 630 µm
Layer 7 Copper layer	Copper thickness = 35 µm Power planes = V_{EEA}, V_{EED}, V_{EET}, V_{DD}, V_{CC}, V_{PLUSD} ground plane

The TSEV8388B is a seven-layer PCB constituted by four copper layers and three dielectric layers.

The four metal layers correspond respectively from top to bottom to the AC and DC signals layer (layer 1), two ground layers (layers 3 and 5), and one supply layer (layer 7).

The upper inner ground plane (layer 3) constitutes the reference plane for the 50Ω impedance signal traces. The lower inner ground plane (layer 5) is used for dielectric substrate rigidity and is a replica of the upper ground plane.

The backside metal layer is dedicated to the power supplies planes, surrounded by a ground plane.

The three dielectric layers are respectively (from top to bottom) constituted by a low insertion loss dielectric layer (RO4003) (layer 2) and two parallel BT/Epoxy dielectric layers (layers 4 and 6).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, it is necessary to use a sandwich of two different dielectric materials, with specific characteristics:

- A low insertion loss RO4003 Hydrocarbon/wovenglass dielectric layer of 200 µm thickness, chosen for its low loss (–0.318 dB/inch) and enhanced dielectric consistency in the high frequency domain. The RO4003 dielectric layer is dedicated to the routing of the 50Ω impedance signal traces (the RO4003 typical dielectric constant is 3.4 at 10 GHz). The RO4003 dielectric layer characteristics are very close to PTFE in terms of insertion loss characteristics.
- A BT/Epoxy dielectric layer of 2 mm total thickness which is sandwiched between the upper ground plane and the back-side supply layer.

The BT/Epoxy layer has been chosen because of its enhanced mechanical characteristics for elevated temperature operation. The typical dielectric constant is 4.5 at 1 MHz.

More precisely, the BT/Epoxy dielectric layer offers enhanced characteristics compared to FR4 Epoxy, namely:

- Higher operating temperature value: 170°C (125°C for FR4).
- Better with standing of thermal shocks (–65°C up to 170°C).

The total board thickness is 2.6 mm. The previously described mechanical and frequency characteristics makes the board particularly suitable for the device evaluation and characterization in the high frequency domain and in the military temperature range.

1.4 Analog Input, Clock Input and De-embedding Fixture Accesses

The differential active inputs (Analog, Clock, De-embedding fixture) are provided by SMA connectors.

Reference: VITELEC 142-0701-851.

1.5 Digital Outputs Accesses

Access to the differential output data port is provided by a 2.54 mm pitch connector, compatible with the High Speed Digital Acquisition System. It enables access to the converter output data, as well as proper 50Ω differential termination.

1.6 Power Supplies and Ground Accesses

The power supplies accesses are provided by five 4 mm section banana jacks respectively for V_{EEA}, V_{EED}, V_{EET}, V_{DD}, V_{PLUSD} and V_{CC}.

The Ground accesses are provided by 4 mm and two 2 mm banana jacks.

1.7 ADC Functions Settings Accesses

For ADC functions settings accesses (GORB, Die junction temp., ADC gain adjust), smaller 2 mm section banana jacks are provided.

A potentiometer is provided for ADC gain adjust.

0973D–BDC–02/09

e2v

Section 2
Layout Information

2.1 Board

The TS8388B requires proper board layout for optimum full speed operation.

The following explains the board layout recommendations and demonstrates how the Evaluation Board fulfills these implementation constraints.

A single low impedance ground plane is recommended, since it allows the user to lay out signal traces and power planes without interrupting the ground plane.

Therefore a multi-layer board structure has been retained for the TSEV8388B.

Four copper metal layers are used, dedicated respectively (from top to bottom) to the signal traces, ground planes and power supplies.

The input/output signal traces occupy the top metal layer.

The ground planes occupy the second and third copper metal layers.

The bottom metal layer is dedicated to the power supplies.

2.2 AC Inputs/Digital Outputs

The board uses 50Ω impedance microstrip lines for the differential analog inputs, clock inputs, and differential digital outputs (including the out-of-range bit and the data ready output signal).

The input signals and clock signals must be routed on one layer only, without using any through-hole vias. The line lengths are matched to within 2 mm.

The digital output lines are 50Ω differentially terminated.

The output data traces lengths are matched to within 0.25 inch (6 mm) to minimize the data output delay skew.

For the TSEV8388B the propagation delay is approximately 6.1 ps/mm (155 ps/inch). The RO4003 typical dielectric constant is 3.4 at 10 GHz.

For more informations about different output termination options, refer to the specification application notes.

2.3 DC Functions Settings

The DC signals traces are low impedance.

They have been routed with 50Ω impedance near the device because of room restriction.

2.4 Power Supplies

The bottom metal layer 7 is dedicated to the power supply traces (V_{EEA}, V_{EED}, V_{EET}, V_{CC}, V_{DD}, V_{PLUSD}).

The supply traces are approximately 6 mm wide in order to present low impedance, and are surrounded by a ground plane connected to the two inner ground planes.

The Analog and Digital negative power supply traces are independent, but the possibility exists to short-circuit both supplies on the top metal layer.

No difference in ADC high speed performance is observed when connecting both negative supply planes together. Obviously one single negative supply plane could be used for the circuit.

Each power supply incoming is bypassed by a 1 µF Tantalum capacitor in parallel with 1 nF chip capacitor.

Each power supply access is decoupled very close to the device by a 10 nF and 100 pF surface mount chip capacitors in parallel.

Note: The decoupling capacitors are superposed. In this configuration, the 100 pF capacitors must be mounted first.

2.5 TS8388B On-board Implementation

Surface-mount resistors and chip capacitors allow the closest possible connections to the device pins, for microstrip line back termination and bypassing.

- Connecting the positive supply pads:
  - The positive supply pads denoted V_{CC}:
    The corresponding V_{CC} pad numbers are 19, 21, 23, 30, 39, 40.
    Each V_{CC} power supply pad is decoupled as closely to the device as possible by a 1 nF chip capacitor.
    The V_{CC} supply pads are connected to the back side V_{CC} plane of the CEB.
  - The positive digital supply pads are denoted V_{PLUSD} (0V or 2.4V).
    The corresponding V_{PLUSD} pad numbers are 1, 11.
    Each V_{PLUSD} power supply pad is decoupled very close to the device by a 1 nF chip capacitor.
    The V_{PLUSD} supply pads are connected to the back side V_{PLUSD} plane of the evaluation board.
- Connecting the negative supply pads:
  - The TS8388BGL has separate analog and digital –5V supplies:
    The negative analog supply pads are denoted V_{EE}.
    The V_{EE} corresponding pad numbers are 22, 29, 31.
    The negative digital supply pad is denoted DV_{EE}.
    The DV_{EE} corresponding pad number is pad 6.
    The DV_{EE} supply pad is dedicated to the digital output buffers only.
    Each V_{EE} and DV_{EE} power supply pad is decoupled as closely as possible near the device by a 1 nF chip capacitor.
  - The V_{EE} and DV_{EE} supply pads are respectively connected to the backside layer 7 V_{EE} and V_{EED} supply planes.
- Ground pads connections:
  - The analog ground pads are denoted GND.
    The corresponding GND pad numbers are 20, 26, 28, 33, 35, 37.

0973D–BDC–02/09

e2v

Section 3

Operating Procedures and Characteristics

3.1 Introduction

This section describes a typical single-ended configuration for analog inputs and clock inputs.

The single-ended configuration is preferable, as it corresponds to the most straightforward and quickest TSEV8388B board setting for evaluating the TS8388B at full speed in the military temperature range.

The inverted analog input V_{INB} and clock input CLKB common mode level is Ground (on-board 50Ω terminated). In this configuration, no balun transformer is needed to convert properly single-ended mixer output to balanced differential signals for the analog inputs.

In the same way, no balun is necessary to feed the TS8388B clock inputs with balanced signals.

Connect directly the RF sources to the in-phase analog and clock inputs of the converter.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

3.2 Operating Procedure

1. Connect the power supplies and Ground accesses
   (V_{CC} = +5V, GND = 0V, V_{PLUSD} = 0V, V_{EAE} = V_{EED} = –5V) through the dedicated banana jacks.
   The –5V power supplies should be turned on first.
   Note: one single –5V power supply can be used for supplying the digital V_{EED} and analog V_{EEA} power planes.

2. The board is set by default for digital outputs in binary format.

3. Connect the CLK clock signal.
   The inverted phase clock input CLKB may be left open (as on-board 50Ω terminated). Use a low phase noise RF source. The clock input level is typically 4 dBm and should not exceed +10 dBm into the 50Ω termination resistor (maximum ratings for clock input power level is 15 dBm). Clock frequency can range between 10 MHz and 1.4 Gsps.

4. Connect the analog signal V_{IN}. The inverted phase clock input V_{INB} may be left open (as on-board 50Ω terminated). Use a low phase noise RF source. Full Scale range is 0.5V peak to peak around 0V, (±250 mV), or –2 dBm into 50Ω. Input frequency can range from DC up to 1.8 GHz. At 1.8 GHz, the ADC attenuates by –3 dB the input signal.
5. Connect the high speed data acquisition system probes to the output connector. The connector pitch (2.54 mm) is compatible with High Speed Digital Acquisition System probes. The digital data are on-board differentially terminated. However, the output data can be picked up either in single-ended or differentially mode.
6. Board functionality verification and proposed product evaluation procedure:
   – A first test can be run at 500 Msps/250 MHz Nyquist: about 7.4 Effective Bits (typ) should be obtained.
   – At 1 Gsps/500 MHz: about 7.0 Effective Bits (typ) should be obtained.
   – At 1 Gsps/1 GHz and –1 dB Full Scale analog input, 6.4 bits and -43 dBc SFDR should be obtained. In the same conditions for –3 dB Full Scale input, 6.8 bits and –48 dBc are obtained.
7. The devices operate respectively from 10 Msps up to 1.4 Gsps in binary output format and 10 Msps up to 2 Gsps in Gray output format. It is capable of sampling analog input waveforms ranging from DC up to 1.5 GHz.

3.3 Electrical Characteristics

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}(2)		GND to –5.7	V
Digital positive supply voltage	V_{PLUSD}		GND –0.3 to 2.8	V
Negative supply voltage	V_{EE}(2)		GND to –6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		–1 to +1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		–2 to +2	V
Clock input voltage	V_{CLK} or V_{CLKB}		–3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		–2 to +2	V
Static input voltage	V_D	GORB	–0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} –0.3 to +0.9	V
Digital output voltage	V_O		V_{PLUSD} –3 to V_{PLUSD} –0.5	V
Maximum junction temperature	Tj		+145	°C
Storage temperature	T_{stg}		–65 to +150	°C
Lead temperature (soldering 10s)	T_{leads}		+300	°C

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory.
2. In case only one supply is used for supplying the –5V negative power planes, apply the V_{EED} absolute maximum ratings.

3.4 Operating Charcteristics

The power supplies denoted V_{CC}, V_{EEA}, V_{EED} and V_{PLUSD} are dedicated for the TS8388B ADC.

The power supplies denoted V_{EET}, V_{DD} are dedicated to the optional MC100EL16 asynchronous differential receivers.

Table 3-2. Electrical Operating Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Positive supply voltage (dedicated to TS8388B ADC only)	V_{CC}	4.75	5	5.25	V
	V_{PLUSD}	 LVDS: 1.4	ECL: –0.8 LVDS: 1.6	 LVDS: 2.6	V V
	V_{EEA}	–5.25	–5	–4.75	V
	V_{EED}	–5.25	–5	–4.75	V
Positive supply current	I_{CC}	–	400	425	mA
	I_{PLUSD}	–	120	130	mA
	I_{EEA}	–	170	185	mA
	I_{EED}	–	140	160	mA
Positive supply voltage not used by default – If installed (dedicated to MC100EL16 differential Receivers)	V_{EET}	–5.25	–5	–4.75	V
	V_{DD}	–2.15	–2	–185	V
Positive supply current not used by default – If installed (dedicated to MC100EL16 differential Receivers)	I_{EET}	–	150	–	mA
	I_{DD}	–	390	–	mA
Nominal power dissipation (without receivers)	PD	–	3.6	3.9 (Tj = 125°C)	W
Analog input impedance	Z_{IN}	–	50	–	Ω
Full Power Analog Input Bandwidth (–3 dB)	–	1.3	1.5	–	GHz
Full Power Analog Input Bandwidth (–3 dB) CBGA68 packaged device CQFP68 packaged device	– – –	– 1.3 1.3	– 1.8 1.5	– – –	– GHz GHz
Analog Input Voltage range (differential mode)	V_{IN}	–125	–	125	V
Clock input impedance	–	–	50	–	Ω
Clock inputs voltage compatibility (Single-ended or differential) (See Application Notes)	–	ECL levels or 4 dBm (typ.) into 50Ω			–
Clock input power level into 50Ω termination resistor	–	–2	4	10	dBm

e2v

Section 4
Application Information

4.1 Introduction

For this section, refer also to the product Specification application notes (TS8388BGL Datasheet). More particularly, refer to sections related to single-ended and differential input configurations.

4.2 Analog Inputs

The analog inputs can be entered in differential or single-ended mode without any high speed performance degradation.

The board digitizes single-ended signals by choosing either input and leaving the other input open, as the latter is on-board 50Ω terminated. The nominal In-phase inputs are V_{IN} (See Section 3).

4.3 Clock Inputs

The clock inputs can be entered in differential or single-ended mode without any high speed performance degradation. Moreover, the clock input common mode may be 0V, or -1.3V if ECL input format is used for the clock inputs.

As for the analog input, either clock input can be chosen, leaving the other input open, as both clock inputs are on-board 50Ω terminated. The nominal in-phase clock input is CLK (See Section 3).

4.4 Setting the Digital Output Data Format

For this section, refer to the Evaluation Board Electrical schematic and to the components placement document (respectively Figure 6-1 and Figure 6-7).

Refer also to the TS8388B specification pages about digital output coding.

The TS8388B delivers data in natural binary code or in Gray code. If the “GORB” input is left floating or tied to V_{CC} the data format selected will be natural binary, if this input is tied to ground the data will follow Gray code.

Use the jumper denoted ST2 for selecting the output data port format:

- If ST2 is left floating or tied to V_{CC}, the data output format is true Binary,
- If ST2 is tied to GND, the data outputs are in Gray format.

The V_{PLUSD} positive supply voltage allows the adjustment of the output common mode level from -1.2V (V_{PLUSD} = 0V for ECL output compatibility) to +1.2V (V_{PLUSD} = 2.4V for LVDS output compatibility).

Each output voltage varies between -1.02V and -1.35V (respectively +1.38V and +1.05V), leading to ±0.33V = 660 mV in differential, around -1.8V (respectively +1.21V) common mode for V_{PLUSD} = 0V (respectively 2.4V).

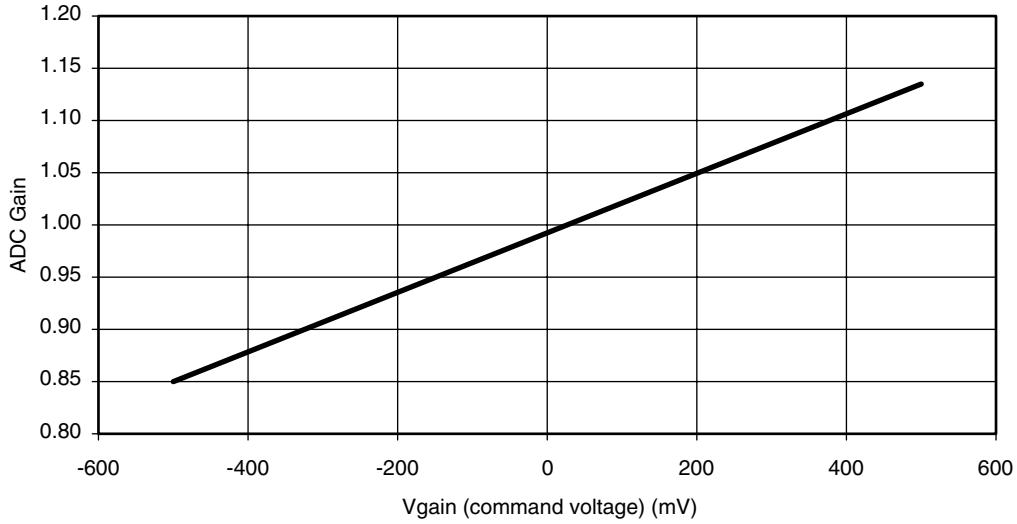
4.5 ADC Gain Adjust

The ADC gain is adjustable by the means of the pin (60) (pad input impedance is 1 MΩ in parallel with 2 pF). A jumper denoted ST1 has been foreseen in order to have access to the ADC gain adjust pin.

The P1 potentiometer is dedicated for adjusting the ADC gain from approximately 0.85 up to 1.15.

The gain adjust transfer function is given below.

Figure 4-1. ADC Gain Adjust



4.6 SMA Connectors and Microstrip Lines De-embedding Fixture

Attenuation in microstrip lines can be found by taking the difference in the log magnitudes of the S21 scattering parameters measured on two different lengths of meandering transmission lines.

Such a difference measurement also removes common losses such as those due to transitions and connectors.

The scattering parameter S21 corresponds to the amount of power transmitted through a two-port network.

The characteristic impedance of the microstrip meander lines must be close to 50Ω to minimize impedance mismatch with the 50Ω network analyzer test ports.

Impedance mismatch will cause ripple in the S21 parameter as a function of both the degree of mismatch and the length of the line.

0973D–BDC–02/09

4.7 Temperature Monitoring and Data Ready Reset Function

One single pad is used for both DRRB input command and die junction monitoring. The pad denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

4.7.1 TS8388B ADC Diode Junction Temperature Measurement Setup

For operation in the extended temperature range, forced convection is required, to maintain the device junction temperature below the specified maximum value (Tj max = 125°C).

A die junction temperature measurement setting has been included on the board, for junction temperature monitoring.

Four 2 mm section banana jacks (J9, J10, J11, J12) are provided to force current and measure the VBE voltage across the dedicated transistor connected between pads 32 and 33.

The measurement method consists of forcing a 3 mA current flowing into a diode mounted transistor, connected between pad 32 and pad 33 (pad 32 is the emitter and pad 33 is the shorted base-collector).

CAUTION:

Respect the current source polarity. In any case, make sure the maximum voltage compliance of the current source is limited to maximum 1V or use the resistor mounted in serial with the current source to avoid damage occurring to the transistor device. This may occur for instance if current source is reverse connected.

The measurement setup is described in Figure 4-2. The diode VBE forward voltage versus junction temperature (in steady state conditions) is given in Figure 4-3.

Figure 4-2. TS8388B Diode Junction Temperature Measurement Setup

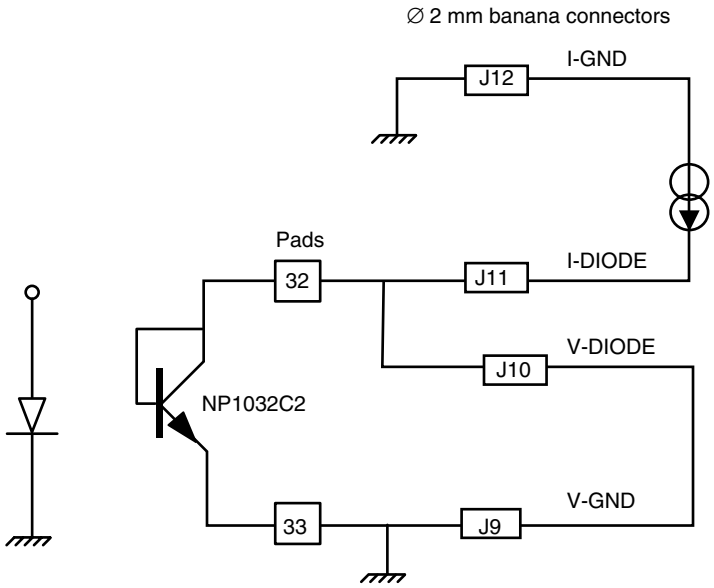
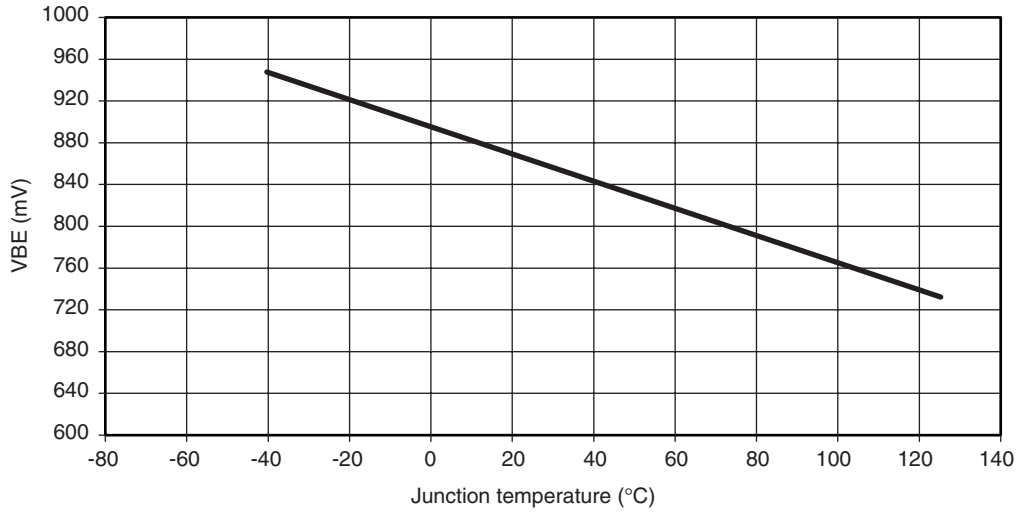


Figure 4-3. Transistor VBE Forward Voltage Versus Junction Temperature (I = 3 mA)



4.8 Data Ready Output Signal Reset

A subvis connector is provided for DRRB command.

The Data ready signal is reset on falling edge of DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal master Reset. As long DRRB as remains at logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typical.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data ready Reset command may be a pulse of 1 ns minimum time width.

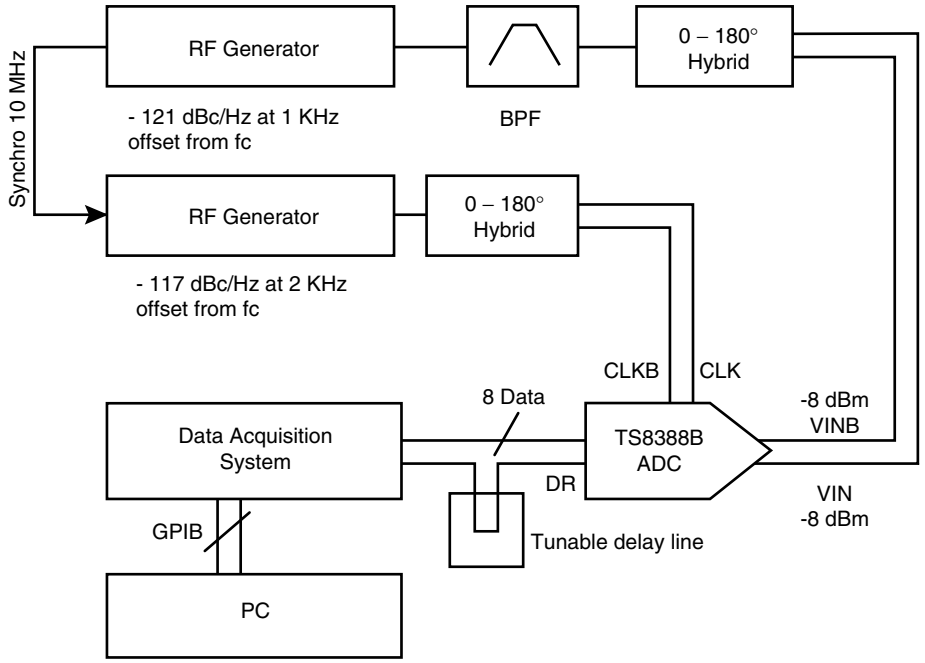
The Data ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V).

DRRB may also be grounded, or is allowed to float, for normal free running Data ready output signal.

0973D–BDC–02/09

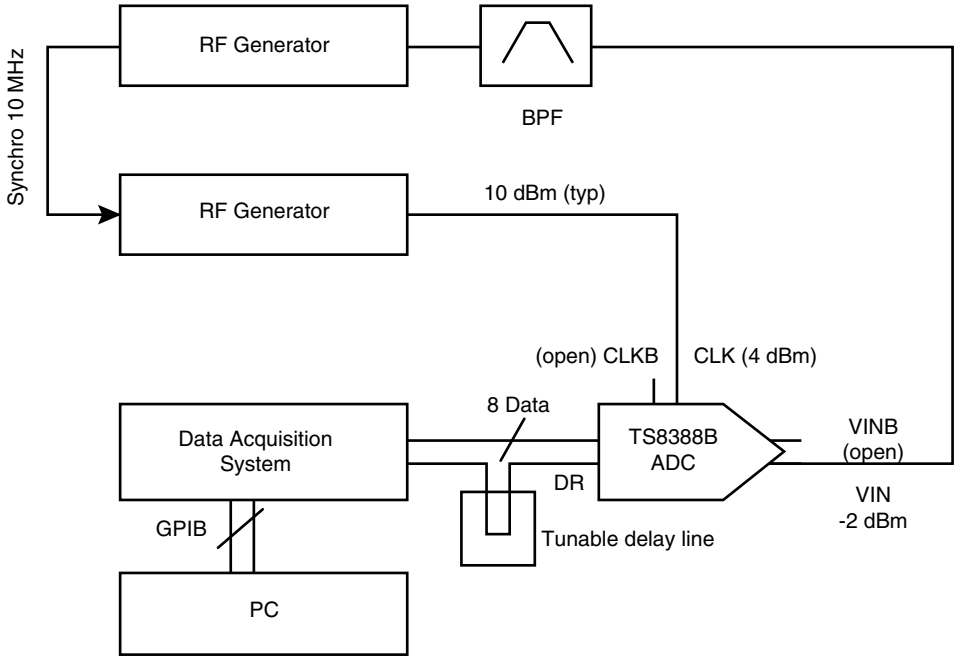
4.9 Test Bench Description

Figure 4-4. Differential Analog and Clock Inputs Configuration



Note: The TS81102G0 DMUX device can be used at the ADC output in order to slow down the ADC output data rate by a factor of 4 or 8.

Figure 4-5. Single-ended Analog and Clock Input Configuration



Note: The TS81102G0 DMUX device can be used at the ADC output in order to slow down the ADC output data rate by a factor of 4 or 8.

Section 5

Package Description

5.1 TS8388BGL Pinout

Figure 5-1. TS8388BGL Pinout of CBGA68 Package

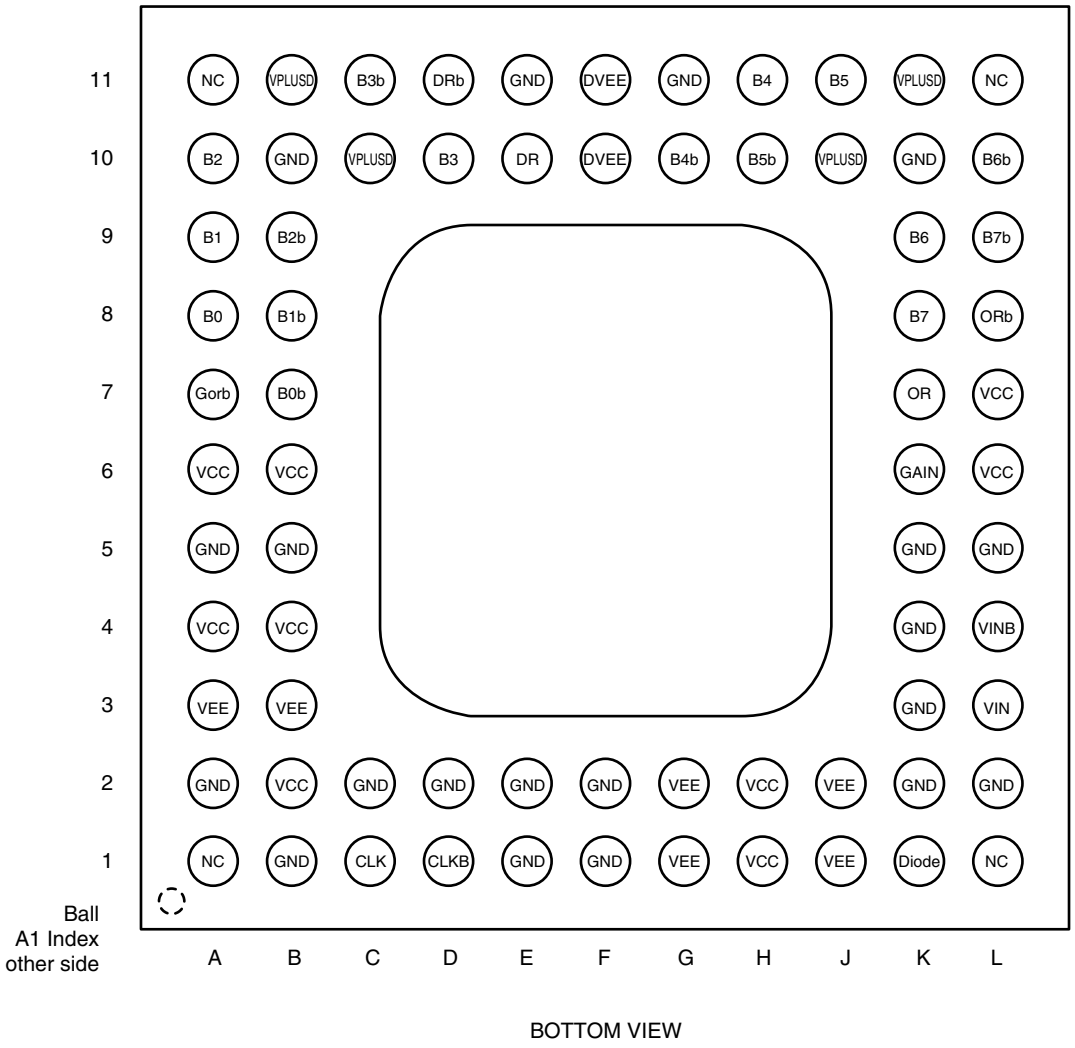


Table 5-1. TS8388BGL Pin Description (CBGA68 Packaged Device)

Symbol	Pin Number	Function
GND	A2, A5, B1, B5, B10, C2, D2, E1, E2, E11, F1, F2, G11, K2, K3, K4, K5, K10, L2, L5	Ground pins. To be connected to external ground plane.
V_{CC}	A4, A6, B2, B4, B6, H1, H2, L6, L7	+5V positive supply.
V_{EE}	A3, B3, G1, G2, J1, J2	5V analog negative supply.
DV_{EE}	F10, F11	–5V digital negative supply.
V_{IN}(1)	L3	In phase (+) analog input signal of the sample and Hold differential preamplifier.
V_{INB}(1)	L4	Inverted phase (-) of ECL clock input signal (CLK).
CLK	C1	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	D1	Inverted phase (-) of ECL clock input signal (CLK).
B0, B1, B2, B3, B4, B5, B6, B7	A8, A9, A10, D10, H11, J11, K9, K8	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
B0B, B1B, B2B, B3B, B4B, B5B, B6B, B7B	B7, B8, B9, C11, G10, H10, L10, L9	Inverted phase (-) Digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	K7	In phase (+) out-of-range bit. Out of range is high on the leading edge of code 0 and code 256.
ORB	L8	Inverted phase (+) of out-of-range bit (OR).
DR	E10	In phase (+) output of Data Ready Signal.
DRB	D11	Inverted phase (-) output of Data Ready Signal (DR).
GORB	A7	Gray or Binary select output format control pin. - Binary output format if GORB is floating or V_{CC}. - Gray output format if GORB is connected at ground (0V).
GAIN	K6	ADC gain adjust pin. The gain pin is by default grounded, the ADC gain transfer function is nominally close to one.
DIOD/DRRB	K1	Die function temperature measurement pin and asynchronous data ready reset active low, single ended ECL input.
V_{PLUSD}	B11, C10, J10, K11	+2.4V for LVDS output levels otherwise to GND(1)
NC	A1, A11, L1, L11	Not connected.

Note: 1. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

0973D–BDC–02/09

5.2 TS8388BF/ TS8388BFS Pinout

Figure 5-2. TS8388BF/TS8388BFS Pinout of CQFP68 Package

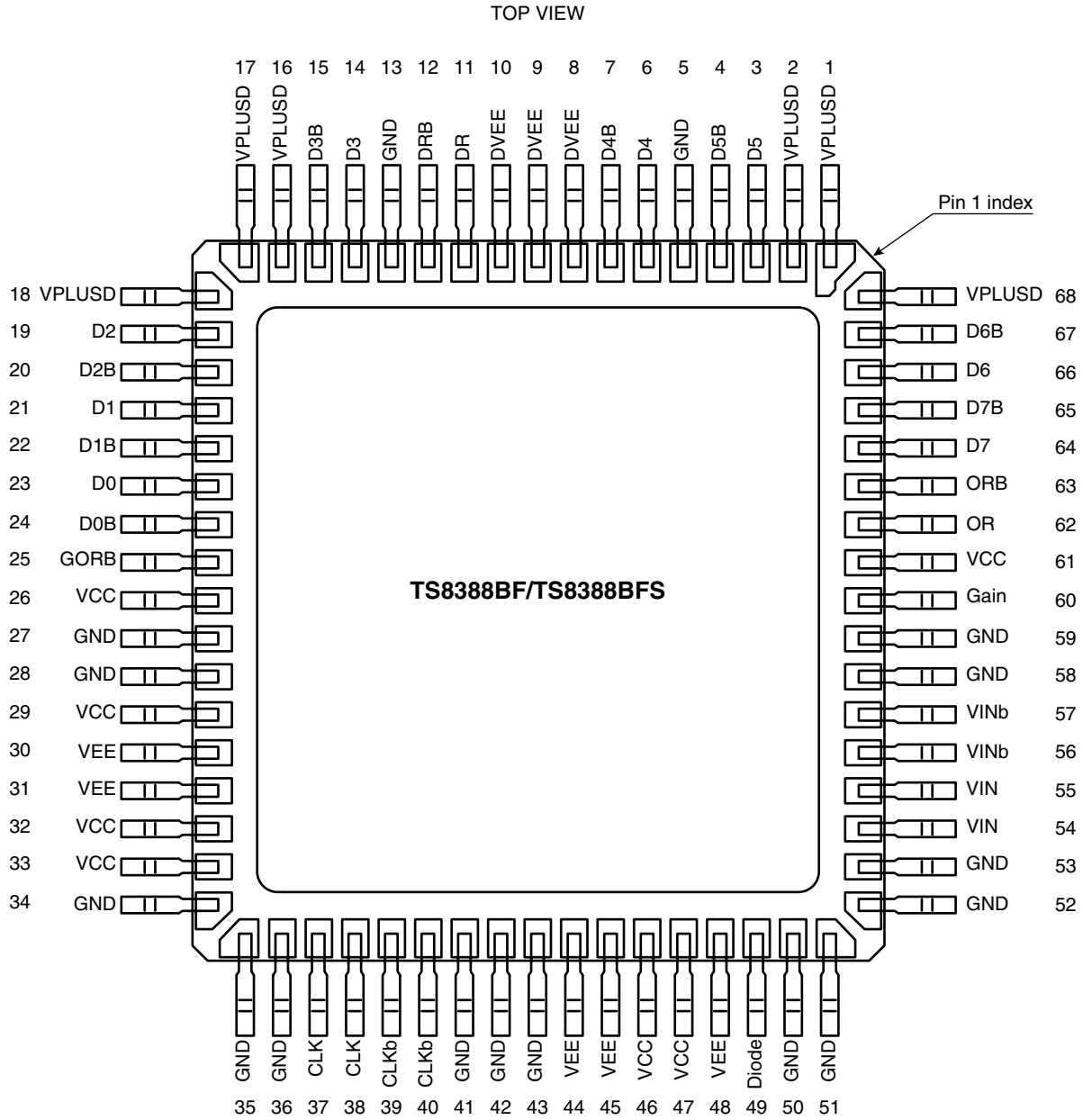


Table 5-2. TS8388BF/TS8388BFS Pin Description (CQFP68 Packaged Device)

Symbol	Pin Number	Function
GND	5, 13, 27, 28, 34, 35, 36, 41, 42, 43, 50, 51, 52, 53, 58, 59	Ground pins. To be connected to external ground plane.
V_{PLUSD}	1, 2, 16, 17, 18, 68	Digital positive supply (0V for ECL compatibility, 2.4V for LVDS compatibility).(2)
V_{CC}	26, 29, 32, 33, 46, 47, 61	+5V positive supply.
V_{EE}	30, 31, 44, 45, 48	–5V analog negative supply.
DV_{EE}	8, 9, 10	–5V digital negative supply.
V_{IN}	54(1), 55	In phase (+) analog input signal of the Sample and Hold differential preamplifier.
V_{INB}	56, 57(1)	Inverted phase (-) of analog input signal (V_{IN}).
CLK	37(1), 38	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	39, 40(1)	Inverted phase (-) of ECL clock input signal (CLK).
D0, D1, D2, D3, D4, D5, D6, D7	23, 21, 19, 14, 6, 3, 66, 64	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B	24, 22, 20, 15, 7, 4, 67, 65	Inverted phase (-) digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	62	In phase (+) out-of-range bit. Out of range is high on the leading edge of code 0 and code 256.
ORB	63	Inverted phase (+) out-of-range bit (OR).
DR	11	In phase (+) output of Data Ready Signal.
DRB	12	Inverted phase (-) output of Data Ready Signal (DR).
GORB	25	Gray or Binary select output format control pin. - Binary output format if GORB is floating or V_{CC}. - Gray output format if GORB is connected at ground (0V).
GAIN	60	ADC gain adjust pin.
DIOD/DRRB	49	This pin has a double function (can be left open or grounded if not used): - DIOD: die junction temperature monitoring pin. - DRRB: asynchronous data ready reset function.

Notes: 1. Following pin numbers 37 (CLK), 40 (CLKB), 54 (V_{IN}) and 57 (V_{INB}) have to be connected to GND through a 50Ω resistor as close as possible to the package (50Ω termination preferred option).

2. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

0973D–BDC–02/09

5.3 CBGA68 Thermal Characteristics

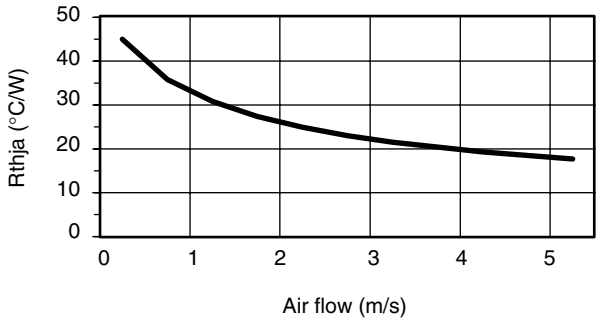
5.3.1 Thermal Resistance from Junction to Ambient: Rthja

The following table lists the converter thermal performance parameters of the device itself, with no external heatsink added.

Table 5-3. Thermal Resistance

Air Flow (m/s)	Estimated ja Thermal Resistance (°C/W)
0	45
0.5	35.8
1	30.8
1.5	27.4
2	24.9
2.5	23
3	21.5
4	19.3
5	17.7

Figure 5-3. Thermal Resistance from Junction to Ambient: Rthja



5.3.2 Thermal Resistance from Junction to Case: Rthjc

Typical value for Rthjc is given to 1.56°C/W.

This value does not include thermal contact resistance between package and external component (heatsink or PCBoard).

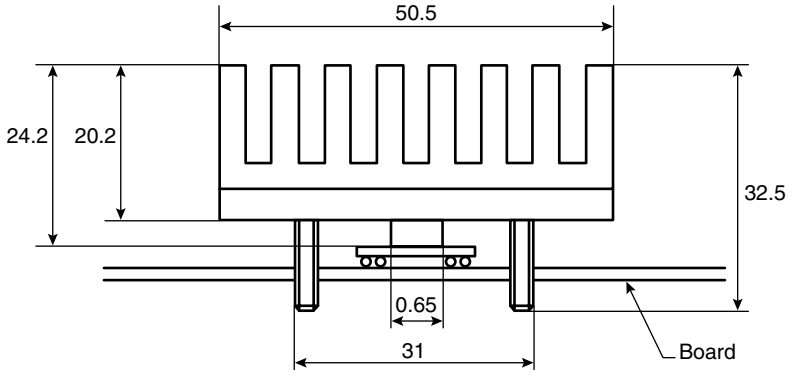
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

5.3.3 CBGA68 Board Assembly with External Heatsink

It is recommended to use an external heatsink or PCBoard special design.

Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

Figure 5-4. CBGA68 Board Assembly



Note: Dimensions are given in mm.

5.4 Nominal CQFP68 Thermal Characteristics

Although the power dissipation is low for this performance, the use of a heat sink is mandatory.

The user will find some advice on this topics below.

5.4.1 Thermal Resistance from Junction to Ambient: Rthja

The following table lists the converter thermal performance parameters, with or without heatsink.

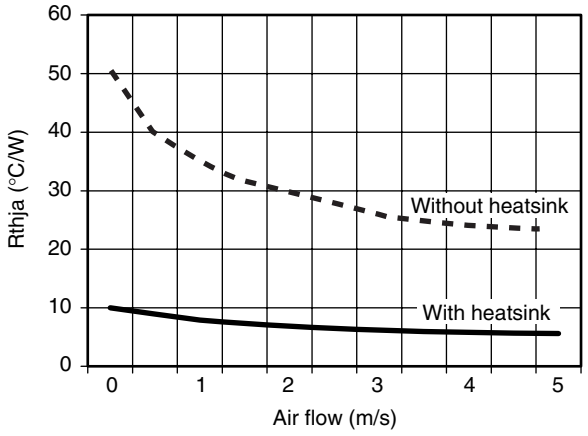
For the following measurements, a 50 x 50 x 16 mm heatsink has been used (see Figure 5-6 on page 7).

Table 5-4. Thermal Resitance

Air Flow (m/s)	ja Thermal Resistance (°C/W) – CQFP68 on Board	
	Estimated – Without Heatsink	Targeted – With Heatsink(1)
0	50	10
0.5	40	8.9
1	35	7.9
1.5	32	7.3
2	30	6.8
2.5	28	6.5
3	26	6.2
4	24	5.8
5	23.5	5.6

Note: 1. Heatsink is glued to backside of package or screwed and pressed with thermal grease.

Figure 5-5. Thermal Resistance from Junction to Ambient: Rthja



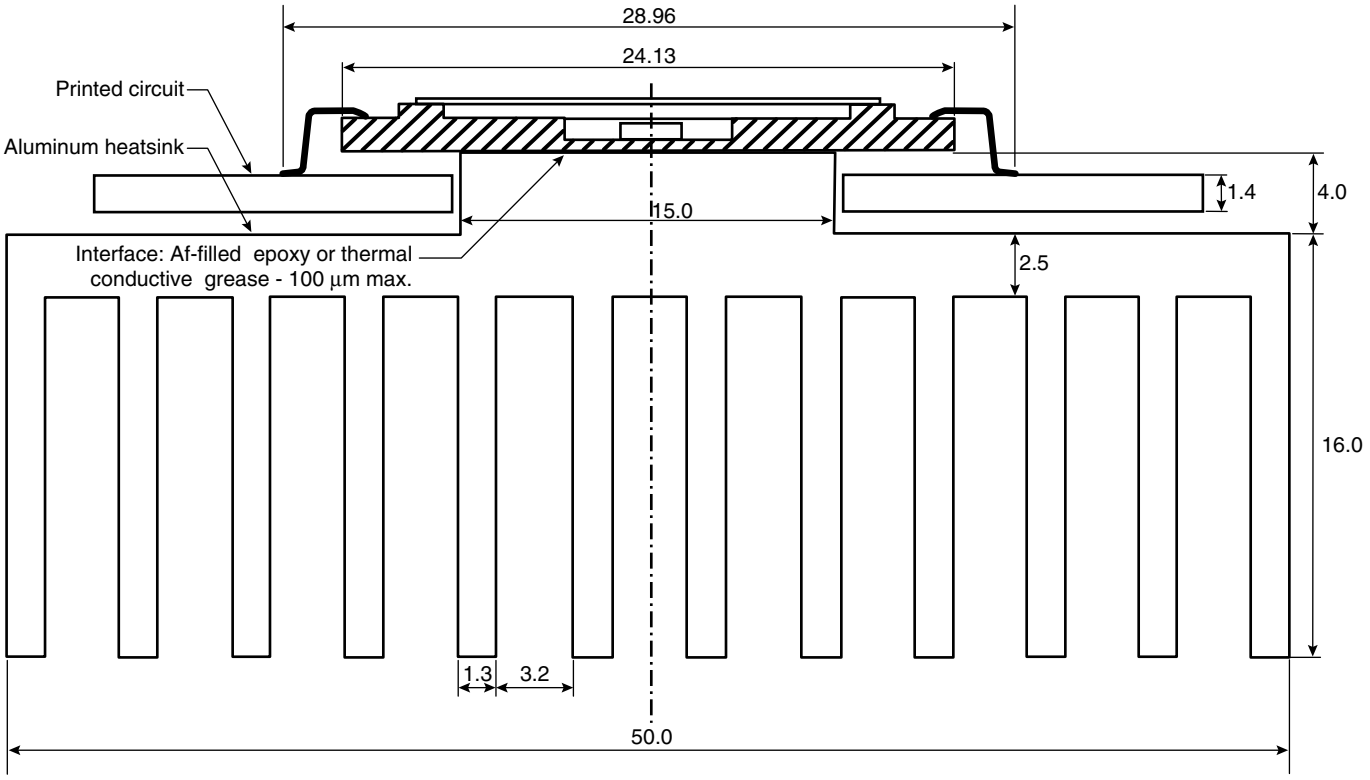
5.4.2 Thermal Resistance from Junction to Case: Rthjc

Typical value for Rthjc is given to 4.75°C/W.

0973D–BDC–02/09

5.4.3 CBGA68 Board Assembly with External Heatsink

Figure 5-6. CQFP68 Board Assembly with a 50 x 50 x 16 mm External Heatsink



5.5 Enhanced CQFP68 Thermal Characteristics

5.5.1 Enhanced CQFP68

The CQFP68 has been modified, in order to improve the thermal characteristics:

- A CuW heatspreader has been added at the bottom of the package.
- The die has been electrically isolated with the ALN substrate.

5.5.2 Thermal Resistance from Junction to Case: Rthjc

Typical value for Rthjc is given to 1.56°C/W.

This value does not include thermal contact resistance between package and external component (heatsink or PCBoard).

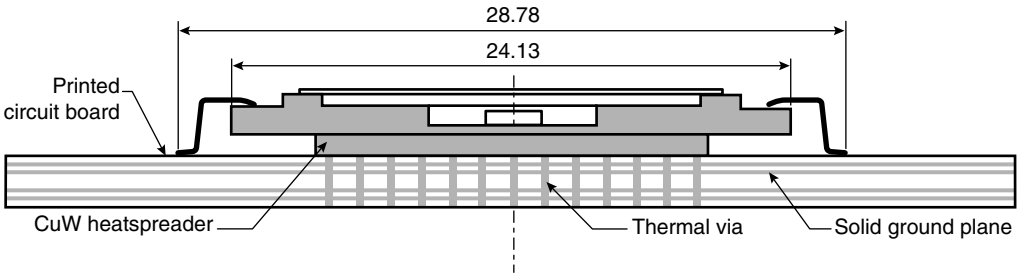
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

5.5.3 Heatsink

It is recommended to use an external heatsink, or PCBoard special design.

The stand off has been calculated to permit the simultaneous soldering of the leads and of the heatspreader with the solder paste.

Figure 5-7. Enhanced CQFP68 Suggested Assembly



Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

0973D–BDC–02/09

5.6 Ordering Information

Table 5-5. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
TS8388BVF	CQFP 68	"V" grade: –40°C < Tc; Tj < 110°C	Standard	
TS8388BMF	CQFP 68	"M" grade: –55°C < Tc; Tj < 125°C	Standard	
TS8388BMF B/Q	CQFP 68	"M" grade: –55°C < Tc; Tj < 125°C	Mil-PRF-38535, QML level Q	DSCC 5962-0050401QYC
TS8388BMFS	CQFP 68 with heatspreader	"M" grade: –55°C < Tc; Tj < 125°C	Standard	
TS8388BMFS B/Q	CQFP 68 with heatspreader	"M" grade: –55°C < Tc; Tj < 125°C	Mil-PRF-38535, QML level Q	DSCC 5962-0050401QXC
TS8388BMFS9NB1	CQFP 68 with heatspreader	"M" grade: –55°C < Tc; Tj < 125°C	- ESA/SCC9000 Screening - Non ESA/SCC qualified - Level B selection - Lot Acceptance Test 1, 2, 3	
TS8388BCGL	CBGA 68	"C" grade: 0°C < Tc; Tj < 90°C	Standard	
TS8388BVGL	CBGA 68	"V" grade: –40°C < Tc; Tj < 110°C	Standard	
TSEV8388BF	CQFP68	Ambient	Prototype	Evaluation Board Contact e2v for availability
TSEV8388BGL	CBGA 68	Ambient	Prototype	Evaluation Board (delivered with heatsink)

Section 6

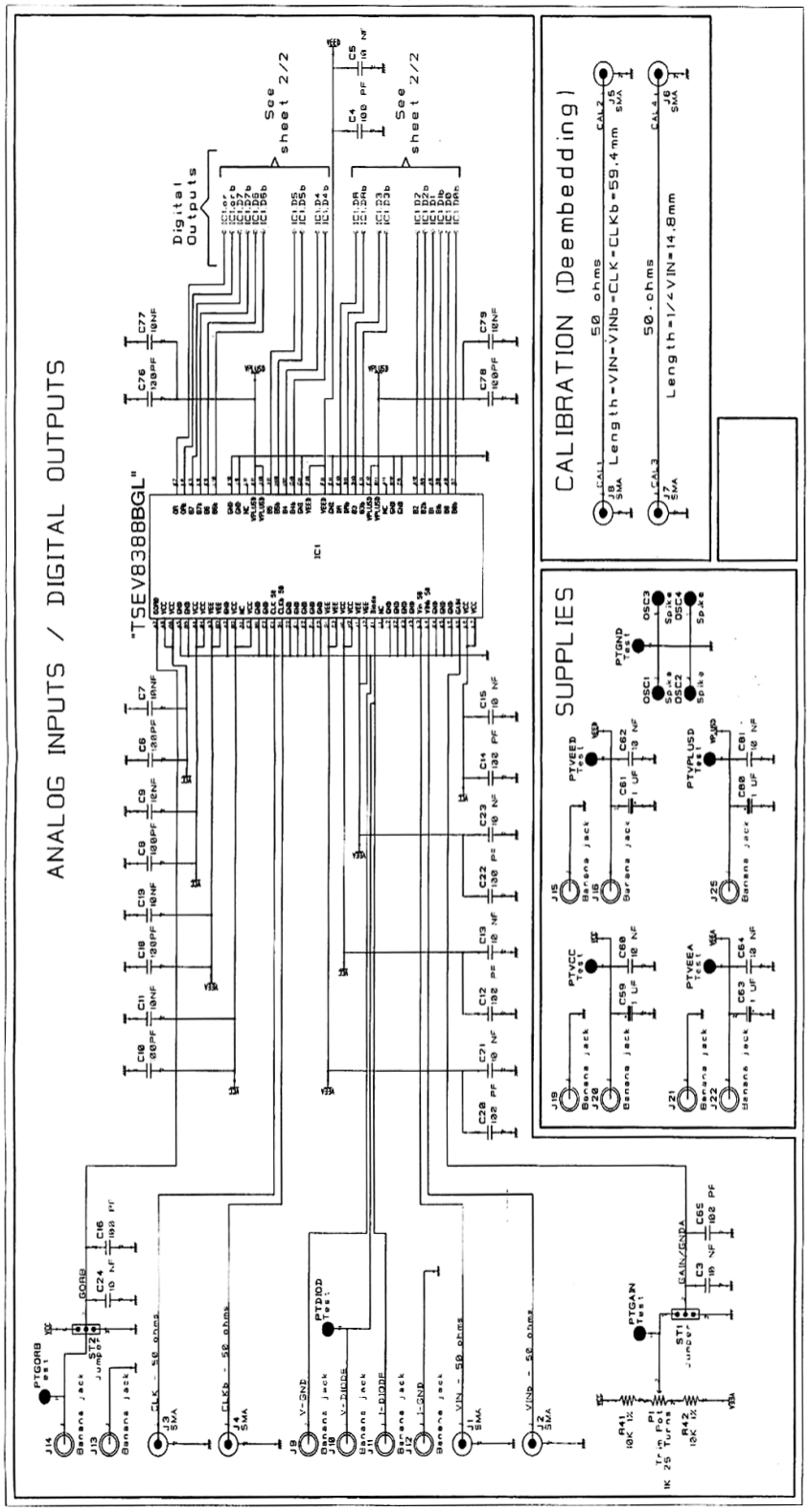
Schematics

6.1 TSEV8388B Electrical Schematics

Please refer to figure 6.1 below.

0973D–BDC–02/09

Figure 6-1. TSEV8388B Electrical Schematic



0973D–BDC–02/09

Figure 6-2. Board Digital Outputs Default Option

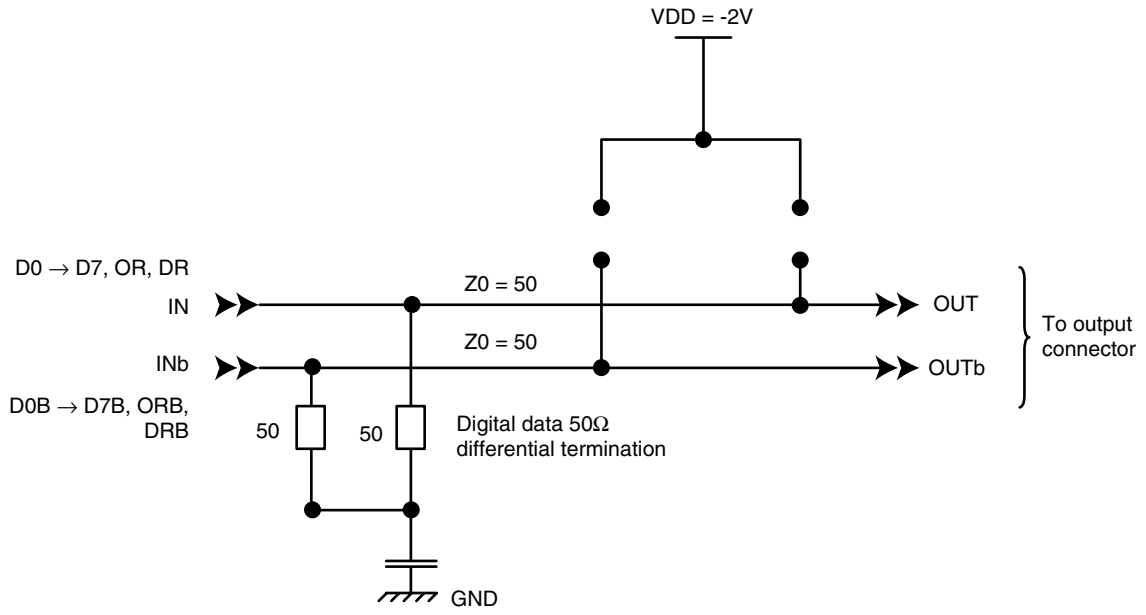
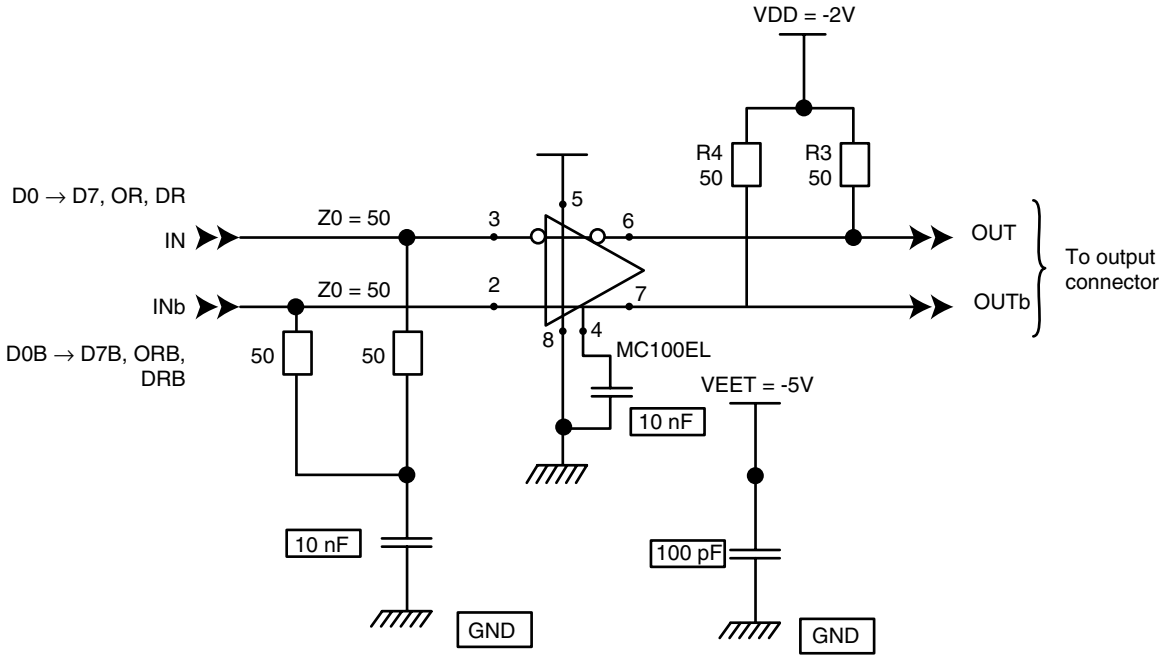


Figure 6-3. Board Digital Outputs Option Using MC100EL16 Differential Receivers



6.2 Evaluation Board Schematics

6.2.1 CBGA68 Option

Figure 6-4. Component Side Description

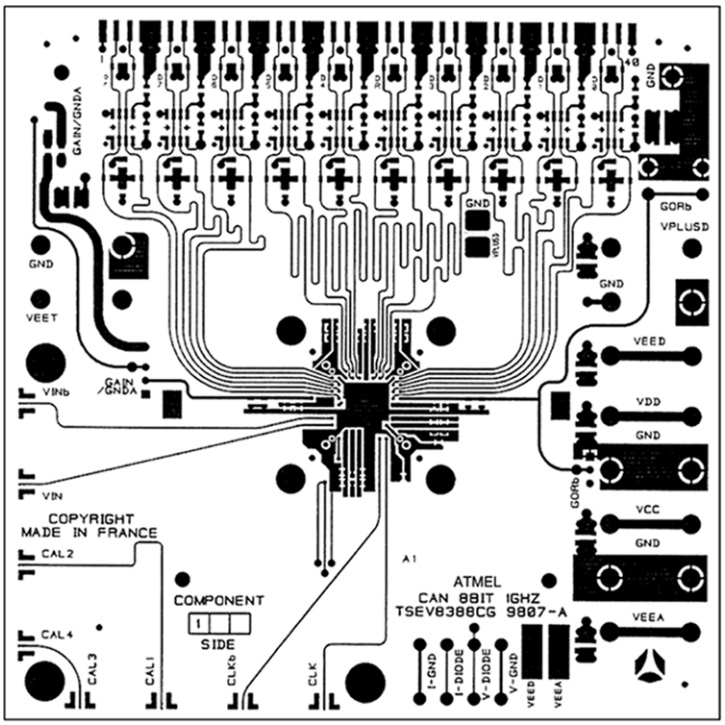


Figure 6-5. Ground Plane

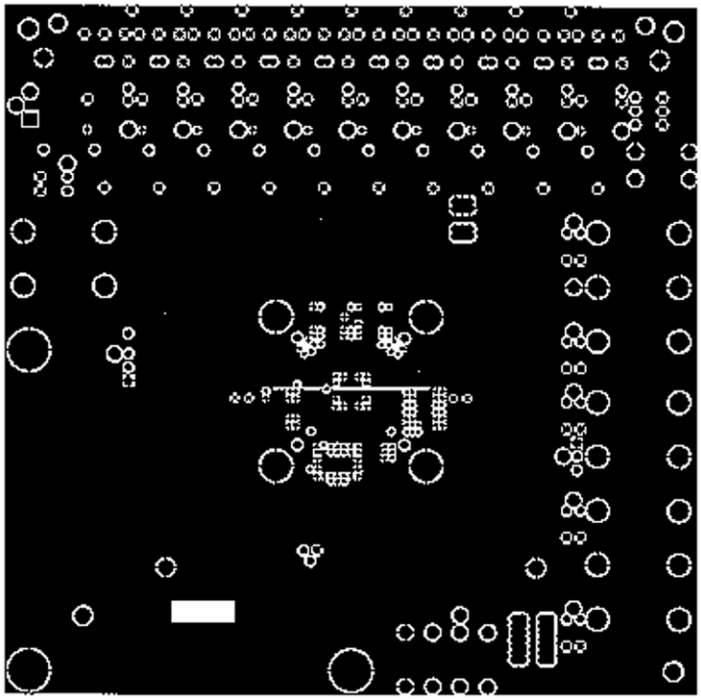


Figure 6-6. Power Supplies Planes

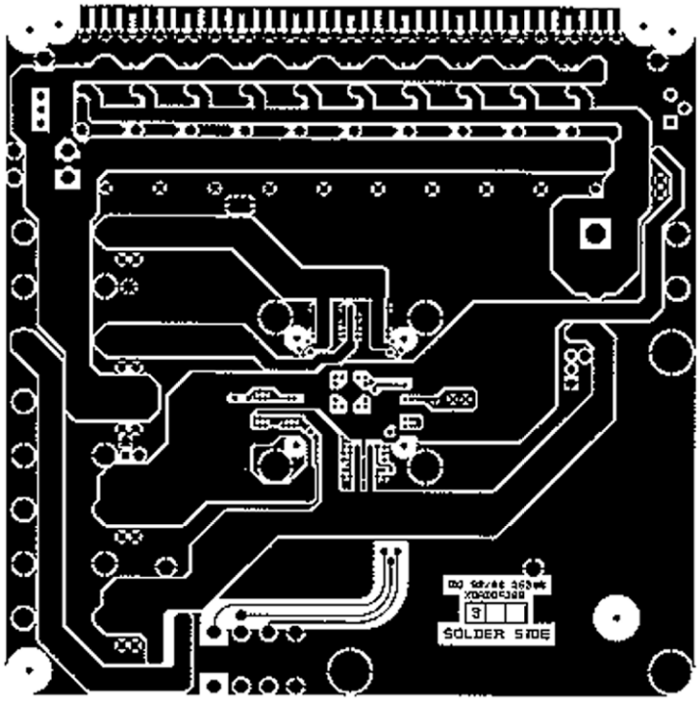
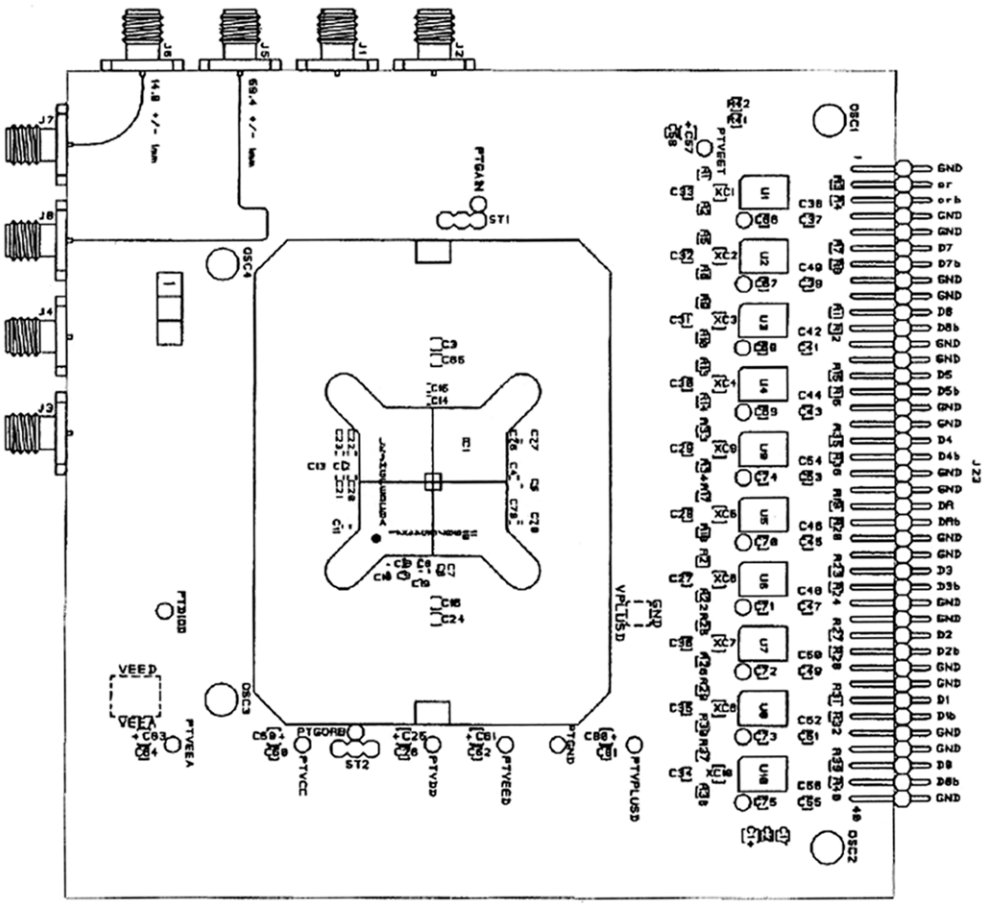


Figure 6-7. TSEV8388B Evaluation Board: Component Placement



6.2.2 CQFP68 Option

Figure 6-8. Component Side Description

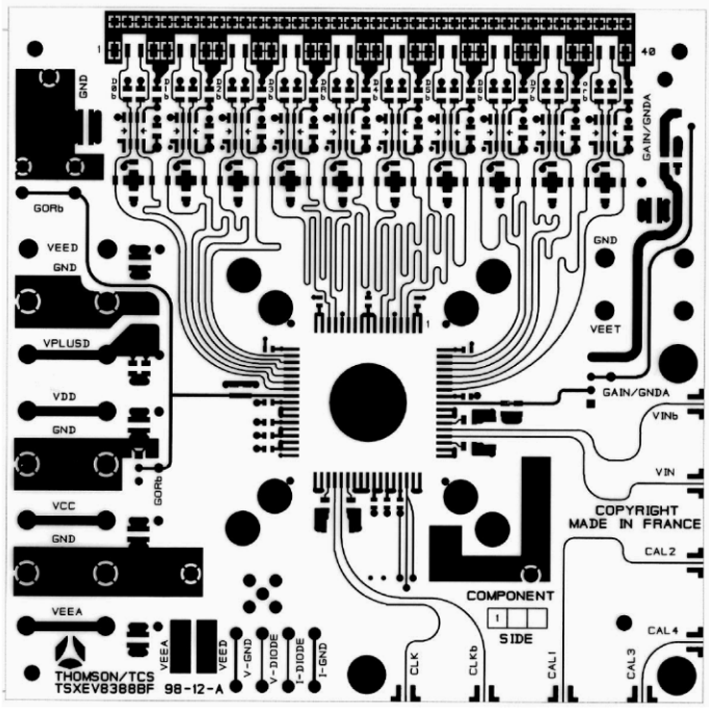


Figure 6-9. Ground Plane

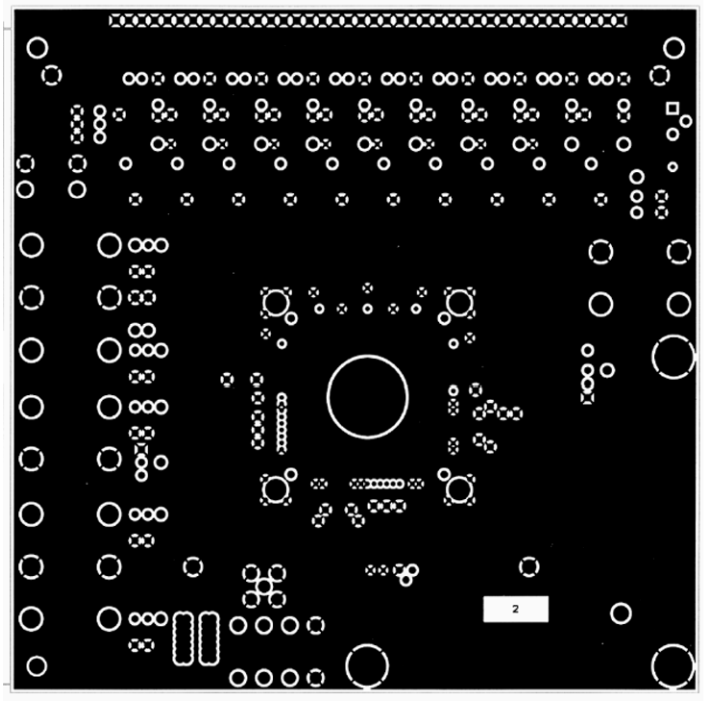


Figure 6-10. Power Supplies Planes

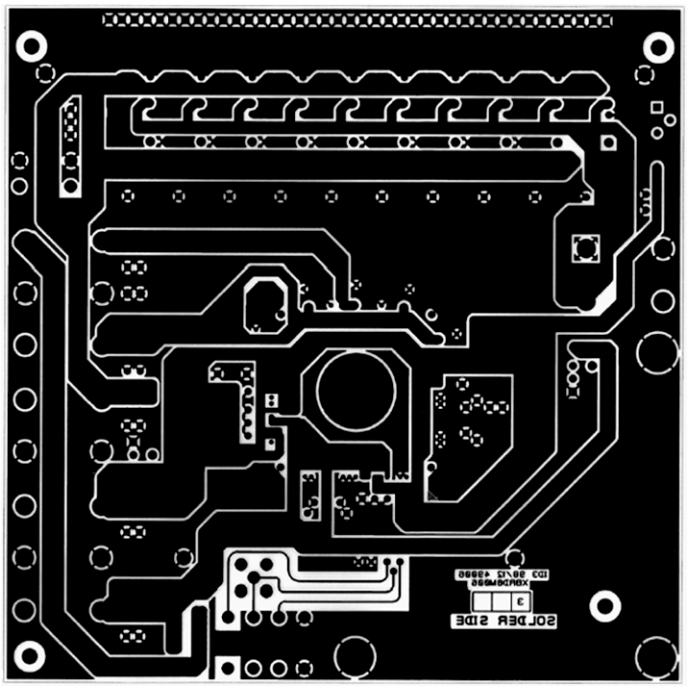
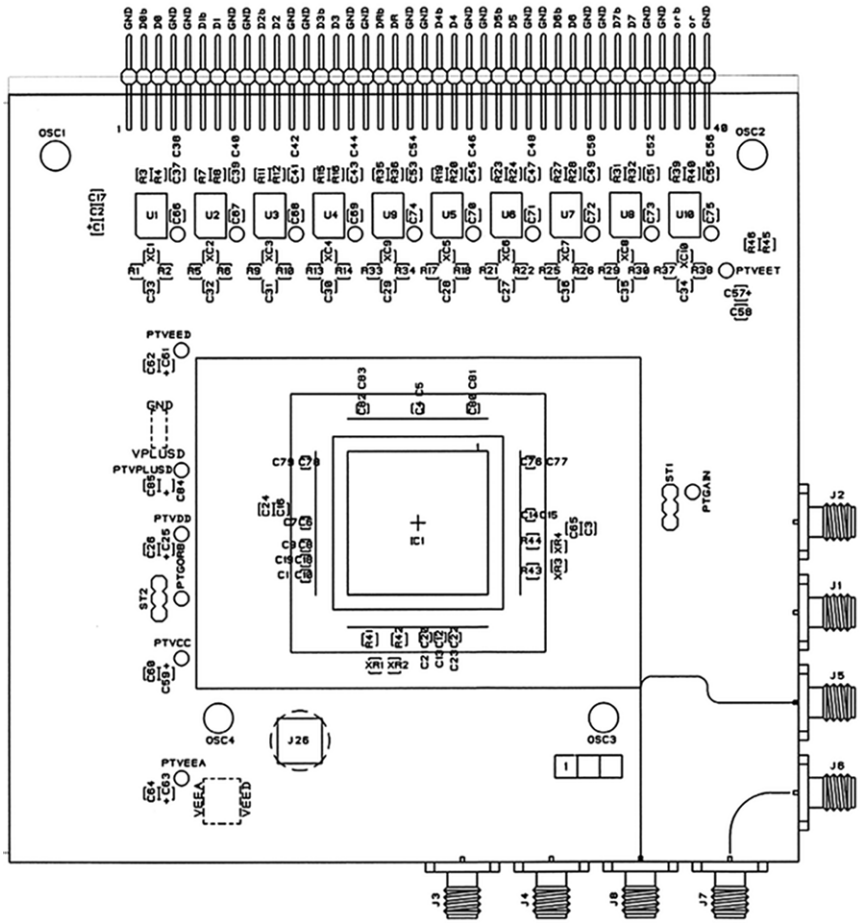


Figure 6-11. TSEV8388B Evaluation Board: Component Placement



0973D–BDC–02/09

How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax: +49 (0) 8142 284547

mailto: enquiries-de@e2v.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline-bdc@e2v.com