

Application Note

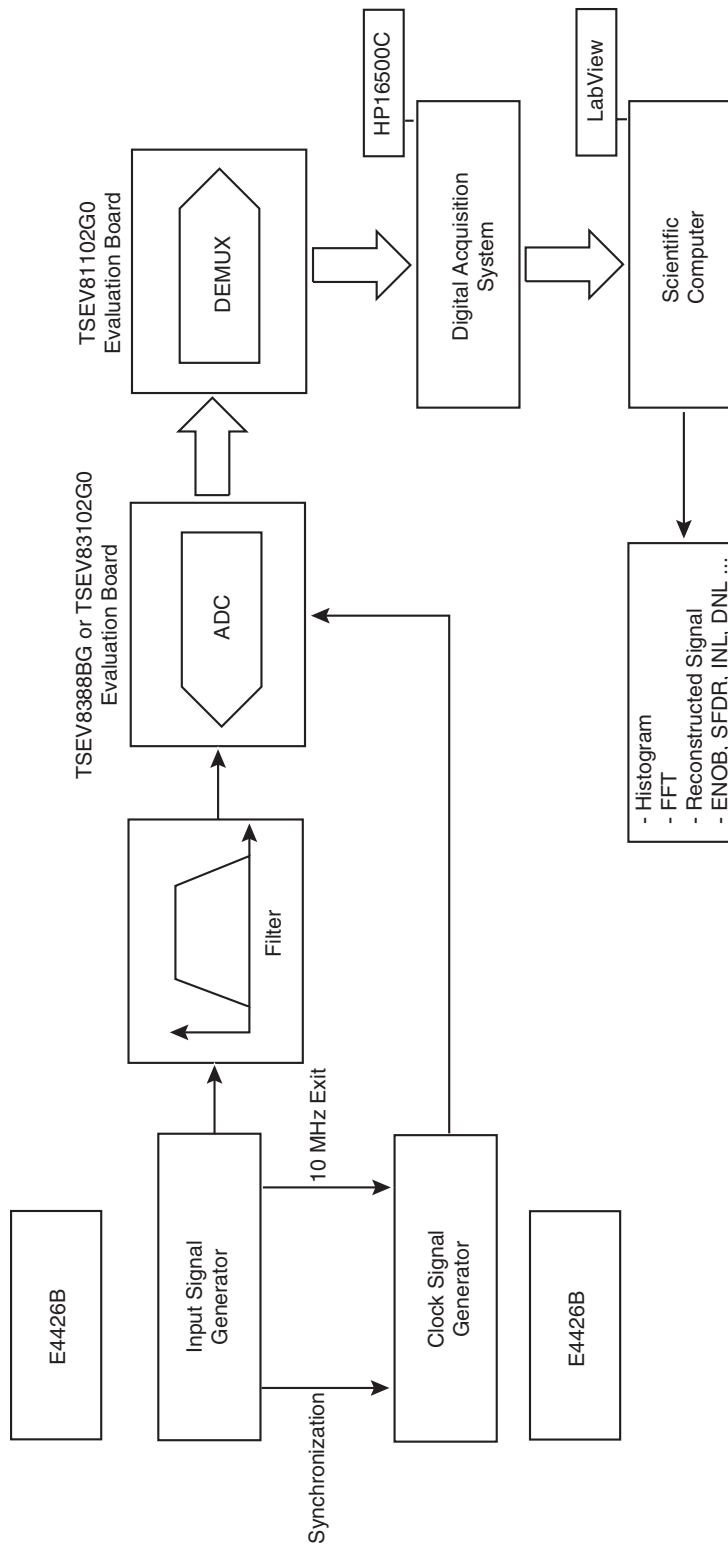
Getting Started with the TS8388B 8-bit 1 Gbps ADC and the TS81102G0 1:4/8 DMUX

1. Introduction

The aim of this application note is to help the user set up a test bench using e2v's TS8388B 8-bit 1 Gbps ADC and TS81102G0 1:4/8 DMUX evaluation boards. It first gives a description of the test bench used in e2v's laboratory, provides recommendations on how to connect all the components together and finally describes in detail the test procedure that should be followed to rapidly evaluate e2v broadband data conversion devices.

TS8388B and TS81102G0 Evaluation Boards

Figure 1-1. Test Bench



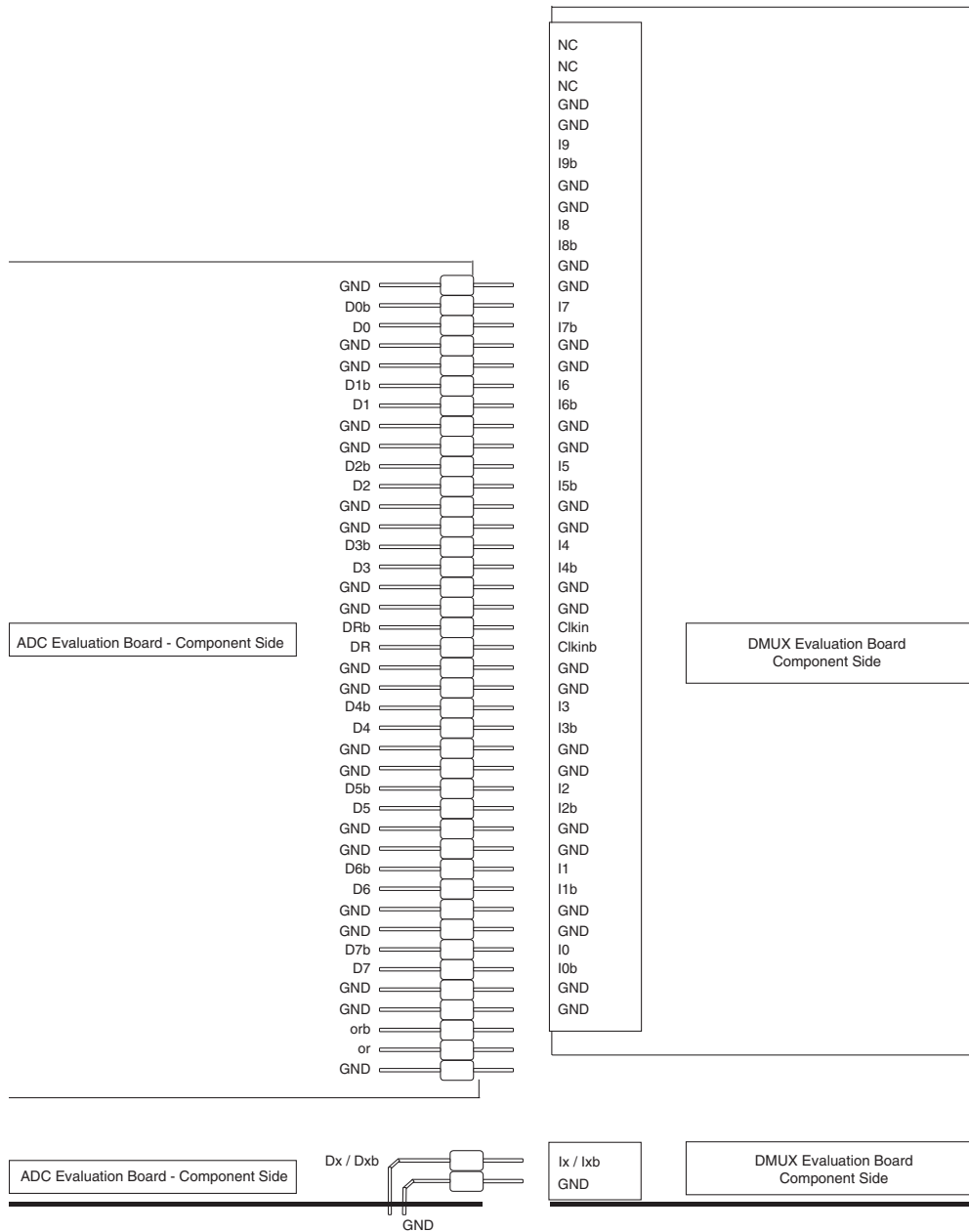
2. Interfacing the ADC and DMUX Evaluation Boards

2.1 Settings

In [Figure 2-1](#) and [Figure 2-2](#) on page 4, there is an offset between the ADC output connector and the DMUX input connector.

2.1.1 TSEV8388BF/FZA2 Evaluation Boards (ADC in CQFP Package)

Figure 2-1. Evaluation Boards (ADC in CQFP Package)

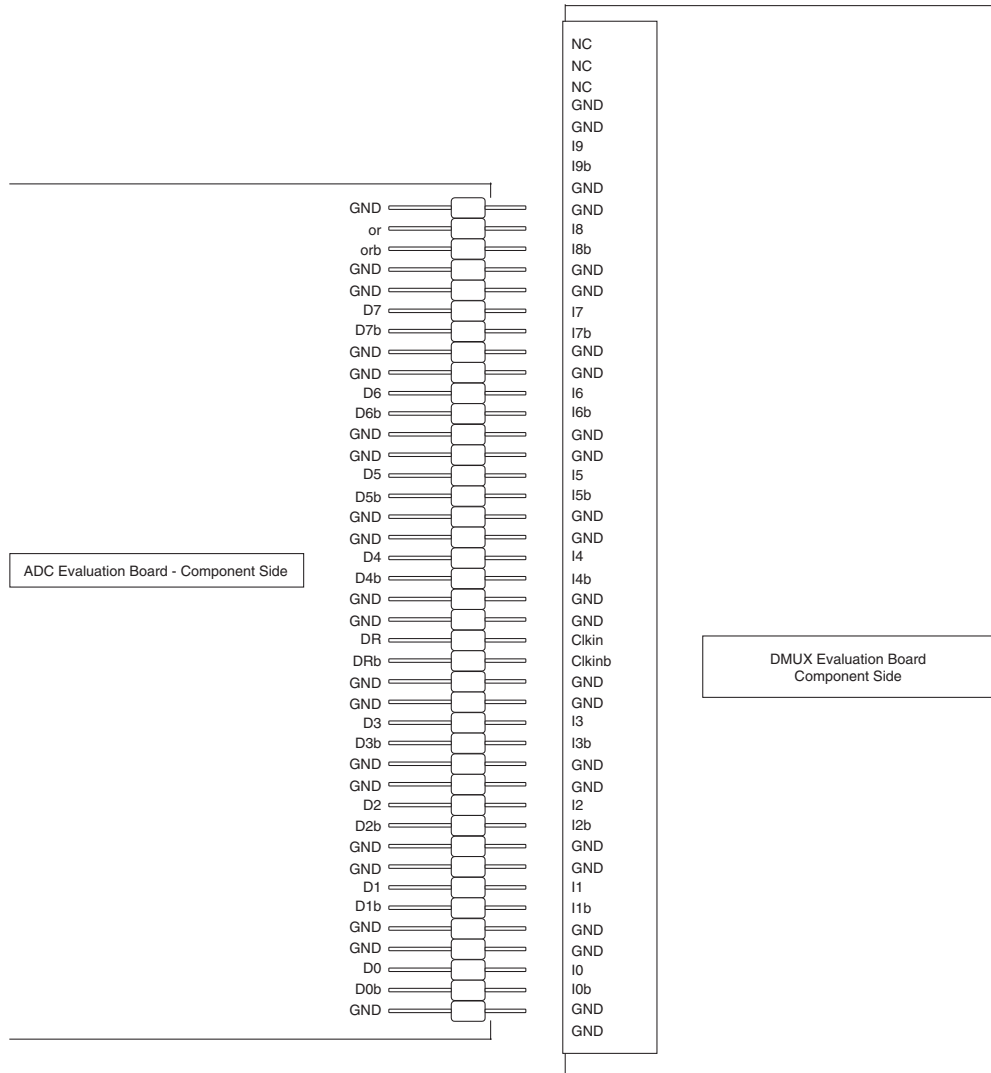


Note: In this configuration, the MSB on the DMUX is bit 0. Ensure the boards are connected as illustrated above, otherwise the ADC or the DMUX may be damaged by forcing a signal to ground, for example.

TS8388B and TS81102G0 Evaluation Boards

2.1.2 TSEV8388BGL/GLZA2 Evaluation Boards (ADC in CBGA Package)

Figure 2-2. Evaluation Boards (ADC in CBGA Package)



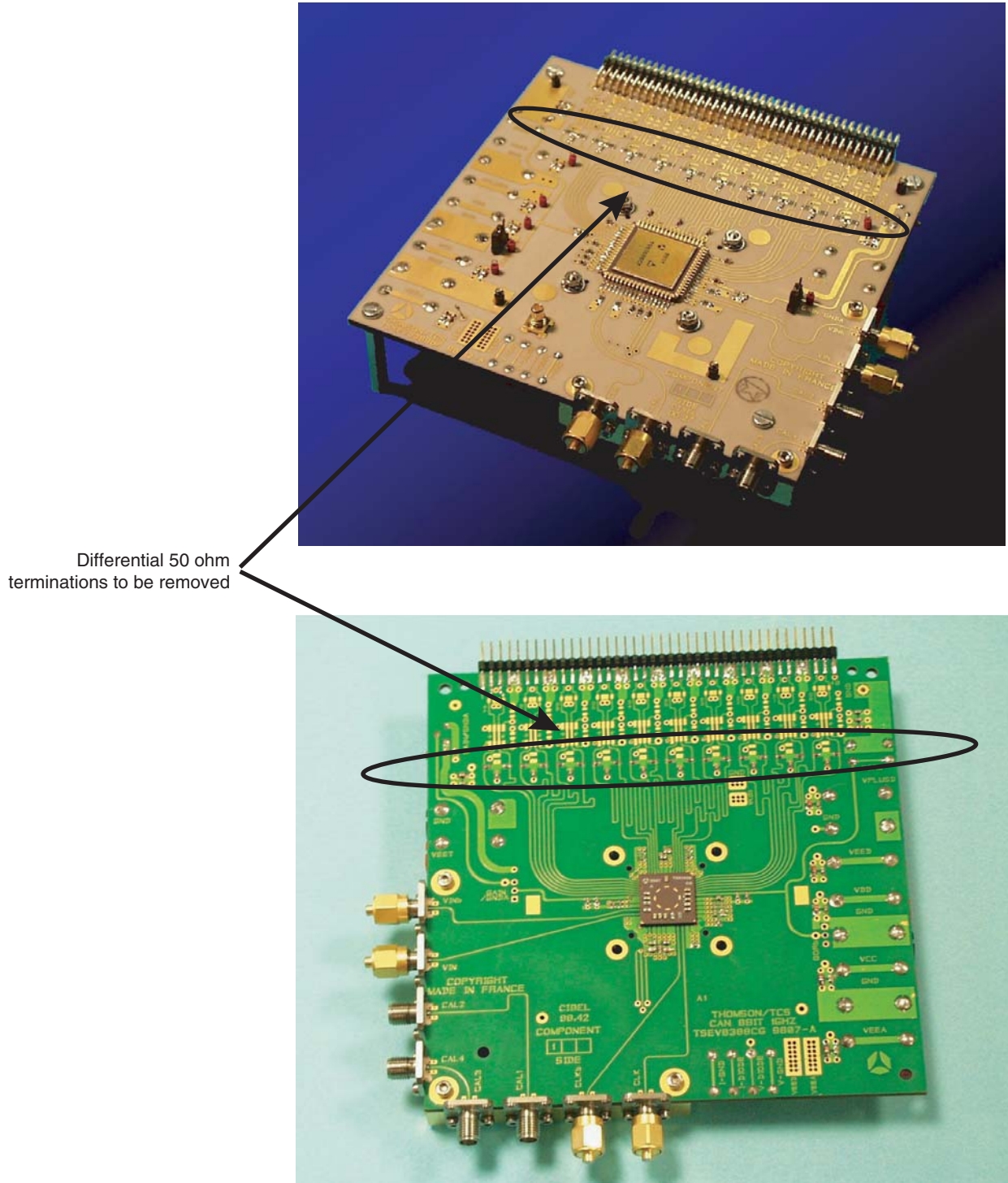
Note: Ensure the boards are connected as illustrated above, otherwise damage to the ADC or the DMUX can occur by forcing a signal to ground, for example.

TS8388B and TS81102G0 Evaluation Boards

2.1.3 TSEV8388BGL/F ADC Evaluation Boards without Digital Output Buffers

Since both the ADC data outputs are on-board 50Ω differentially terminated and the DMUX input buffers are on-chip 50Ω differentially terminated, it may be necessary to remove the extra termination at the ADC end when the ADC board is to be plugged to the DMUX board.

Figure 2-3. Boards without Digital Output Buffers



TS8388B and TS81102G0 Evaluation Boards

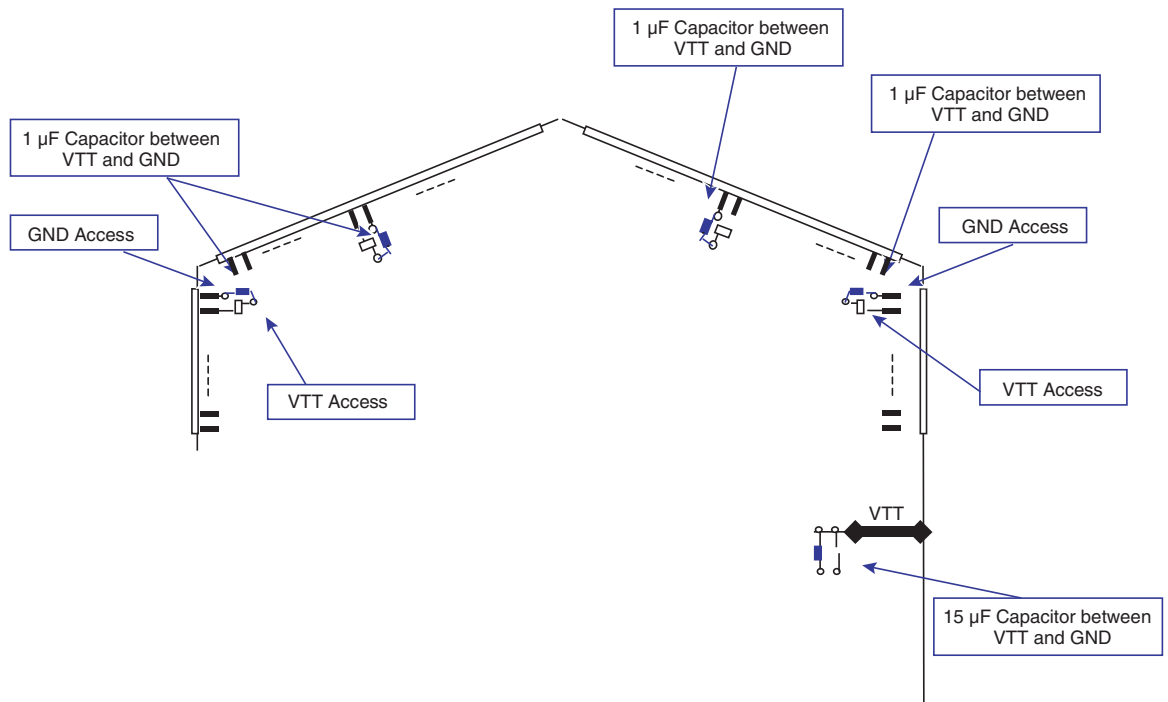
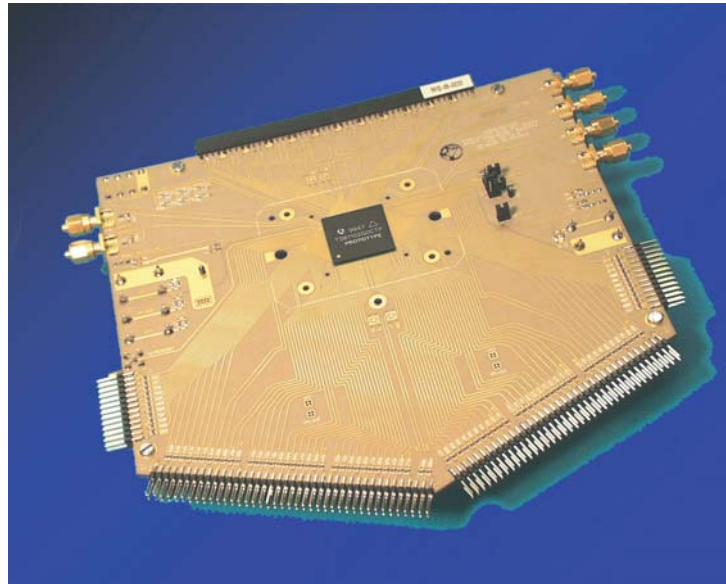
2.1.4 TSEV8388BGLZA2/FZA2 ADC Evaluation Boards with Digital Output Buffers

The ADC and DMUX boards can be connected directly to one another with no hardware modification required.

2.1.5 TSEV81102G0TPZR3 DMUX Evaluation Board

It may be necessary to add extra decoupling capacitors at the DMUX output between V_{TT} and ground: 4 capacitors of $1\ \mu\text{F}$ are recommended with 1 capacitor of $15\ \mu\text{F}$.

Figure 2-4. DMUX Evaluation Board



2.2 Other Settings

- DMUX jumpers⁽¹⁾
 - BIST: jumper OUT (BIST inactive)
 - NBBIT: jumper ON (8-bit)
 - CLKINTYPE: jumper ON (DR/2 mode)
 - RATIOSEL: jumper OUT (for 1:4 ratio)

- Power supplies

ADC

- $V_{EE} = D_{VEE}$ connected to $-5V$ supply
- V_{CC} connected to $5V$ supply
- V_{PLUSD} connected to ground
- V_{DD} connected to $-2V$ supply⁽²⁾
- V_{EET} connected to $-5V$ supply⁽²⁾

DMUX

V_{EE} connected to $-5V$ supply

V_{CC} connected to $5V$ supply

V_{TT} connected to $-2V$ in ECL mode

All grounds have to be connected together.

- Notes:
1. BIST jumper ON = BIST active
NBBIT jumper OUT = 10-bit
CLKINTYPE jumper OUT = DR mode
RATIOSEL jumper ON = 1:8 ratio
 2. The V_{DD} and V_{EET} power supplies have to be connected to $-2V$ and $-5V$ sources respectively only if the ADC board has the "ZA2" suffix ("with buffer" option).

3. Connecting the Logic Analyzer

Once the ADC and DMUX boards are connected and ready for operation, the last step before power up is to connect the logic analyzer probes to the DMUX outputs. It is recommended to have at least one of the DMUX ports fully connected to the logic analyzer in addition to the Data Ready signal from the DMUX, thus providing the synchronization clock for the logic analyzer.

4. Quick Start

4.1 Power Up Sequence

1. Apply the $D_{V_{EE}} = V_{EE} = -5V$ power supplies (on both ADC and DMUX)
2. Turn on the $V_{CC} = 5V$ power supply (on both ADC and DMUX)
3. If applicable (*with buffer* ADC board), supply V_{DD} and V_{EET}
4. Supply V_{TT}
5. All grounds have to be connected (as well as V_{PLUSD} directly to ground)
6. Apply the clock (0 dBm sinusoidal differential clock) and the analog input (-1 dBFS input level)
7. Perform an asynchronous reset on the DMUX

The devices should now operate properly. The next section describes the test procedure to be followed so that the whole system works correctly and optimum results are obtained.

5. Test Procedure

5.1 DMUX Output Levels Setting

This first step is mandatory to match the logic analyzer threshold to the DMUX output levels in both DC and dynamic conditions.

5.1.1 Static Adjustment

5.1.1.1 Configuration

ADC and DMUX ON, logic analyzer ON.

The clock and analog input signals are active at the ADC input (the frequency of both signals has no importance but one could choose $F_s = 1$ Gsps and F_{in} close to $F_s/2$ for optimum settings). Perform an asynchronous reset on the DMUX and then release it to make the system operational and re-activate the asynchronous reset to freeze the outputs at their level at reset.

Note: Always choose F_s and F_{in} so that $F_s/F_{in} = N/M$, where N = number of samples (2^n) and M = number of cycles (must be an odd number).

While the asynchronous reset of the DMUX is active (held high), with a voltmeter measure the VOL and VOH levels of all the output bits of the DMUX and the Vref level of all ports.

Vref should be close to $(VOL + VOH)/2$. In a typical case, Vref is lower than $(VOL + VOH)/2$.

The logic analyzer threshold has to be set to the value obtained with $(VOL+VOH)/2$.

- Notes:
1. The logic analyzer threshold is a very important parameter in a single-ended data acquisition. This is not the case when dealing with differential data acquisition (both Data and DataB are taken into account).
 2. It is necessary to calibrate the logic analyzer with all the probes connected prior to the first acquisition.
 3. Setting the threshold of the logic analyzer between $-1.4V$ and $-1.6V$ should satisfy the conditions for detection of the DMUX output data.

TS8388B and TS81102G0 Evaluation Boards

5.1.2 Dynamic Check

To make sure the previous value for the logic analyzer threshold is correct for both DC and dynamic domains, a dynamic test has to be performed.

1. From the last configuration, de-activate the asynchronous reset of the DMUX (the data should then run at the DMUX output).
2. With $F_s = 1$ Gsps and F_{in} close to $F_s/2$ (~ 500 MHz in Nyquist conditions), measure the VOL and VOH with an oscilloscope (eye diagram). The Vref value can also be checked with a voltmeter.
3. The obtained VOL, VOH and Vref values should be close to the ones found during the previous test. If not, we recommend you re-check the connection between the ADC and the DMUX boards:
 - Is the data from the ADC properly sent to the DMUX?
 - Perform another asynchronous reset on the DMUX and see what happens.
 - Tune the DMUX swing adjust.
4. If you still cannot identify the source of your problem:
 - Check the entire system again.
 - Take down all your test conditions.

Finally, contact the hotline at hotline-bdc@e2v.com for support.

5. If the output swing ($VOH - VOL$) is too low for the logic analyzer to detect the DMUX outputs, then the DMUX swing adjust should be used. By tuning the swing adjust, you should be able to obtain satisfying values for VOL, VOH and Vref.

Note: The nominal setting for the swing adjust (SWIADJ = 0V) of the DMUX should be suitable for a standard HP logic analyzer.

5.2 DMUX Delay Adjust

Once you are sure that the logic analyzer effectively detects the DMUX outputs, the next adjustment is the delay adjust of the DMUX (DMUXDelAdj).

1. Using the same configuration as previously described ($F_s = 1$ Gsps and F_{in} close to $F_s/2$), one can find the right DMUX delay to perform optimum synchronization between the ADC and the DMUX.

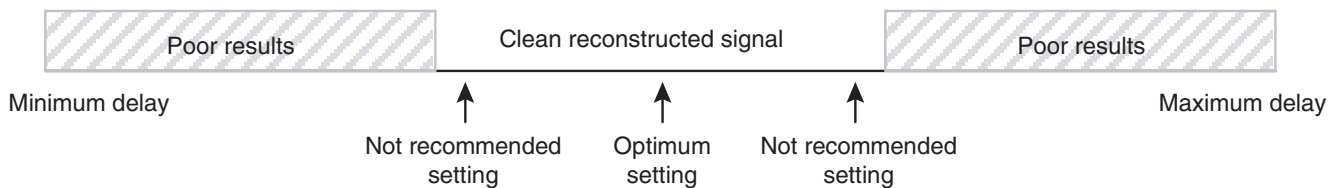
For this setting, special care has to be taken with the sampling and input frequencies. In fact, the adjustment on the DMUX delay adjust depends on the sampling frequency. It is not dependent on the input frequency, but the optimum setting for a given sampling frequency is achieved when the Nyquist condition is met, where $F_{in} = F_s/2$.

2. To find the right adjustment between the DMUX and ADC, it is recommended to cover the entire DMUX delay adjust range and check the reconstructed signal obtained for each delay.

The optimum delay is the one which corresponds to a clean reconstructed signal with no glitch (it is possible that a whole range of delays is satisfactory).

In addition, as illustrated in [Figure 5-1 on page 10](#), you should not choose a delay too close to an adjustment where the ADC gives poor results.

Figure 5-1. DMUX Delay Adjust

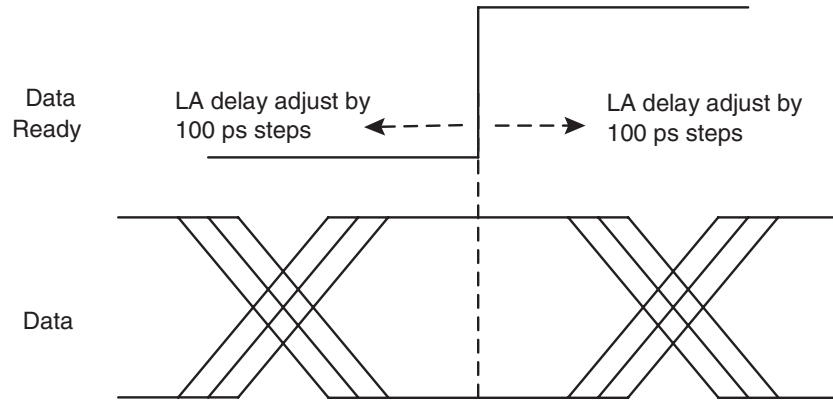


5.3 Logic Analyzer Delay Adjust

If the results are still not satisfactory (glitches on the reconstructed signal), the last adjustment to make is the logic analyzer delay.

1. By means of an oscilloscope, the eye diagram with the data and the Data Ready signal should be observed. In theory, the Data Ready signal should be right in the middle of the data but a small amount of skew may have made it shift to the right or left.
2. Fine tuning the logic analyzer delay may then be necessary to prop up the Data Ready signal in the middle of the data.

Figure 5-2. Logic Analyzer Delay Adjust



We then recommend you proceed as follows:

3. First, by 500 ps steps, change the logic analyzer delay to approximately find the *good* and *bad* zones (this is where the reconstructed signal shows many glitches)
4. Second, by 100 ps steps, fine-tune the logic analyzer delay until the reconstructed signal has no glitch and until the test gives satisfying dynamic results.

Typical results you should obtain are:

At $F_s = 1$ Gsps $F_{in} = 500$ MHz (-1 dBFS input level)

SFDR = -52 dBc

THD = -50 dB

SNR = 44 dB

ENOB = 7.0 bits

If you still do not obtain the expected results for the ADC, please contact the hotline for specific technical support at hotline-bdc@e2v.com



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