ADC and DMUX
TS830500, TS8388B, TS83102G0B ADCs and TS81102G0 DMUX

Application Note

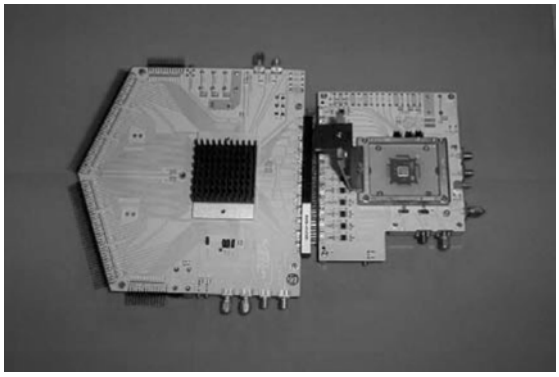
Applying e2v ADC and DMUX

1. Introduction

This document aims at presenting relevant information needed to properly apply the e2v ADCs and DMUX.

It describes the different configurations the product can be set at for best performance results.

An important benefit is the full compatibility of the e2v ADCs and DMUX devices and their evaluation boards. In particular, this document offers some tips to help the users apply our products in a very user-friendly way.



TSEV81102G0TPZR3 DMUX and
TSEV83102G0BGL ADC Evaluation Boards

Visit our website: www.e2v.com
for the latest version of the datasheet

2. ADC and DMUX Connection

2.1 ADC and DMUX Level Compatibility

The TS8308500 8-bit 500 Msps ADC, TS8388B 8-bit 1 Gsps ADC and TS83102G0B 10-bit 2 Gsps ADC data outputs are ECL/LVDS compatible. As the DMUX can only accept ECL levels at its inputs, the ADCs have to be set in ECL output mode (V_{PLUSD} to ground for the TS8308500 and TS8388B devices and at –0.8V for the TS83102G0B).

In the particular case of the TS83102G0B device (10-bit 2 Gsps ADC), V_{PLUSD} can be connected to ground and still make the output levels of the ADC compatible with the input level requirements from the DMUX.

2.2 DMUX Settings

If connecting to one of the TS83xxx e2v ADCs, the DMUX has to be set in DR/2 clock mode (the Data Ready signal frequency out of the ADC is half the sampling frequency and thus half the data rate). The other settings on the DMUX depend on the required speed ratio and resolution:

- NBBIT: set to 0 for 8 bits and 1 for 10 bits
- RATIOSEL: set to 0 for 1:4 ratio and 1 for 1:8 ratio

Note: The DMUX output buffers are limited to 250 Msps. The choice of the speed ratio has to be made according to the required data rate out of the DMUX but also to this 250 Msps limitation.

2.3 ADC and DMUX Interfacing

Because the DMUX input buffers are already on-chip differentially 2 x 50Ω terminated, it is not necessary to add any termination resistor between the ADC and DMUX. Consequently, the ADC outputs can be directly sent to the DMUX (direct traces) as illustrated in Figure 2-1 and Figure 2-2.

Figure 2-1. TS8388B 8-bit 1 Gsps ADC and DMUX Interfacing

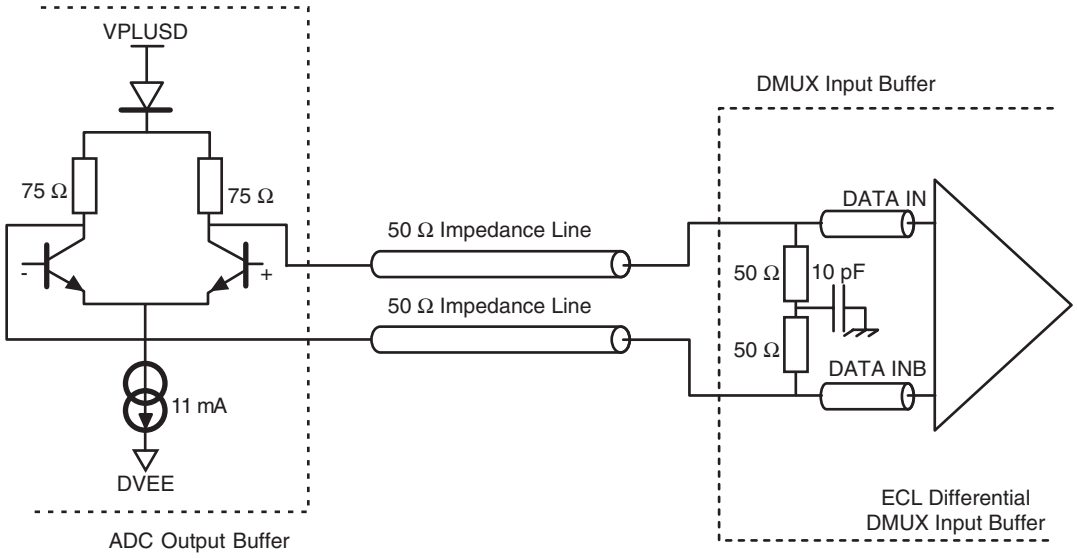
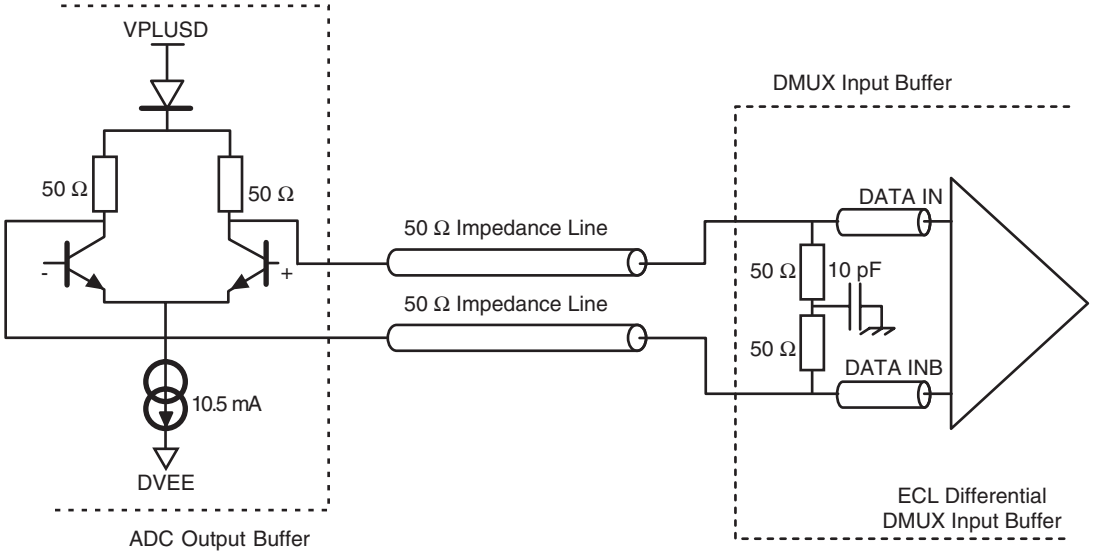


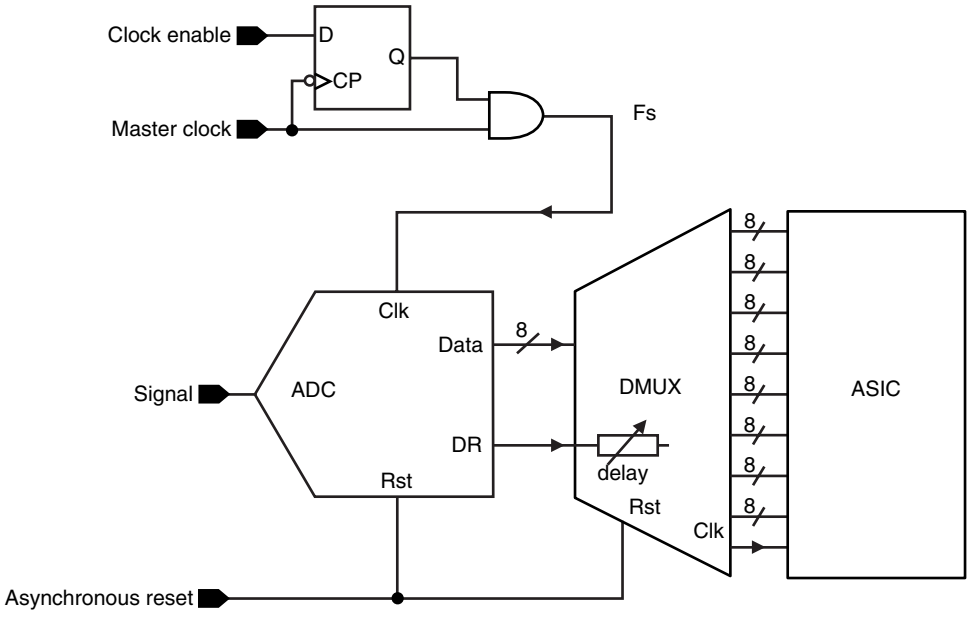
Figure 2-2. TS83102G0B 10-bit 2 Gsps ADC and DMUX Interfacing



Note: When connecting the ADC and DMUX evaluation boards, it is recommended to remove the extra 50 Ω termination resistors on the ADC board since the DMUX is already terminated. This does not apply for ADC boards with digital receivers, in which case the termination resistors are required for the digital receivers.

3. ADC and DMUX Mono-channel Application

Figure 3-1. ADC and DMUX Mono-channel Application



3.1 Aim

To constitute an acquisition channel with a high speed ADC, a DMUX and an ASIC.

The high speed ADC may be one of e2v family: TS8308500, TS8388B, TS83102G0B.

The DMUX is designed to slow down the output data frequency from the ADC, in order to allow the following ASIC to process calculations of this data at acceptable rates.

The whole system consisting of the ADC and the DMUX can be controlled via the asynchronous reset of the DMUX. This asynchronous reset is needed to start the DMUX and consequently can be used as the trigger for an acquisition.

Note: The Data Ready Reset DRRB of the ADC is not necessary for proper operation of the device.

The DMUX input clock phase can be adjusted with an adjustable delay of ±250 ps to ensure an adequate phase between clock and data inside the DMUX due to the DMUXDelAdjCtrl function of the DMUX device.

4. ADC and DMUX Interleaving Applications

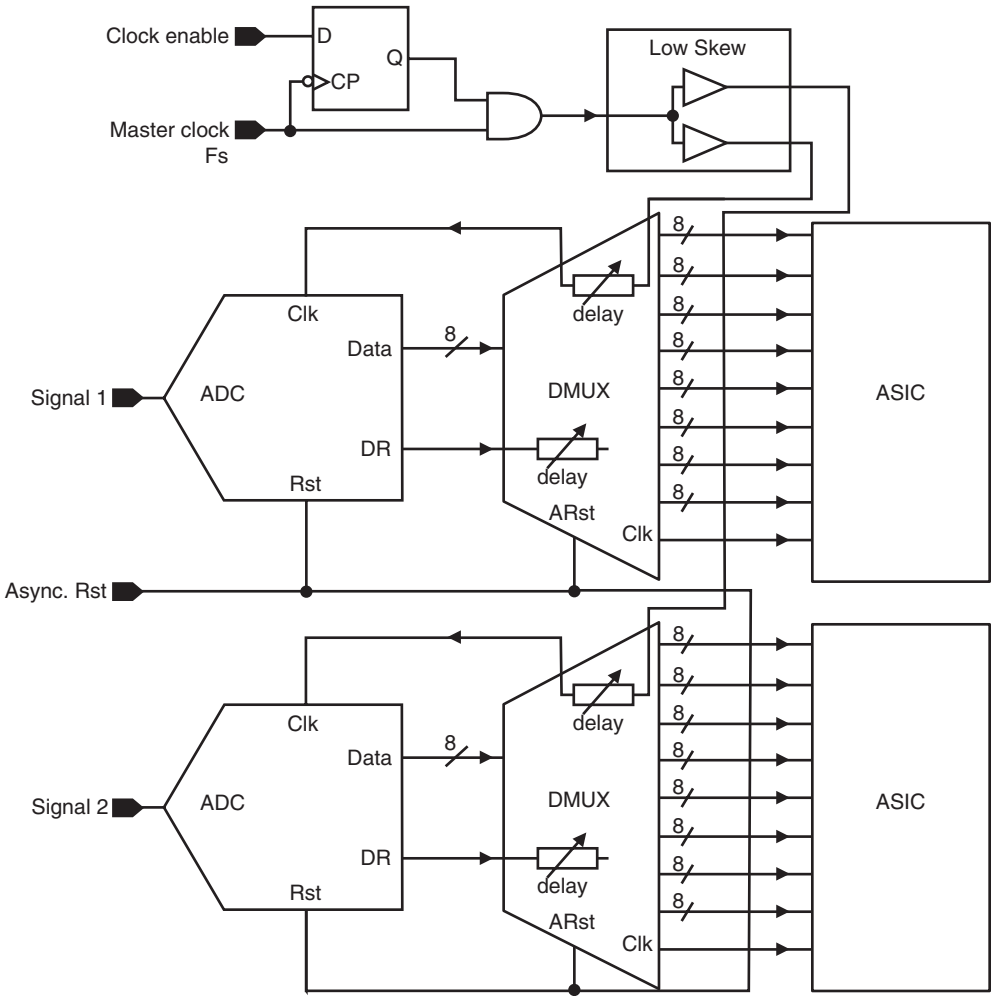
For several applications (multi-channel, multiplication of sampling frequency, multiplication of speed ratio), it is necessary to interleave 2 (or more) ADC and DMUX couples. In these cases, it is essential to align with more than 1 ps accuracy the internal sampling instant of the ADCs for correct HF performances.

In the case of the TS8388B ADC, a stand-alone delay adjustment (±250 ps) is available in the DMUX (ADC Delay Adjust).

When the TS83102G0 ADC is used, the internal sampling instant can be fine-tuned by the Sampling Delay adjust function of the ADC. In this case, it is not necessary to use the ADC delay adjust function in the DMUX.

4.1 Multi-channel Application

Figure 4-1. ADC and DMUX Multi-channel Application



4.2 Aim

To constitute multiple acquisition channels composed of a high speed ADC, a DMUX and an ASIC.

The state of each DMUX and each ADC is controlled with the asynchronous reset: the reset pulse is sent to all the devices.

For each channel, the DMUX input clock phase can be adjusted with an adjustable delay of ±250 ps to ensure an adequate phase between clock and data inside the DMUX thanks to the DMUX Delay Adjust function.

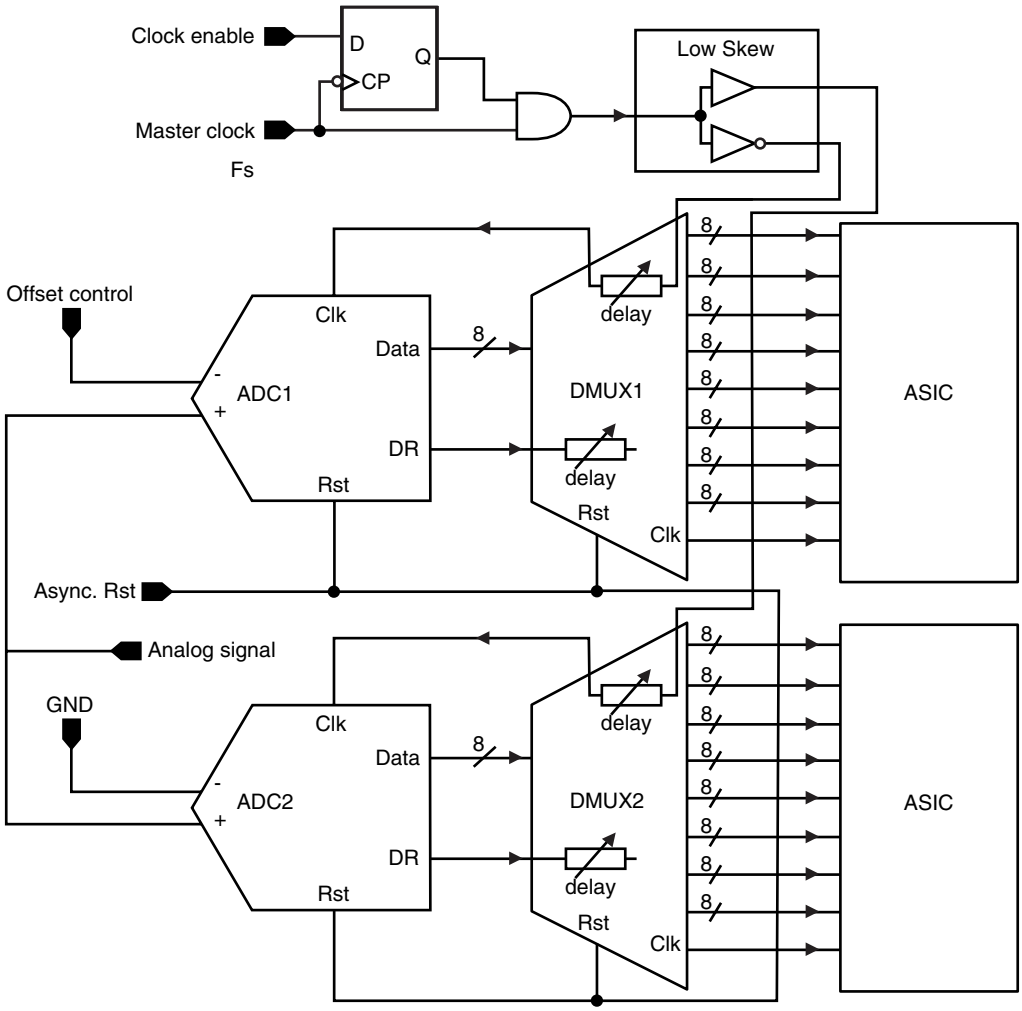
Note: It is recommended to use the synchronous reset of the DMUX to ensure good synchronization of both channels.

How to align the internal sampling instant of the ADCs:

1. Connect all the ADCs inputs (Refer to Figure 4-1 on page 5, Signal 1 = Signal 2).
2. Generate a signal on the ADCs inputs.
3. Check the ADC or DMUX outputs with an acquisition system.
4. Tune the delay adjust until the codes on the outputs are exactly the same for all the channels.

4.3 Multiplication of Sampling Frequency

Figure 4-2. Multiplication of Sampling Frequency



4.4 Aim

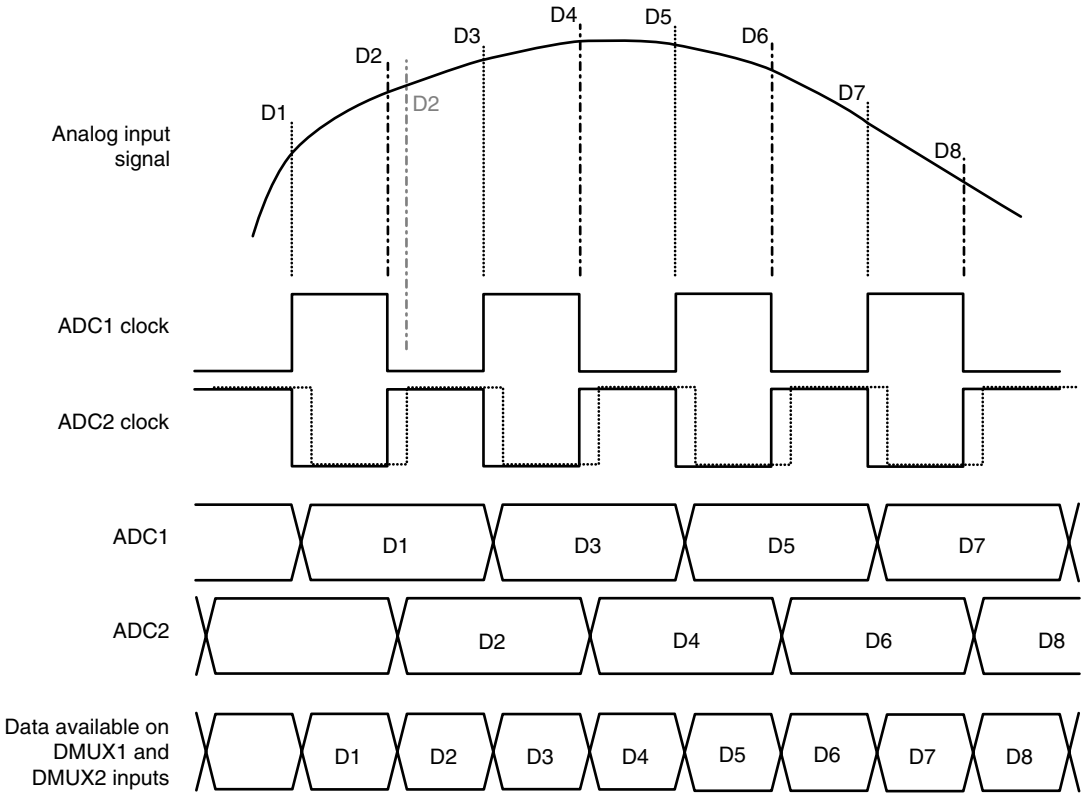
To multiply artificially the sampling frequency of 1 acquisition channel by using several ADC and DMUX couples.

The state of each DMUX and each ADC is controlled with the asynchronous reset: the reset pulse is sent to all the devices.

For each couple, the DMUX input clock phase can be adjusted with an adjustable delay of ±250 ps to ensure a good phase between clock and data inside the DMUX (DMUX Delay Adjust).

In this application, it is very important to align the internal sampling of the ADCs for proper operation of the interleaving scheme.

Figure 4-3. Timing Diagram



Note: These timing diagrams do not take into account the different propagation delays in the ADCs (pipeline delays for example).

In this application, the data available on the DMUX inputs are as if the sampling frequency was 2 x Fs instead of Fs. Practically, it is recommended to limit the number of channels for such an application to 4, so that the sampling frequency can be 4 x Fs.

The shaded gray in Figure 4-3 is an example of bad alignment of the sampling of the ADCs. It is obvious that the data D2 will be different from the data expected in the case of sampling frequency of 2 x Fs.

How to align the internal sampling instant of the ADCs:

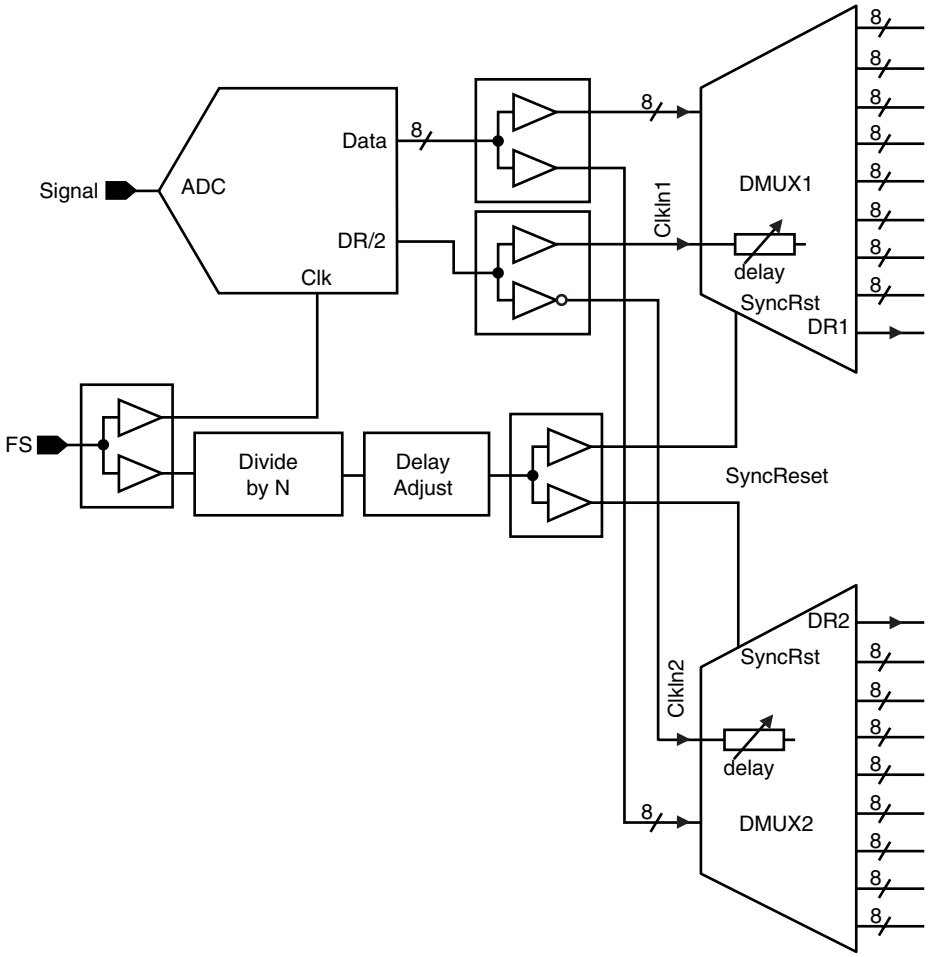
1. Provide the Master Clock with a low frequency signal (typically 100 Msps).
2. Connect the ADCs positive input to a common analog sinewave signal of frequency twice the frequency of the Master Clock (typically 50 MHz).
3. Tune the sampling instant of one of the two ADCs until the codes at the two ADCs outputs are the same.

5. 1:16 Conversion Ratio

This 1:16 conversion ratio is achieved using two DMUXs in parallel.

5.1 Multi-channel Application

Figure 5-1. 1:16 Conversion Ratio



5.2 Aim

To reduce the data speed out of the ADC and DMUX couple from Fs/8 to Fs/16.

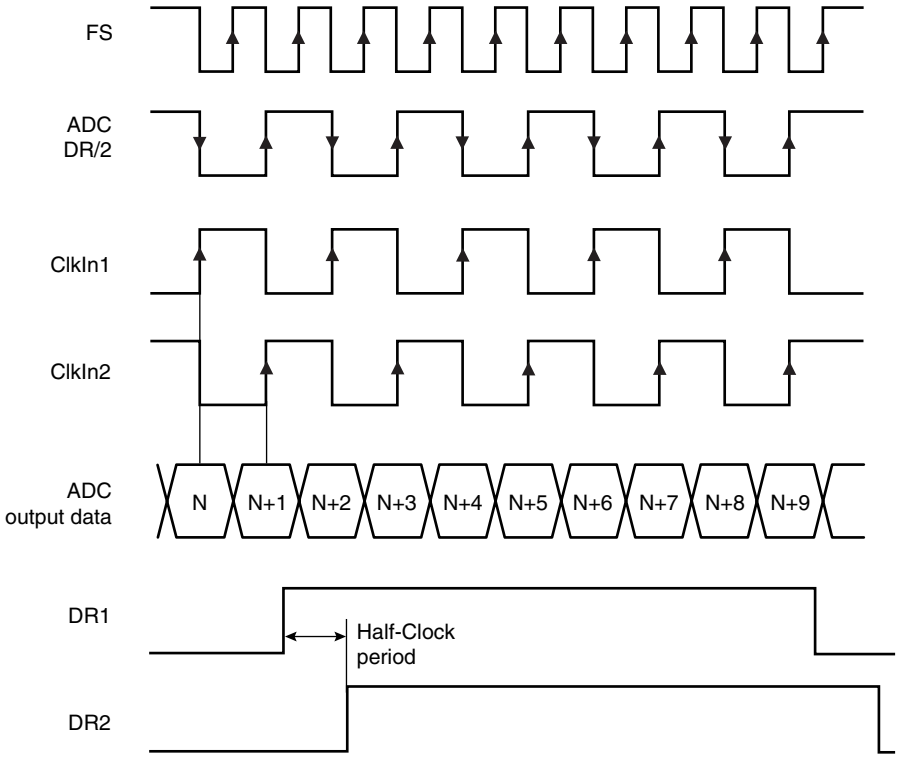
To obtain 1:16 ratio, the ADC must provide a DR/2 clock, and each DMUX is configured to work in DR mode.

The DR/2 is wired to the clock input of each DMUX (ClkIn1 and ClkIn2), so that they work in opposite phase. Thus, odd data is read by the first DMUX on the rising edge of ClkIn1, and even data is read by the second DMUX on the rising edge of ClkIn2.

To ensure a good synchronization between the two DMUXes, it is advised to start both boards at the beginning by performing an asynchronous reset on both the DMUXes and then to send a common synchronous reset to the two boards simultaneously (if the synchronous reset is to be used as a single-ended signal, it is recommended to leave the negative synchronous reset signal floating).

As implied by Figure 5-1 on page 8, there is no need to use the DRRB reset from the e2v ADC. As a matter of fact, the DRRB reset signal from the ADC is not mandatory when the e2v ADCs are used with the e2v DMUX, since the state of the ADC and DMUX system can be controlled thanks to the DMUX asynchronous reset.

Figure 5-2. Timing Diagram



6. ADC and DMUX Power Up Sequence

The power up sequence for the ADC and DMUX system is described hereafter:

1. Supply V_{EE} = –5V
2. Supply V_{CC} = +5V
3. Supply V_{PLUSD} if needed
4. Supply V_{TT} if needed
5. Apply the clock and the analog inputs on the ADC
6. Perform an Asynchronous reset on the DMUX

The first four steps of this sequence are not critical but it is recommended not to have the +5V supply on while the –5V is off for too long a time.

On the other hand, the last two steps are mandatory in the specified order (do not apply the clock and analog input signals to the ADC while the supplies are Off).

The Asynchronous Reset of the DMUX is then required to start the DMUX device.

7. PCB Ground Planes

Concerning the ground planes on ADC and DMUX boards, we recommend the configuration used in our ADC and DMUX evaluation boards (TSEV8388, TSEV83102G0 and TSEV81102G0) as being the same ground plane for both analog and digital parts.

You will find in the datasheets:

- The board layers characteristics on *Board Layers Thickness Profile* for all the evaluation boards
- The board metal layers schematics on *Electrical Schematics* of TSEV83102G0
- The board metal layers schematics on *Electrical Schematics* of TSEV8388
- The board metal layers schematics *Evaluation Board Schematics* of TSEV81102G0

7.1 ADC Boards

The ADC boards are constituted of several ground planes, some of which are identical and were duplicated for board rigidity.

We can consider that there is one main ground plane, being both an analog ground plane and digital ground plane.

One common plane is used for both analog and digital grounds:

- The ADC digital output buffers are differential buffers so there is no significant transient current in the power planes, even if several buffers switch at the same time.
- The other parasitics which may perturb the ground plane are due to the poor adaptation of the digital output buffers. This may cause reflections and perturb the digital ground plane. But this situation can not ensure a correct transmission of the output signals. If the digital output signals are perturbed, the load acquisition will be ineffective. With a good adaptation of the output buffers, this can be avoided.

Consequently, because of the use of well-adapted differential output buffers, the choice was made to merge the analog and digital ground planes.

7.2 DMUX Boards

There is one reference plane (divided in V+D and GND planes) and there is one power supply plane.

V+D and ground planes are separated because:

- The DMUX digital output buffers are single ended buffers and consequently, when several output buffers switch simultaneously, large transients can be created in the V+D plane. As V+D and ground planes are separated, V+D plane does not corrupt significantly the ground plane.
- V+D and ground planes are on the same layer and not stacked, that allows to avoid the corruption of the ground plane by V+D plane through the coupling capacitances.
- As for the ADC board, there are also the issues of bad adaptations on the load which can corrupt the V+D plane. Moreover this involves a bad quality of the signals for the load acquisition.

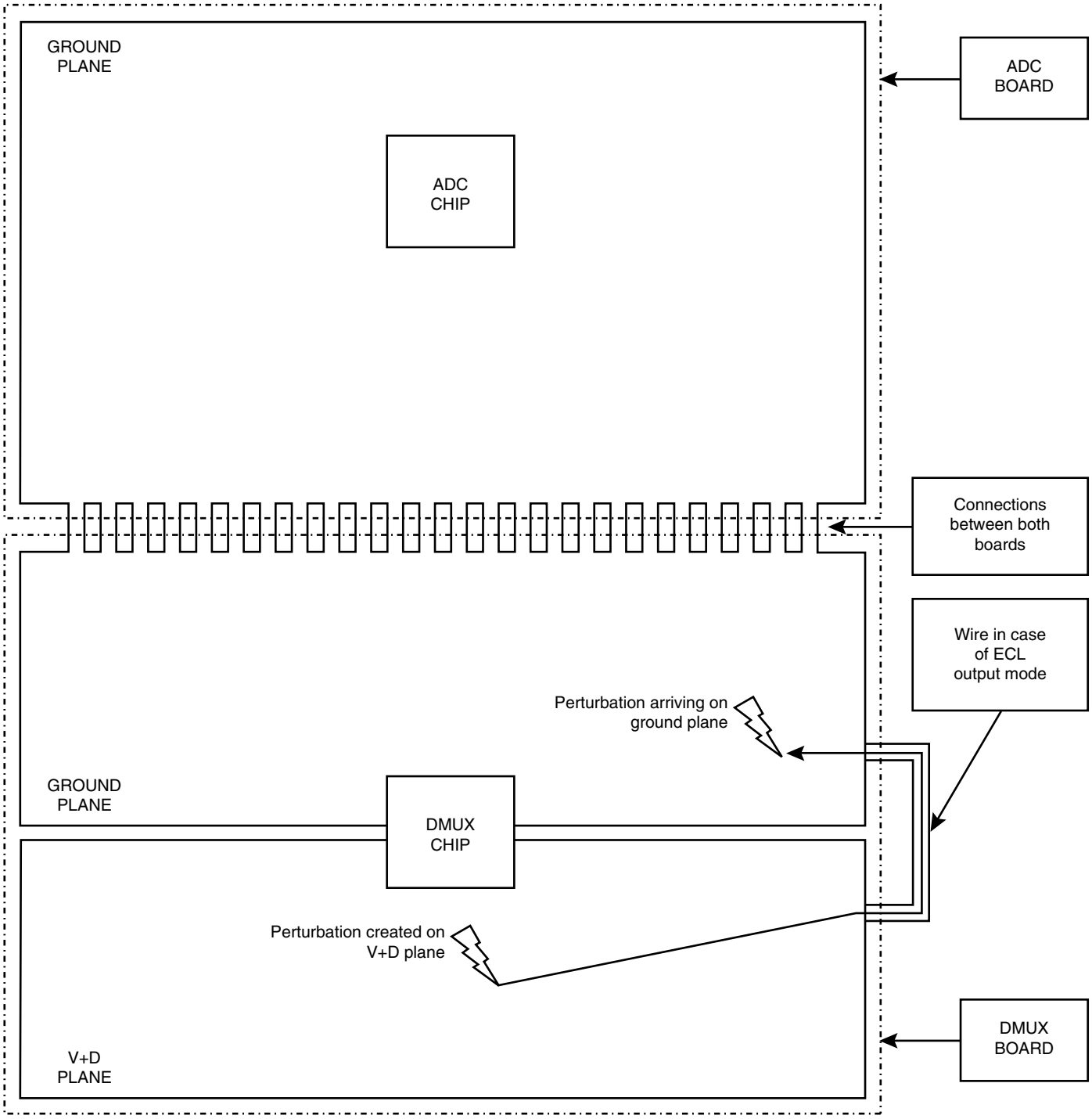
In the case of ECL output mode, V+D is connected to the ground by one wire, which allows the current to flow (see Figure 7-1 on page 11).

Moreover this imposes on the perturbation to cover a big distance (several centimeters) before reaching the ground plane. As the planes have a very low impedance, the perturbation is quickly dissipated.

Note: V_{PLUSD} power supply has to be decoupled to V_{EE} and not to ground.

Finally, Figure 7-1 represents the ADC and DMUX boards, which can work at a frequency of up to 2 GHz (providing a good matching of the DMUX load).

Figure 7-1. ADC and DMUX Boards Schematic



8. ADC and DMUX Board Layout Recommendations

8.1 Board's Layer Profile

It is recommended to use HTG dielectric layers because of their very good high frequency performances.

The number of layers can be calculated as follows:

(1 copper layer + 1 reference plane + 2 dielectric layers) x Number of signals to be separated (min = 3).

8.2 I/O Transmission Lines

For proper matching and transmission of high frequency signals, 50 Ω microstrip lines should be used.

Particular care should be taken with regards to the line length of similar signals: it should be the same with less than 2 mm accuracy for high-speed signals.

8.3 Power Supplies

For proper operation of the device and good shielding versus noise, it is recommended to uncouple the power supplies of the ADC and DMUX at the 10 nF and 100 pF SMC capacitors in parallel (to be superimposed on one another).

In the case of the DMUX, at least 30 x (10 nF + 100 pF) capacitors are necessary for all the power supplies.

Note: 39 x (10 nF + 100 pF) capacitors are used on the evaluation board.

When all 80 output data of the DMUX are to be used, it may be necessary to extra decouple the V_{TT} power supply thanks to 4 additional 1 µF tantalum capacitors and 1 additional 15 µF capacitor.

In the case of the TS8388B 8-bit 1 Gsps ADC, at least 11 x (10 nF + 100 pF) decoupling capacitors are necessary.

Note: 24 x 10 nF + 16 x 100 pF capacitors are used on the evaluation board.

9. Appendix

9.1 Appendix 1: TS81102G0 DMUX, TS8388B ADS and TS83102G0B ADC Block Diagrams

Figure 9-1. TS81102G0 DMUX Block Diagram

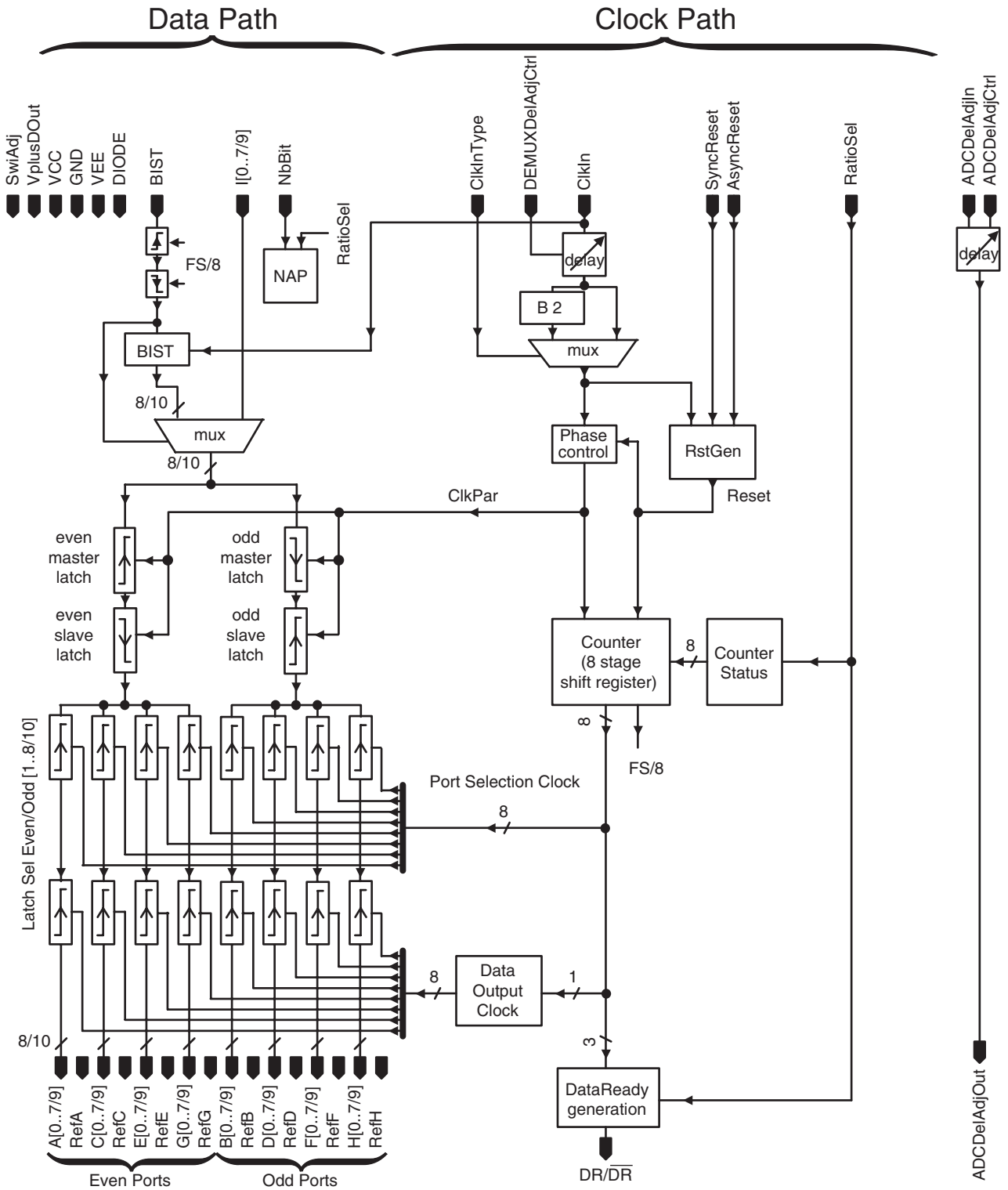


Figure 9-2. TS8388B ADC Block Diagram

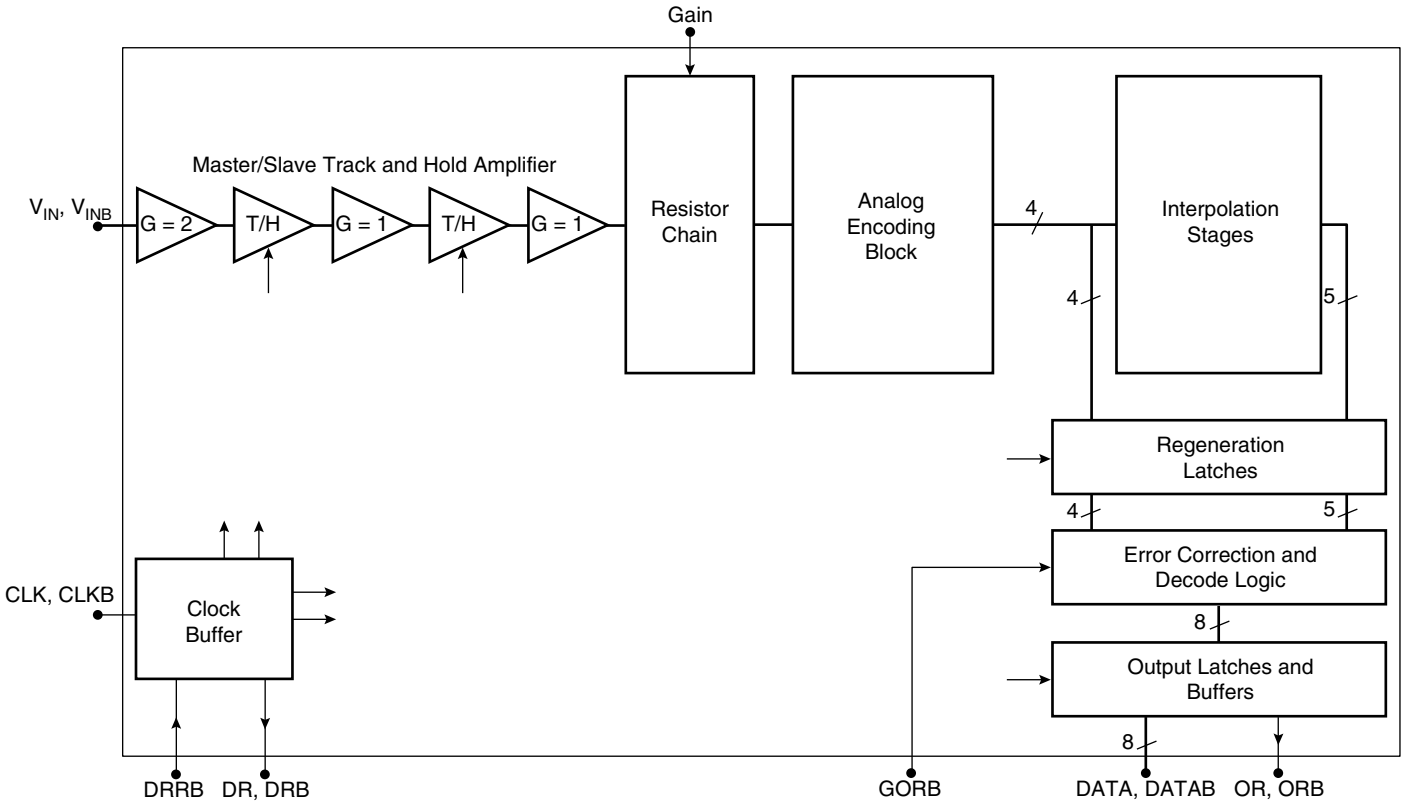
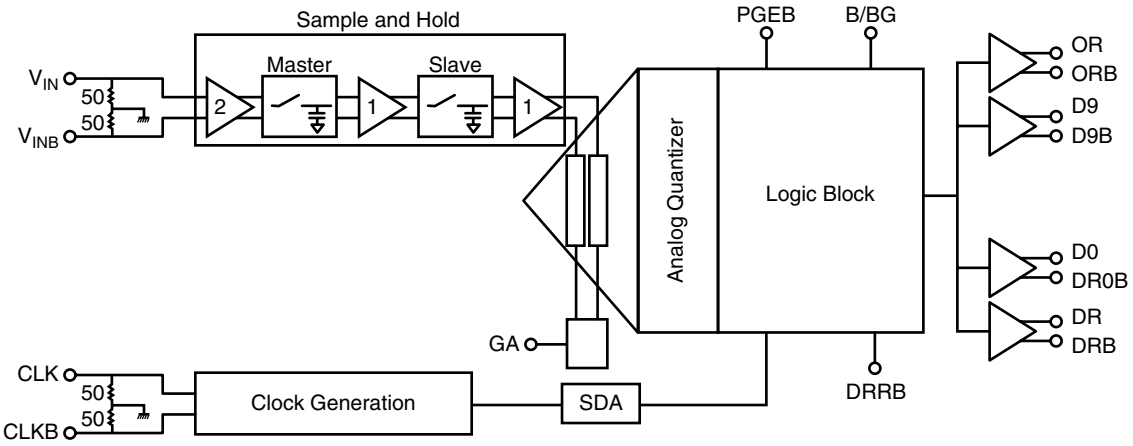


Figure 9-3. TS83102G0B ADC Block Diagram

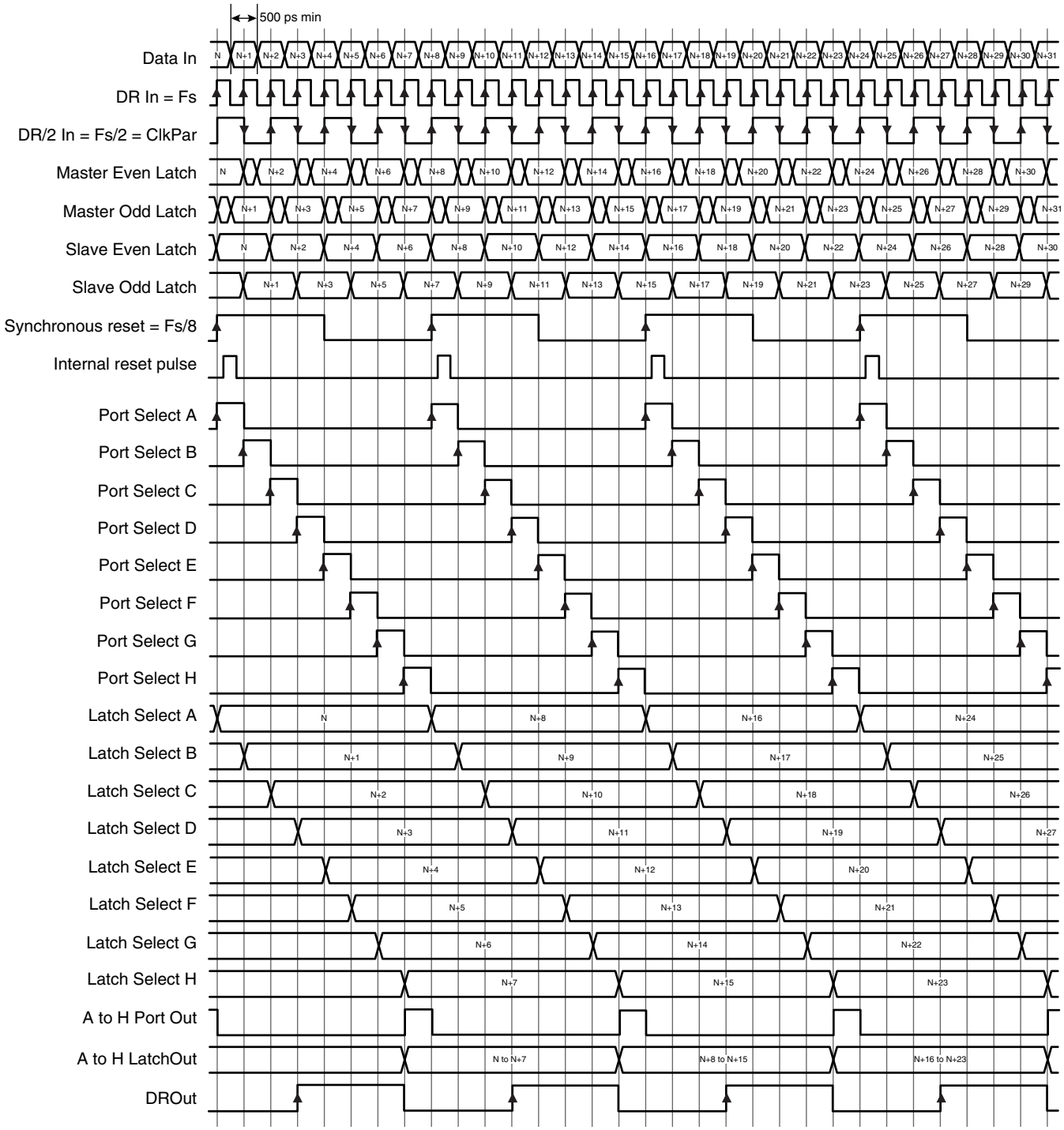


9.2 Appendix 2: Internal Timing Diagram

9.2.1 DMUX Timing Diagram

This diagram corresponds to an established operation of the DMUX with Synchronous Reset.

Figure 9-4. DMUX Timing Diagram



9.2.2 ADCs Timing Diagrams

The timing diagrams for the TS8388B and TS83102G0 ADCs are similar. Care should only be taken regarding the values of the specified timings (refer to the corresponding device datasheet for more details).

Figure 9-5. Timing Diagram: Data Ready Reset, Clock Held at LOW Level

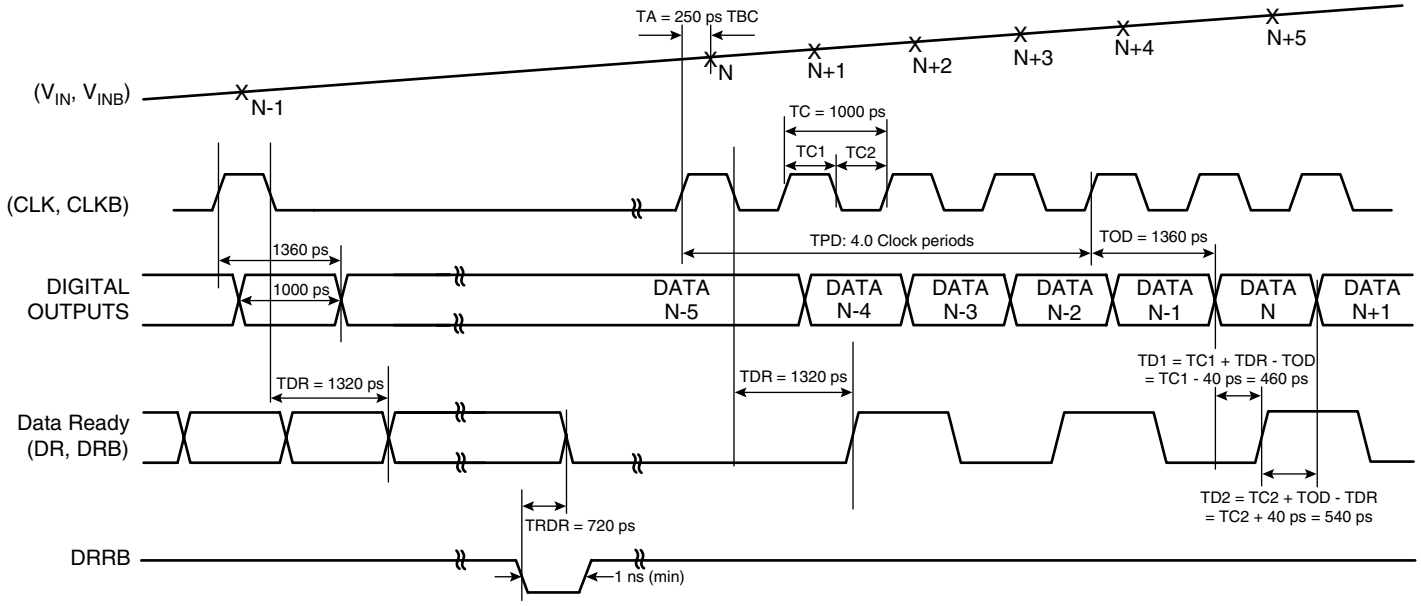
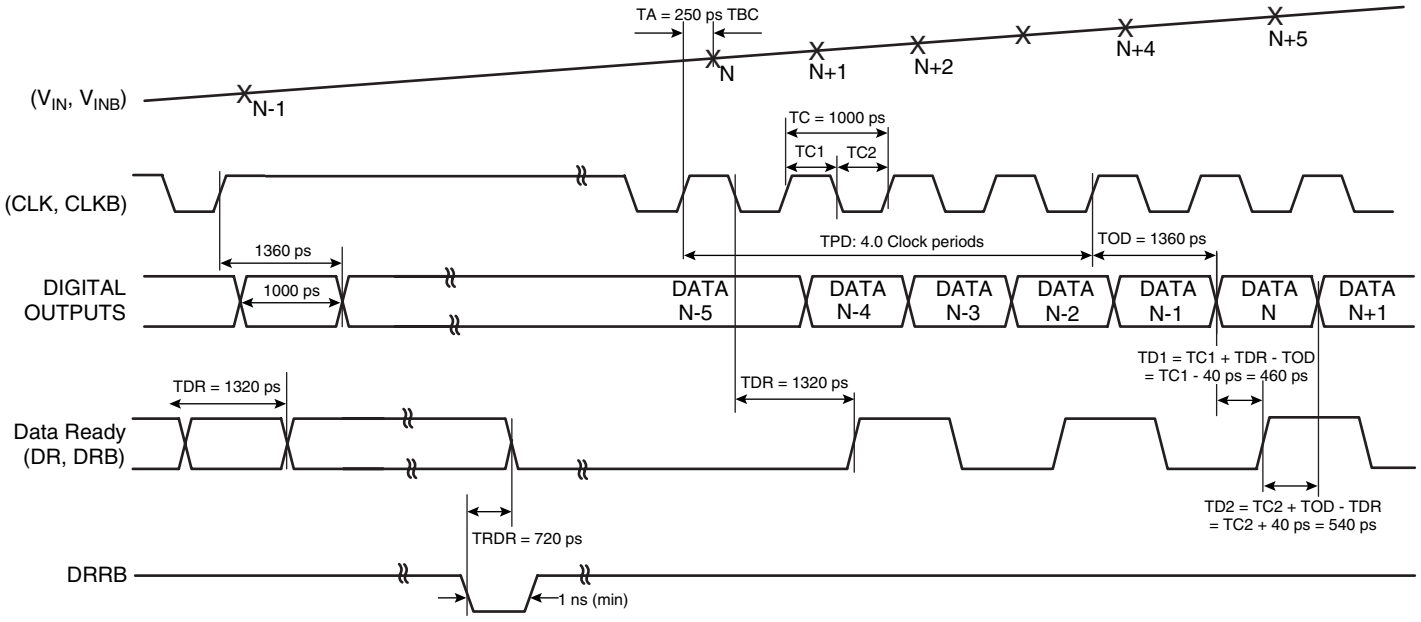
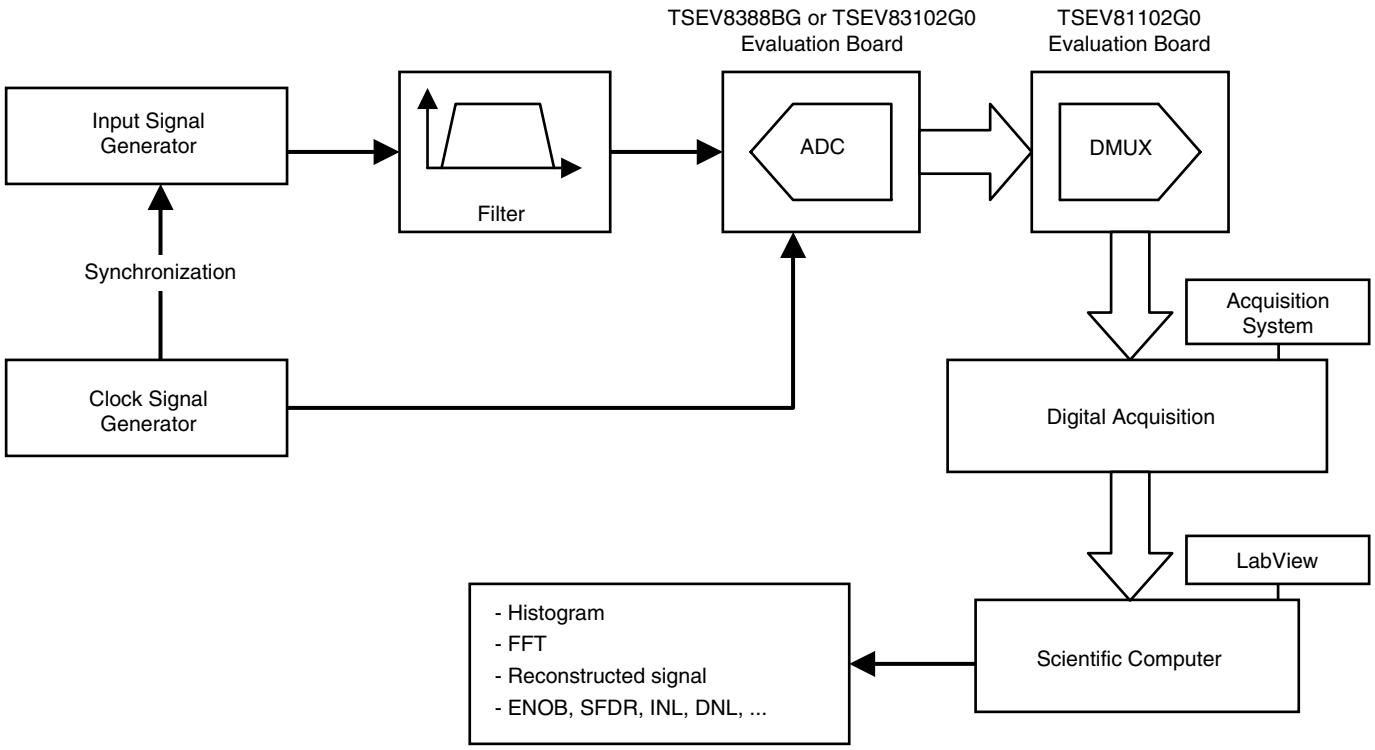


Figure 9-6. Timing Diagram: Data Ready Reset, Clock Held at HIGH Level



9.3 Appendix 3: ADC and DMUX Test Bench

Figure 9-7. Example of ADC and DMUX Test Bench



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