EV12AS350
Interpolation & Calibration

June 2017

Document aim and comment

This document aims at explaining the interpolation and the calibration procedure of the EV12AS350.

The information contained in this document should be used in addition to the datasheet of the EV12AS350.

Introduction

The interpolation and the calibration are two different processes on the EV12AS350. Both are related to the interleaving calibration of the 4 internal cores of the EV12AS350 allowing reaching 5.4GSps. And both improve the TILD (Total Interleaving Distortion) performance. There are three possibilities to calibrate the interleaving:

- Using the factory calibration stored within the ADC OTP (One Time Programmable fuse) either the one for ambient and hot temperature (optimum around Tj = 90°C) or the one for cold temperature (optimum around Tj = 50°C);
- Doing the interpolation versus temperature between these two sets of factory calibration;
- Doing a manual interleaving calibration for offset, gain and phase

In case the junction temperature is either close to 90°C or 50°C; the right factory calibration will offer similar performance than the interpolation. In case the junction temperature is not close, the interpolation method will offer an improvement on the interleaving performance. Finally, the manual calibration will always offer better interleaving performance as these depend from the sampling speed and the input signal. And these vary greatly from application to application which cannot be accounted for through the factory calibration. It should be noted that the manual calibration, if done, should be done in addition to the interpolation; using the interpolation value as a starting point for the process describe in the manual calibration section.
The implementation complexity goes up from using the factory calibration to doing the manual calibration and in most application, the interpolation solution would be sufficient while involving small extra effort to implement.

Summary

1. Loading the factory calibration

Two sets of calibration are stored during the factory testing of the device. The 1st set is for ambient and hot temperature (optimum around Tj = 90°C) and the 2nd one is for cold temperature (optimum around Tj = 50°C). The 1st set for ambient and hot temperature is loaded by default. When working around the conditions of temperature of set 1 or set 2, simply loading the corresponding factory calibration is sufficient to reach the performance of the datasheet. This is the easiest solution to implement when working with applications that have a small variation of temperature (+/- 15°C) close to the factory calibration temperature.

1.1. Necessary SPI instructions

To load the 1st set of calibration the following SPI operation should be done:

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x0000*	*#Selection of factory calibration*
WRITE	*@0x15 (CAL_SET_SEL)*	*0x0000*	*#Selection of factory calibration set 1 (hot and ambient)*

To load the 2nd set of calibration the following SPI operation should be done:

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x0000*	*#Selection of factory calibration*
WRITE	*@0x15 (CAL_SET_SEL)*	*0x0001*	*#Selection of factory calibration set 2 (cold)*

2. Implementing the interpolation

2.1. Process description

The interpolation objective is to adapt the calibration of the ADC to the temperature of its use. Two sets of factory calibration are written into the device OTP (One Time Programmable fuse) when it is tested. The 1st set of factory calibration is dedicated to ambient and hot temperature (optimum around Tj = 90°C) and the 2nd set to cold temperature (optimum around Tj = 50°C).
To realize the interpolation the following process should be done for each register listed in Table 1:

1. Read register value from 1st set of factory calibration (this value converted in base 10 is noted R_0 hereafter);
2. Read register value from the 2nd set of factory calibration (this value converted in base 10 is noted R1 hereafter);
3. Measure the temperature diode value in mV (this value in mV is noted V_d hereafter);
4. Apply the following formula: $R_{SPI} = \frac{R_0 - R_1}{787 - 830}(V_d - 830) + R_1$;
5. Convert R_{SPI} in binary and write it in the corresponding SPI register.

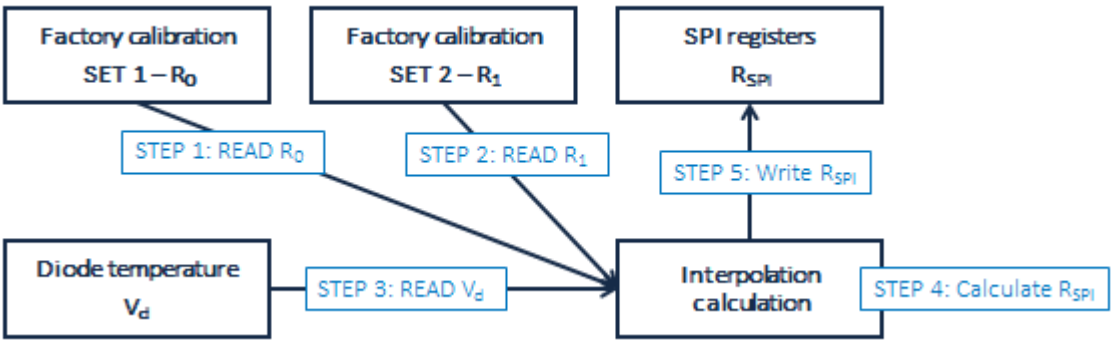


Figure 1: Interpolation process

NB: Example of implementation can be found in ANNEX A and ANNEX B at the end of this document

NB: Instead of doing the process explained in this section for each register one after the other; it is more time optimized to read all the register with the 1st set of factory calibration then all register with the 2nd set of factory calibration, then doing all the calculation and finally writing all the register back into the SPI.

Table 1: Register to interpolate

Register name	Register address	Register size	Comment
A_OFFSET_CAL	0x17	<8:0>	Master register
B_OFFSET_CAL	0x18	<8:0>	Master register
C_OFFSET_CAL	0x19	<8:0>	Master register
D_OFFSET_CAL	0x1A	<8:0>	Master register
CAL1	0x33	<6:0>	Channel register
CAL2	0x34	<6:0>	Channel register
CAL3	0x35	<6:0>	Channel register
CAL4	0x36	<6:0>	Channel register
CAL5	0x37	<6:0>	Channel register
CAL6	0x38	<6:0>	Channel register
CAL7	0x39	<6:0>	Channel register
GAIN_CAL	0x3A	<9:0>	Channel register
INT_GAIN_CAL	0x3B	<7:0>	Channel register
PHASE_CAL	0x3D	<7:0>	Channel register

The figure below shows the TILD performance of the ADC at 3 junction temperature versus the interpolation done at various temperatures. The measurements were done at 5GSps and with an input of 1900MHz.

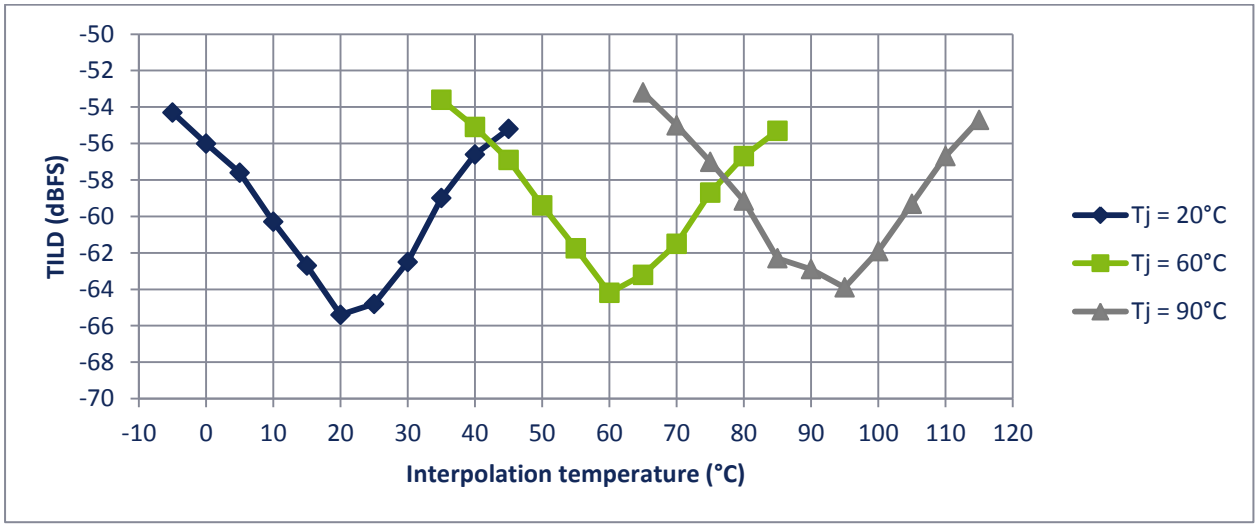


Figure 2: TILD performance versus interpolation temperature

2.2. Necessary SPI instructions

To access the 1st set of calibration the following SPI operation should be done:

WRITE @0x01 (CHANNEL_SEL) 0x0004 #Selection of all channels
WRITE @0x16 (OTP_SPI_SEL) 0x0000 #Selection of factory calibration
WRITE @0x15 (CAL_SET_SEL) 0x0000 #Selection of factory calibration set 1 (hot and ambient)
READ REGISTER

To access the 2nd set of calibration the following SPI operation should be done:

WRITE @0x01 (CHANNEL_SEL) 0x0004 #Selection of all channels
WRITE @0x16 (OTP_SPI_SEL) 0x0000 #Selection of factory calibration
WRITE @0x15 (CAL_SET_SEL) 0x0001 #Selection of factory calibration set 2 (cold)
READ REGISTER

To access the master register (example with A_OFFSET_CAL)

READ	*@0x17 (A_OFFSET_CAL)*		*#Read of master register @0x17 value*
WRITE	*@0x17 (A_OFFSET_CAL)*	*0x0005*	*#Write value 0x0005 to master register @0x17*

To access the channel register (example with GAIN_CAL for channel A)

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0000*	*#Selection of channel A register*
READ	*@0x3A (GAIN_CAL)*		*#Read of channel A register @0x3A value*
WRITE	*@0x3A (GAIN _CAL)*	*0x0003*	*#Write value 0x0003 to channel A register @0x3A*

To set the SPI calibration as the configuration registers of the ADC (otherwise the factory calibration is selected by default)

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x01D7*	*#Selection of SPI calibration*

Realizing the interpolation process will improve the performance while working around temperature V_d. If necessary, it is possible to do a manual calibration for register X_OFFSET_CAL, GAIN_CAL and PHASE_CAL in order to optimize even more the interleaving performance and match them to the clock frequency and input signal. This method is detailed in the following section.

3. Implementing the manual calibration

This method allows for tuning of the offset, gain, phase calibration register to optimize the interleaving calibration to the clock frequency and input signal and improve the interleaving performance compared to the interpolation. This should be done in addition to the interpolation and should not be done instead of the interpolation.

The manual calibration is a process in three steps:

- Offset calibration
- Gain calibration
- Phase calibration

The offset calibration must be done first, followed by the gain calibration and then the phase calibration. Using a different order will result in error in the calibration.

Multiple methods exist to identify the correction to apply for the offset, gain and phase. One method for each of the steps will be explained below. An excel sheet is available upon request at hotline-bdc@e2v.com which can be used to help compute the calibration register value when doing the manual calibration. A user guide of this sheet is in Annex C of this document.
Whichever the method used, the calibration should be done using the sampling frequency and input frequency/power of use to be the most effective. There are two limits to this. The first one is for application where the input power is very low (under -20dBFS). In that case, the calibration should be done at a higher input power otherwise the INL may impacts the calibration. The second one is when working with wideband signals. In that case, the middle frequency should be use when calibrating to avoid side effects.

When doing the manual calibration method, it is necessary to set the SPI calibration as the configuration of the ADC. Otherwise, the factory calibration is used by default and will mask any change made. Refer to the “Necessary SPI instruction” section below.

3.1. Offset calibration

When interleaving multiple ADC cores, as is the case with the EV12AS350, offset mismatch between the cores result in the generation of an interleaving spur at Fs/N, with Fs the sampling frequency and N the number of cores interleaved. The Figure below shows the effect of an offset mismatch between 2 interleaved cores.

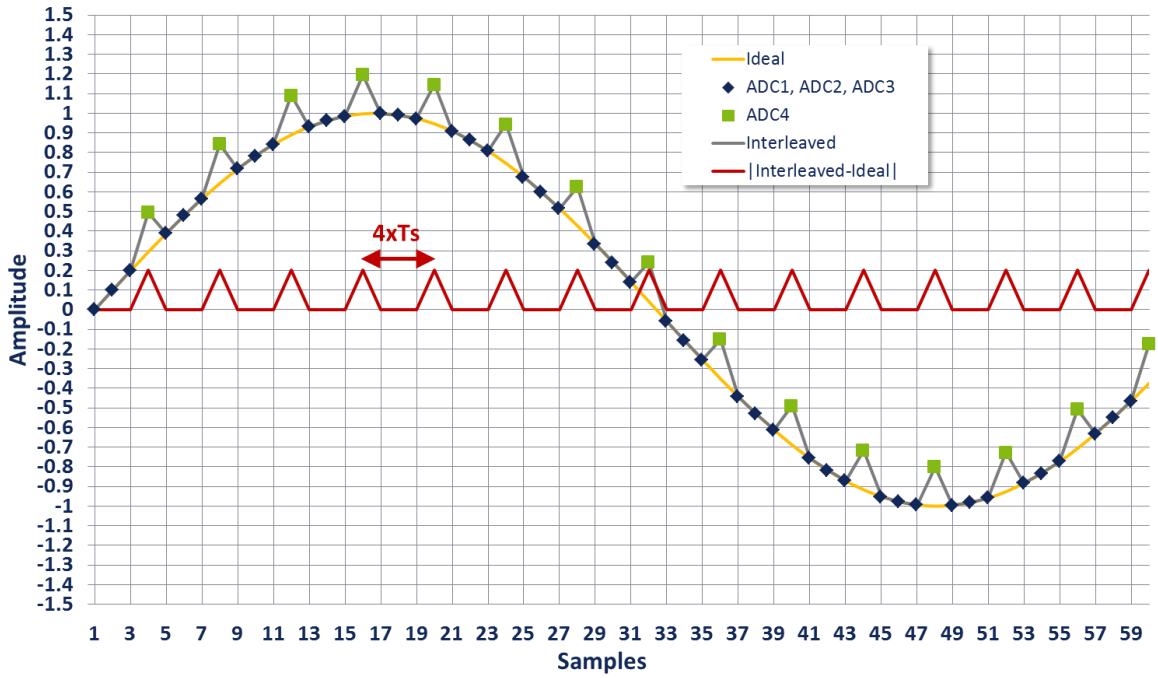


Figure 3: Explanation of offset mismatch consequence

The objective of the offset calibration is to correct for these mismatch in the exact condition of the application. Whereas the interpolation mentioned before corrects for these mismatch in the condition of the factory testing.

In order to correct the offset mismatch between the cores, the following process needs to be applied:

- Input an analog signal with an average value of 0V on the ADC input. A 50Ω termination or a coherent sine wave input can be used for example;
- Do an acquisition over 8192 samples on each of the 4 cores of the EV12AS350. This is the same as doing a single acquisition of 32768 samples (Samples 4n corresponds to core A; samples 4n+1 corresponds to core C; samples 4n+2 corresponds to core B and samples 4n+3 corresponds to core D);
- Average the 8192 per core. Modify X_OFFSET_CAL registers until the average value is within 1-2 LSB from the mid-value of 2047.5.

3.2. Gain calibration

When interleaving multiple ADC cores, as is the case with the EV12AS350, gain mismatch between the cores result in the generation of interleaving spurs at Fs/N +/- Fin, with Fs the sampling frequency, Fin the input frequency and N the number of cores interleaved. The Figure below shows the effect of a gain mismatch between 2 interleaved cores.

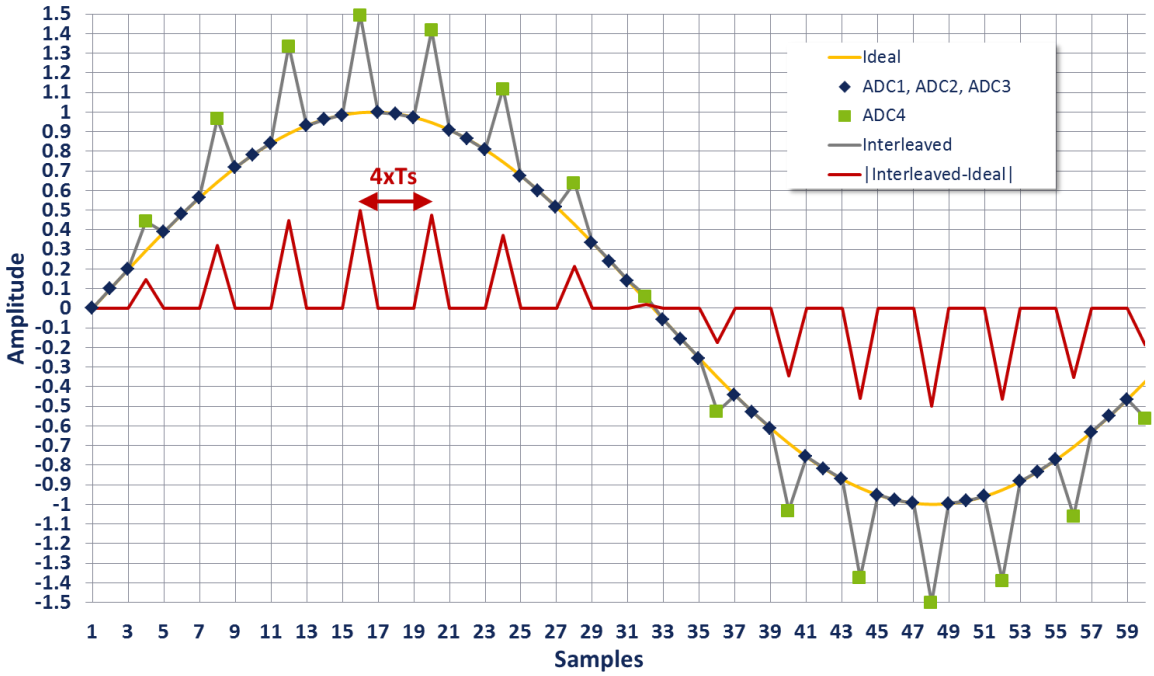


Figure 4: Explanation of gain mismatch consequence

The objective of the gain calibration is to correct for these mismatch in the exact condition of the application. Whereas the interpolation mentioned before corrects for these mismatch in the condition of the factory testing.

In order to correct the gain mismatch between the cores, the following process needs to be applied:

- Input an analog signal with an average gain of 0. A coherent sine wave input can be used for example. A 0Ω termination should not be used as it does not cover a large range of amplitude and would result in an imprecise gain calibration;
- Do an acquisition over 8192 samples on each of the 4 cores of the EV12AS350. This is the same as doing a single acquisition of 32768 samples (Samples 4n corresponds to core A; samples 4n+1 corresponds to core C; samples 4n+2 corresponds to core B and samples 4n+3 corresponds to core D);
- Calculate the average power per core (sum the square value of the samples divided by the number of samples).
- Core A is taken as a reference. Modify the register GAIN_CAL for C, B and D until the average power of core C, B and D are close to the reference.

3.3. Phase calibration

When interleaving multiple ADC cores, as is the case with the EV12AS350, phase mismatch between the cores result in the generation of interleaving spurs at Fs/N +/- Fin, with Fs the sampling frequency, Fin the input frequency and N the number of cores interleaved. The Figure below shows the effect of a phase mismatch between 2 interleaved cores.

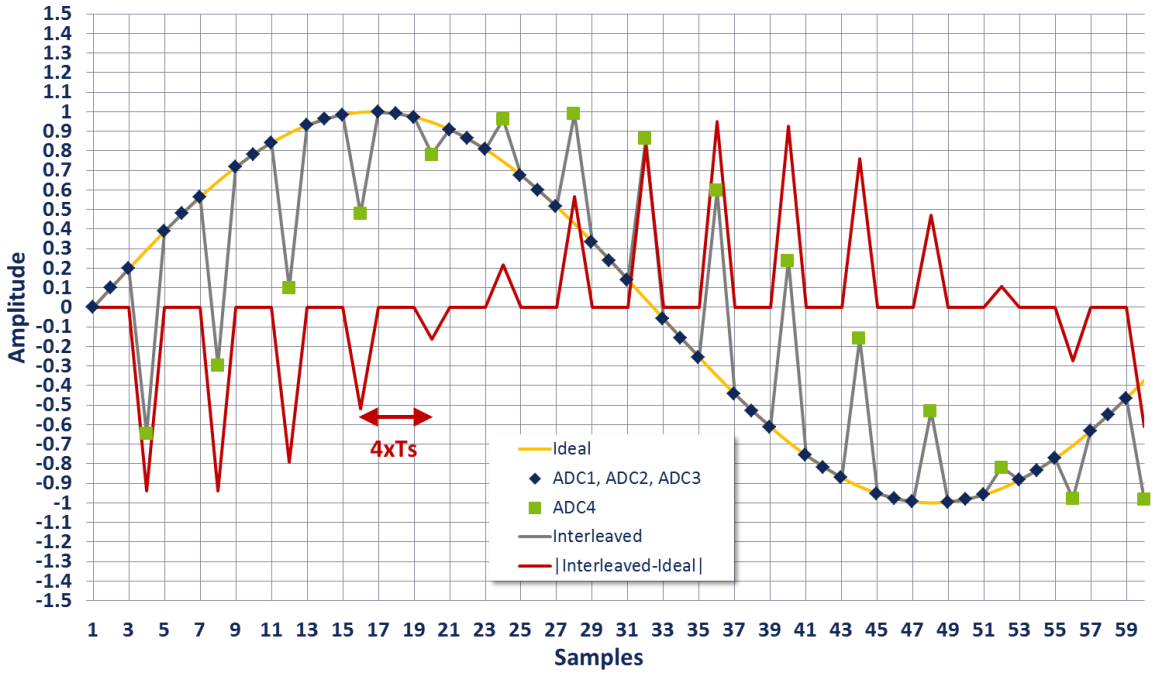


Figure 5: Explanation of phase mismatch consequence

The objective of the phase calibration is to correct for these mismatch in the exact condition of the application. Whereas the interpolation mentioned before corrects for these mismatch in the condition of the factory testing.

The phase mismatch can come from either clock propagation time difference between the cores, input propagation time between the cores or both.

In order to correct the phase mismatch between the cores, the following process needs to be applied:

- Apply a coherent sinewave input signal;
- Do an acquisition per core over 32768 samples; This is the same as doing a single acquisition of 131072 samples (Samples 4n corresponds to core A; samples 4n+1 corresponds to core C; samples 4n+2 corresponds to core B and samples 4n+3 corresponds to core D);
- Calculate the FFT imaging value at the sine wave frequency for each core.
- Correct the PHASE_CAL register until you reach a phase difference of 90° between core A and C; 180° between core A and B; and 270° between core A and D.

3.4. Necessary SPI instructions

To set the SPI calibration as the configuration registers of the ADC (otherwise the factory calibration is selected by default)

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x01D7*	*#Selection of SPI calibration*

To access the offset calibration register (example with C_OFFSET_CAL):

READ	*@0x19 (C_OFFSET_CAL)*		*#Read of master register @0x19 value*
WRITE	*@0x19 (C_OFFSET_CAL)*	*0x0009*	*#Write value 0x0009 to master register @0x19*

To access the gain calibration register (example with channel B GAIN_CAL):

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0001*	*#Selection of channel B register*
READ	*@0x3A (GAIN_CAL)*		*#Read of channel B register @0x3A value*
WRITE	*@0x3A (GAIN _CAL)*	*0x0008*	*#Write value 0x0008 to channel B register @0x3A*

To access the phase calibration register (example with channel D PHASE_CAL):

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0003*	*#Selection of channel D register*
READ	*@0x3D (PHASE_CAL)*		*#Read of channel D register @0x3D value*
WRITE	*@0x3D (PHASE _CAL)*	*0x0023*	*#Write value 0x0023 to channel D register @0x3D*

Related documentation

EV12AS350 Product page: http://www.e2v.com/products/semiconductors/adc/ev12as350/
EV12AS350 Datasheet: http://www.e2v.com/resources/account/download-datasheet/3274

ANNEX A: Example of interpolation process for one master register (example with B_OFFSET_CAL)

1. Read register value from 1st set of factory calibration

```
WRITE   @0x01 (CHANNEL_SEL)     0x0004      #Selection of all channels
WRITE   @0x16 (OTP_SPI_SEL)     0x0000      #Selection of factory calibration
WRITE   @0x15 (CAL_SET_SEL)     0x0000      #Selection of factory calibration set 1 (hot and ambient)
READ    @0x18 (B_OFFSET_CAL)                #Read of master register @0x18 value
```

⇨ Example value read is “100101011”, then R_0 = 299

2. Read register value from the 2nd set of factory calibration

```
WRITE   @0x01 (CHANNEL_SEL)     0x0004      #Selection of all channels
WRITE   @0x16 (OTP_SPI_SEL)     0x0000      #Selection of factory calibration
WRITE   @0x15 (CAL_SET_SEL)     0x0001      #Selection of factory calibration set 2 (cold)
READ    @0x18 (B_OFFSET_CAL)                #Read of master register @0x18 value
```

⇨ Example value read is “100001101”, then R_0 = 269

3. Measure the temperature diode value in mV

⇨ Example value measured is 760mV / 102°C, then V_d = 760

4. Apply the interpolation formula

$$R_{SPI} = \frac{R_0 - R_1}{787 - 830}(V_d - 830) + R_1 = \frac{299 - 269}{787 - 830}(760 - 830) + 299 = 348$$

5. Convert R_{SPI} in binary and write it in the corresponding SPI register

⇨ In binary R_{SPI} is “101011100”.

```
WRITE   @0x18 (B_OFFSET_CAL)    0x015C      #Write value 0x015C to master register @0x18
WRITE   @0x01 (CHANNEL_SEL)     0x0004      #Selection of all channels
WRITE   @0x16 (OTP_SPI_SEL)     0x01D7      #Selection of SPI calibration
```

ANNEX B: Example of interpolation process for one channel register (example with GAIN_CAL of channel A)

1. Read register value from 1st set of factory calibration

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x0000*	*#Selection of factory calibration*
WRITE	*@0x15 (CAL_SET_SEL)*	*0x0000*	*#Selection of factory calibration set 1 (hot and ambient)*
WRITE	*@0x01 (CHANNEL_SEL)*	*0x0000*	*#Selection of channel A register*
READ	*@0x3A (GAIN_CAL)*		*#Read of channel A register @0x3A value*

⇨ Example value read is “0100011011”, then R_0 = 283

2. Read register value from the 2nd set of factory calibration

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x0000*	*#Selection of factory calibration*
WRITE	*@0x15 (CAL_SET_SEL)*	*0x0001*	*#Selection of factory calibration set 2 (cold)*
WRITE	*@0x01 (CHANNEL_SEL)*	*0x0000*	*#Selection of channel A register*
READ	*@0x3A (GAIN_CAL)*		*#Read of channel A register @0x3A value*

⇨ Example value read is “0001110100”, then R_0 = 116

3. Measure the temperature diode value in mV

⇨ Example value measured is 760mV / 102°C, then V_d = 760

4. Apply the interpolation formula

$$R_{SPI} = \frac{R_0 - R_1}{787 - 830}(V_d - 830) + R_1 = \frac{283 - 116}{787 - 830}(760 - 830) + 116 = 388$$

5. Convert R_{SPI} in binary and write it in the corresponding SPI register

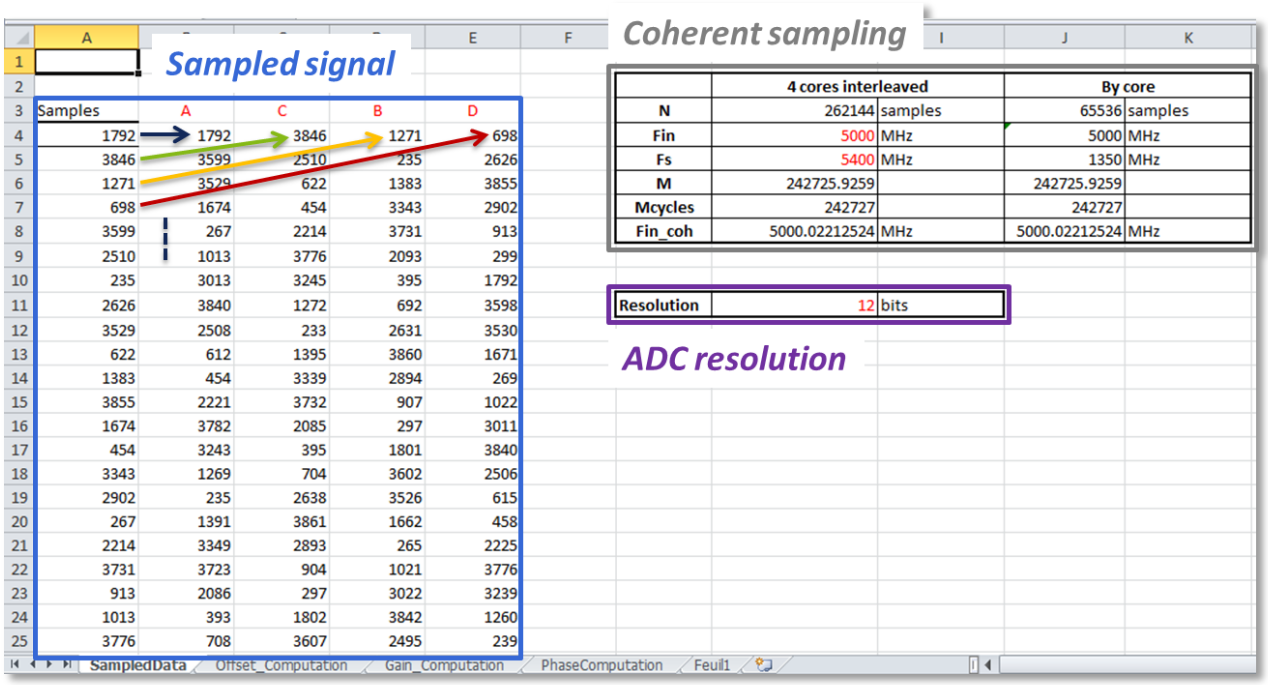
⇨ In binary R_{SPI} is “0110000100”.

WRITE	*@0x01 (CHANNEL_SEL)*	*0x0000*	*#Selection of channel A register*
WRITE	*@0x3A (GAIN _CAL)*	*0x0184*	*#Write value 0x0184 to channel A register @0x3A*
WRITE	*@0x01 (CHANNEL_SEL)*	*0x0004*	*#Selection of all channels*
WRITE	*@0x16 (OTP_SPI_SEL)*	*0x01D7*	*#Selection of SPI calibration*

ANNEX C: Using the excel sheet for manual calibration

An excel sheet is available upon request at hotline-bdc@e2v.com which can be used to help compute the calibration register value when doing the manual calibration. The first worksheet is where the acquisition data and parameters are input. The next 3 worksheet indicate the correction to add on the register value. The cell greyed should not be modified.

Samples from Column A are splitted into 4 columns such as they are gathered according to the core they are digitized from (click on the De-interlacing button at the top to realize this). Coherent input frequency is computed. It corresponds to the frequency of the input signal coming from the signal generator used for the calibration. The ADC resolution is also used for the computation in next worksheets.



Samples	A	C	B	D
1792	1792	3846	1271	698
3846	3599	2510	235	2626
1271	3529	622	1383	3855
698	1674	454	3343	2902
3599	267	2214	3731	913
2510	1013	3776	2093	299
235	3013	3245	395	1792
2626	3840	1272	692	3598
3529	2508	233	2631	3530
622	612	1395	3860	1671
1383	454	3339	2894	269
3855	2221	3732	907	1022
1674	3782	2085	297	3011
454	3243	395	1801	3840
3343	1269	704	3602	2506
2902	235	2638	3526	615
267	1391	3861	1662	458
2214	3349	2893	265	2225
3731	3723	904	1021	3776
913	2086	297	3022	3239
1013	393	1802	3842	1260
3776	708	3607	2495	239

	4 cores interleaved		By core	
N	262144	samples	65536	samples
Fin	5000	MHz	5000	MHz
Fs	5400	MHz	1350	MHz
M	242725.9259		242725.9259	
Mcycles	242727		242727	
Fin_coh	5000.02212524	MHz	5000.02212524	MHz

Resolution	12	bits

Real and imaginary parts of the FFT are computed using cos() and -sin() functions.

Index	Cos()	-Sin()
0	1	0
1	-0.28670458	0.95801904
2	-0.83560097	-0.5493369
3	0.76584583	-0.64302423
4	0.39645795	0.91805288
5	-0.99317845	0.1166043
6	0.17303968	-0.98491485
7	0.89395592	0.44815491
8	-0.68564219	0.72793872
9	-0.5008024	-0.86556164
10	0.97280688	-0.23161775
11	-0.05701398	0.99837338
12	-0.94011454	-0.3408587
13	0.59608427	-0.80292188
14	0.59831436	0.80126146
15	-0.9391632	0.34347122
16	-0.05978957	-0.998211
17	0.97344709	0.22891212
18	-0.49839391	0.8669507
19	-0.68766346	-0.72602959
20	0.89270644	-0.45063867
21	0.1757774	0.98442994

Offset, gain and phase are corrected using next worksheets.

Worksheet used for Offset correction:

	A	B	C	D	E
1		**A**	**C**	**B**	**D**
2	Mean value	2048.07773	2047.89467	2047.92926	2048.14803
3	Theo. Mean	2048	2048	2048	2048
4	Difference	0.07772827	-0.10533142	-0.07073975	0.14802551
5	Offset reg	-0.07772827	0.10533142	0.07073975	-0.14802551
6	**EV12AS350A**	-0.70662065	0.95755837	0.6430886	-1.34568648

Value to adjust

Value to add to the actual OFFSET REGISTER:
= (Offset reg)/(offset correction step)

Worksheet used for Gain correction:

	A	B	C	D	E
1		**A**	**C**	**B**	**D**
2	Real	31215538.24	24427416.3	12377228.4	-2284529.5
3	Imag	-7819335.25	-21021776.4	-29745189.8	-32078701.6
4					
5	Module	32179991.17	32227530.9	32217574.4	32159946.7
6	Diff to Core A		0.01282227	0.01013839	-0.00541201
7	Gain reg		-0.01282227	-0.01013839	0.00541201
8					
9	Module_dBFS	-6.3817585	-6.36893623	-6.37162011	-6.38717051
10			0.01282227	0.01013839	-0.00541201
11	**EV12AS350A**		12.8222687	10.1383851	-5.41201026

Value to adjust

Value to add to the actual GAIN REGISTER:
= (Gain reg)/(gain correction step)

Worksheet used for Phase correction:

	A	B	C	D	E
1		**A**	**C**	**B**	**D**
2	Real	31215538.24	24427416.28	12377228.44	-2284529.501
3	Imag	-7819335.252	-21021776.43	-29745189.78	-32078701.59
4					
5	Arg (°)	-14.06293172	-40.71466968	-67.40738668	85.92647847
6					
7	delta phi theo		333.335	666.670	1000.004
8	delta/A in °		-26.652	-53.344	99.989
9	Delta/theo in ° (between -PI/2 and PI/2)		0.013	-0.014	-0.015
10	Delta/theo in s		7.4742E-15	-7.8176E-15	-8.3415E-15
11	Delta/theo in fs		7.474	-7.818	-8.342
12	Phase reg		-7.474	7.818	8.342
13	**EV12AS350A**		-0.311426731	0.325731438	0.347564466

Value to adjust

Value to add to the actual PHASE REGISTER:
= (Phase reg)/(phase correction step)