EV12AS350
CER improvement from Revision A to Revision B

November 2017

Document aim and comment

This document aims at explaining how the Conversion Error Rate (CER) is improved when moving from Revision A (EV12AS350A) to Revision B (EV12AS350B) of the EV12AS350 ADC. This document should be read with all other applicable documentation related to this part and in particular its datasheet.

Introduction

The Conversion Error Rate (CER) is the probability to exceed a specified error threshold for a sample at a maximum sampling rate. An unexpected behavior on the input stage of the ADC (revision A or EV12AS350A) led to a degradation of the CER.

In this document, the CER is characterized over different conditions of sampling rate (or clock frequency), input signal amplitude, temperature. As a first conclusion, CER is independent of input signal frequency and power supplies. CER of EV12AS350A is improved reducing the clock frequency, increasing the input signal amplitude and reducing the junction temperature.

The results shown in this document should help the users of EV12AS350**A** to determine if the CER will impact their application. We are first describing the root cause of the phenomenon before showing performance results in different conditions. A possible software corrective solution is also provided before EV12AS350**B** is available.

Content

1. Description of the phenomenon

1.1. Quantification errors

Time domain glitches caused by quantification errors or conversion errors can appear in the signals digitized by EV12AS350A, in the conditions described in Figure 1, and at the rate described in Figure 2, Figure 3and Figure 4.

The magnitude of these glitches is modulo 256, that is either 256 or 512 codes, or multiples of 256. The rate of occurrence of these glitches increases with temperature and sampling frequency, as can be seen on Figure 2 and Figure 3. It also decreases with high analog input power (Ain). Thus Figure 2 should be considered as a worst case. The power supplies and input frequency do not impact the rate of occurrence.

Figure 1 – Glitch occurrence zones

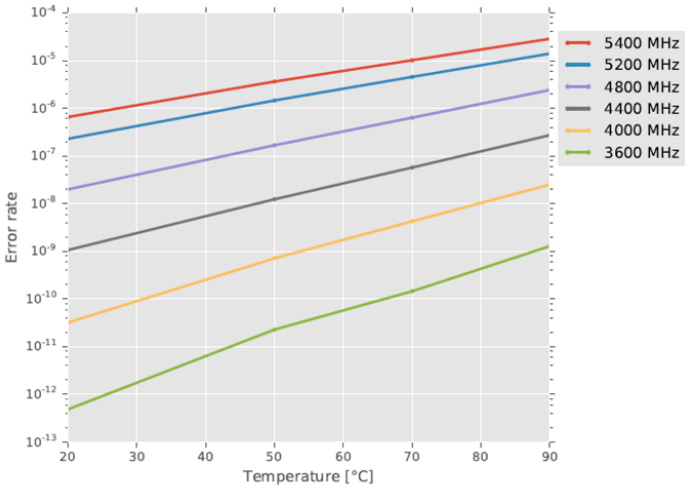

Figure 2 – Error rate versus sampling frequency and temperature (Ain at -40 dBFS)

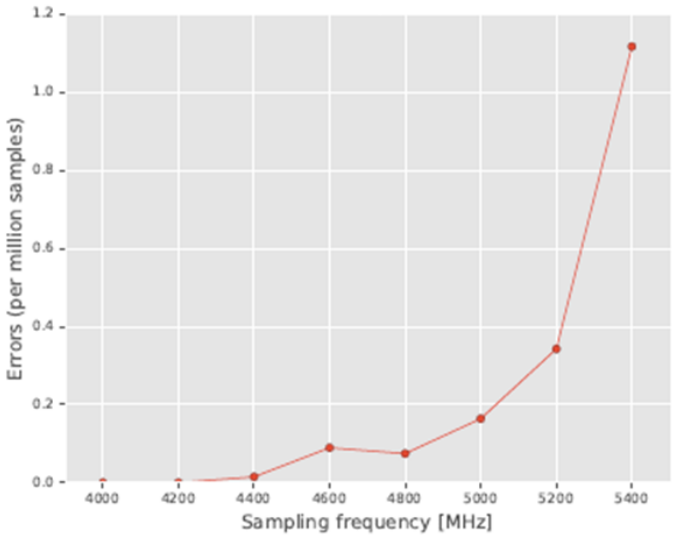

Figure 3 – Error rate versus sampling frequency

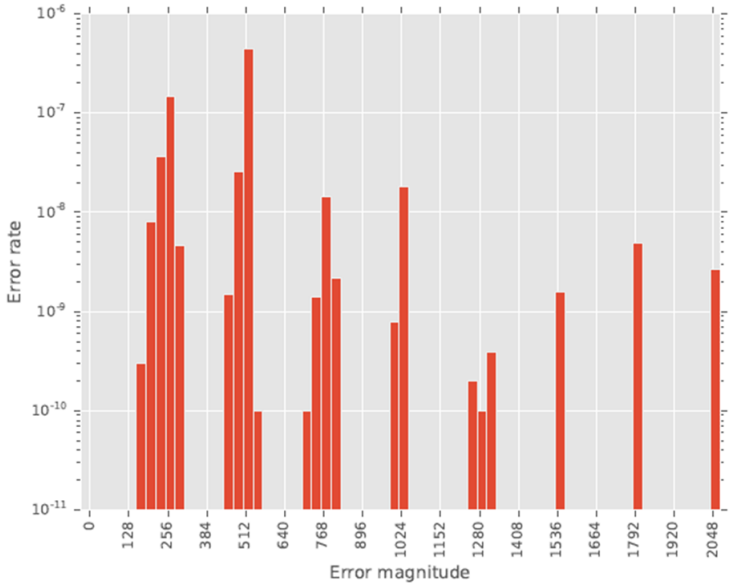

Figure 4 – Statistical distribution quantification errors by error magnitude (Ain at -40 dBFS)

1.2. Root cause

EV12AS350A is structured around four ADC cores that are time interleaved on chip. The errors are caused by the conversion process inside the ADC cores, the errors do not happen in the interface at the output stage.

The phenomenon occurs within a specific stage of the ADC cores which is affected by speed limitations causing conversion errors of the 4 Most Significant Bits (MSBs).

When the analog signal is at a level close to ADC internal references, the MSB quantification can happen in ambiguous conditions and consequently errors can occur.

The quantification process can be affected by:

- ❑ Stage gain
- ❑ Stage settling time compared to clock period
- ❑ Uncertainties on MSB bits cause false quantifications which in turn translate into glitches in the digitized signal and thus reduce the CER

1.3. Impact on performance

- ❑ SFDR performance remains unaffected by the phenomenon
- ❑ Depending on amplitude and occurrence of glitches, noise floor can increase by up to 10 dB (worst case obtained at low Ain) for a short amount of time during the occurrence of glitches. In Ain at -10 dBFS and higher, the impact on noise floor is less than 6-7 dB.

2. Recommendations for treatment

Teledyne-e2v has worked on a workaround algorithm to remove the glitches to be implemented in FPGA. This algorithm is available upon request and brings improvement of about 10^{-3}. More information on this algorithm is detailed below.

Teledyne-e2v is working on a new design of this product to completely correct these glitches. The origin of the glitches has been well understood and Teledyne-e2v has high confidence in the correction being implemented. This correction is targeting a worst case CER at 10^{-9} at Tj=110°C. At ambient temperature, the CER targeted is 10^{-12}. This new version of the EV12AS350 will be called EV12AS350B to differentiate it from revision A.

3. Glitch error correction firmware

The source code and synthesized netlist for an FPGA implementation of glitch error correction logic is available to users of EV12AS350A under a limited license from Teledyne Signal Processing Devices Sweden AB (Teledyne SPDevices, spdevices.com). This error correction logic supports the maximum sampling frequency of EV12AS350, i.e. it can be operated up to 5.4 GSps.

Figure 5 to Figure 7 show the glitch error correction performance for the temperatures 70°C and 90°C, and sampling frequencies 4800 MSps and 5400 MSps, over the first Nyquist zone.

The glitch error correction logic is not intended for latency-critical applications and the logic is implemented in FPGAs without consuming neither predefined multipliers not Block RAM. The resource utilization for the glitch error correction logic is as follows:

FPGA Resource Type	Utilization
Slice Look-up tables	29,591
Slide Registers	34,795
Block RAM	0
Multipliers	0

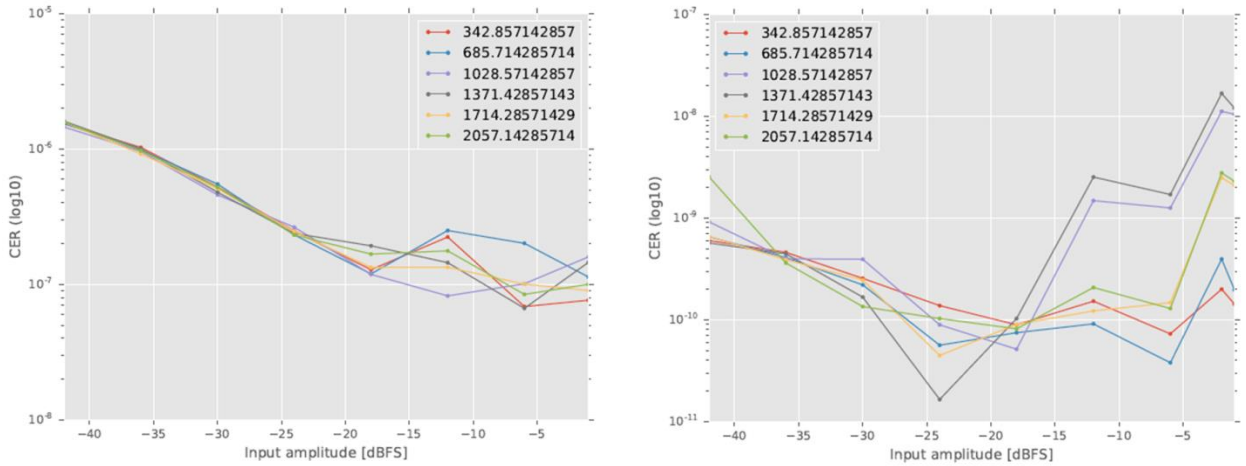

Figure 5 – Conversion error rate versus input amplitude for different input frequencies. Sampling frequency is 4800 MSps and temperature is 90°C. EV12AS350 raw data (left) and EV12AS350A with glitch error correction logic (right)

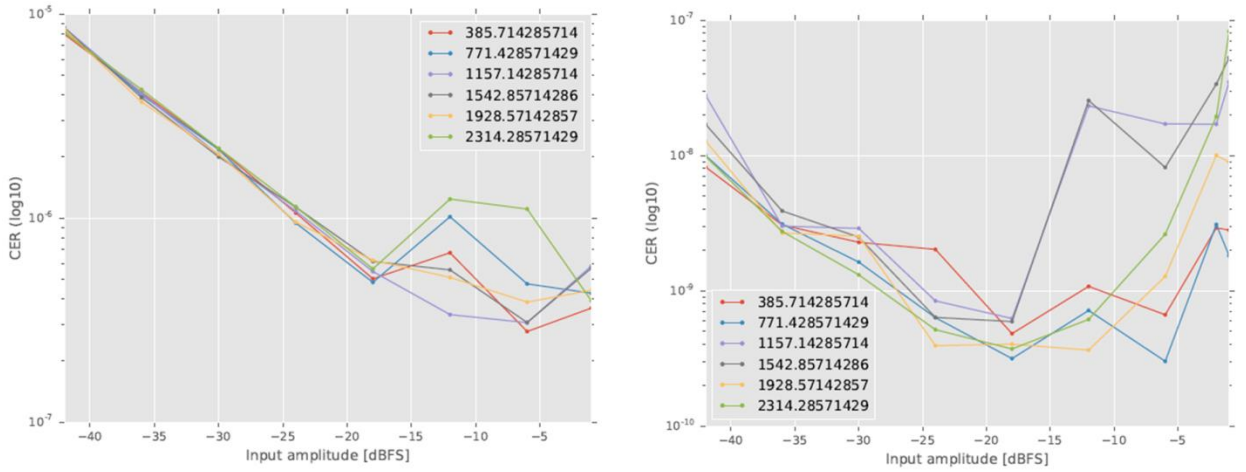

Figure 6 – Conversion error rate versus input amplitude for different input frequencies. Sampling frequency is 5400 MSps and temperature is 70°C. EV12AS350 raw data (left) and EV12AS350A with glitch error correction logic (right)

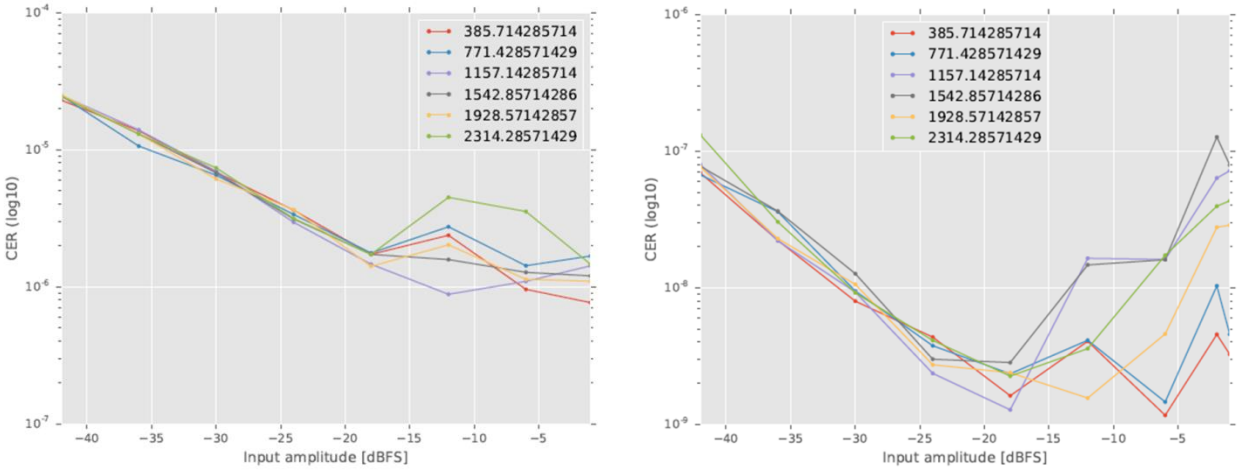

Figure 7 – Conversion error rate versus input amplitude for different input frequencies. Sampling frequency is 5400 MSps and temperature is 90°C. EV12AS350 raw data (left) and EV12AS350A with glitch error correction logic (right)

Related documentation

Datasheet of EV12AS350 ADC:
http://www.e2v.com/resources/account/download-datasheet/3274

Product page of EV12AS350:
http://www.e2v.com/products/semiconductors/adc/ev12as350/

Product overview of EV12AS350-ADX4-EVM:
http://www.e2v.com/shared/content/resources/File/documents/broadband-data-converters/EV12AS350/EV12AS350-ADX4-EVM_PB.pdf