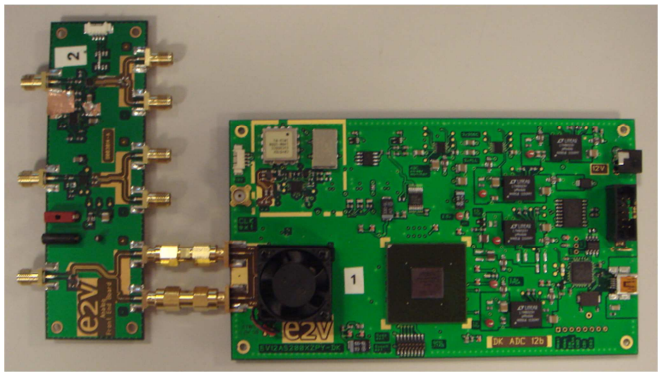


Demo Kit 12bit 1.5GSps ADC EV12AS200ZPY-DK

Summary Datasheet - *Preliminary*

Main Features

- ADC with 12-bit resolution
  - 1.5 Gsps Sampling Rate
- On board PLL generated 1.5 GHz Clock
- External Clock option
- External trigger function demonstrator
- On Board FPGA (Altera Aria2)
- Analog daughter board with 3 analog inputs with different configurations
  - Differential driver (AC or DC coupling)
  - Balun RF transformer.
- Control and Acquisition Display using P.C. based GUI
  - FFT computation (PC software provided)
  - Flexible and easy to operate via USB2 (PC software provided without any license)
  - Monitoring of ADC currents and junction temperature
- +12V supply adaptor supplied.

Operating conditions

- Temperature range: 10℃ < Tamb < 40℃
- Operating with a Microsoft Windows PC environment (Windows 2000, Windows XP, Windows Vista, Windows7) via USB interface.

Applications

- Demonstration and Evaluation of EV12AS200 12 bit 1.5 GSps analog to digital converter

1. General overview

The EV12AS200-DK Demo Kit enables the easy evaluation of the characteristics and performance of the 12 bit , 1.5GSps ADC . The Demo kit is plug_and_play and needs little external equipment.

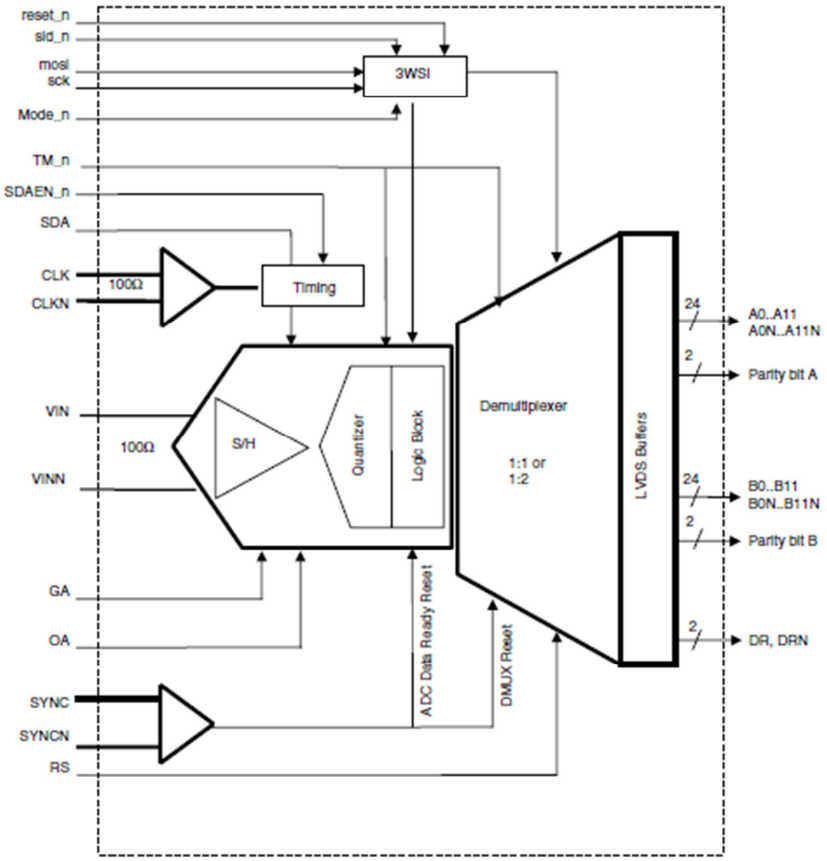
The Demo kit is delivered with software which allows acquisition of data using the on board FPGA.

An on board FPGA is incorporated onto the board providing a full speed interface to the ADC.

This board is designed for use as a reference design.
All front end interfaces are provided on a daughterboard. Included: DC-DC regulator, ADC driver, clock generator….
The VHDL data acquisition code for the FPGA on board is supplied.

2. EV12AS200 Block Diagram

Figure 1. Simplified Block Diagram

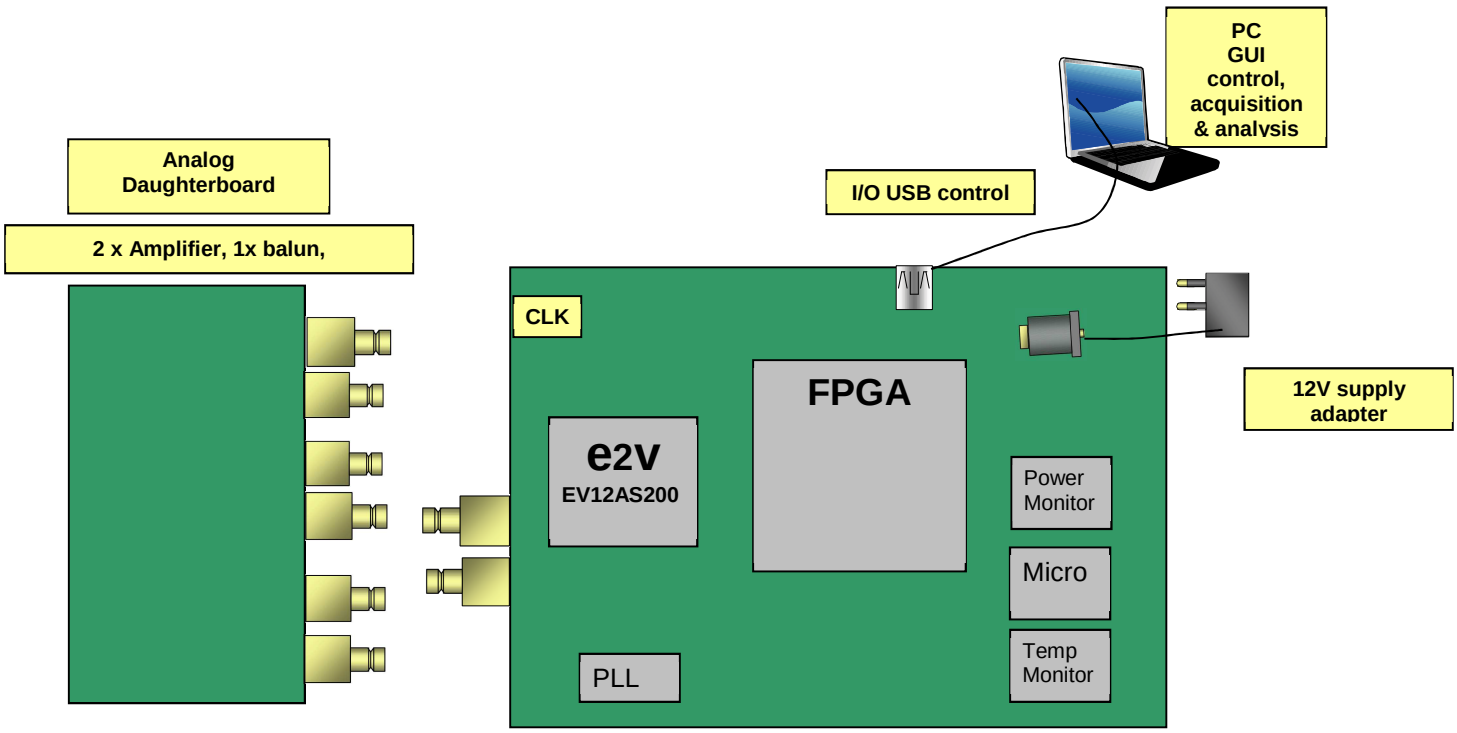


3. EV12AS200 Description

The EV12AS200 is a 12-bit 1.5 GSps ADC. The device includes a front-end Track and Hold stage (T/H),followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels
before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100∧ differential output buffers. It integrates 3 Wires Serial Interface (3WSI) circuit (write only), which can be activated or deactivated (via Mode signal). Main functions accessed via the 3WSI can also be accessed by hardware (OA, GA, SDA, SDAEN_n, TM_n, RS pin).
The EV12AS200 works in fully differential mode from analog inputs through digital outputs.
It operates in the first Nyquist zone up to L-Band.
DEMUX Ratio (1:1 or 1:2) can be selected with the pin RS or via the 3WSI when activated.

The gain control pin GA and offset control OA are provided to adjust the ADC gain and offset transfer function. These functions can also be accessed via the 3WSI.
A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example. It is enabled thanks to SDAEN_n pin. This
function is also available with the 3WSI. In this case the tunable range is extended thanks to 2 bits for coarse adjustment.

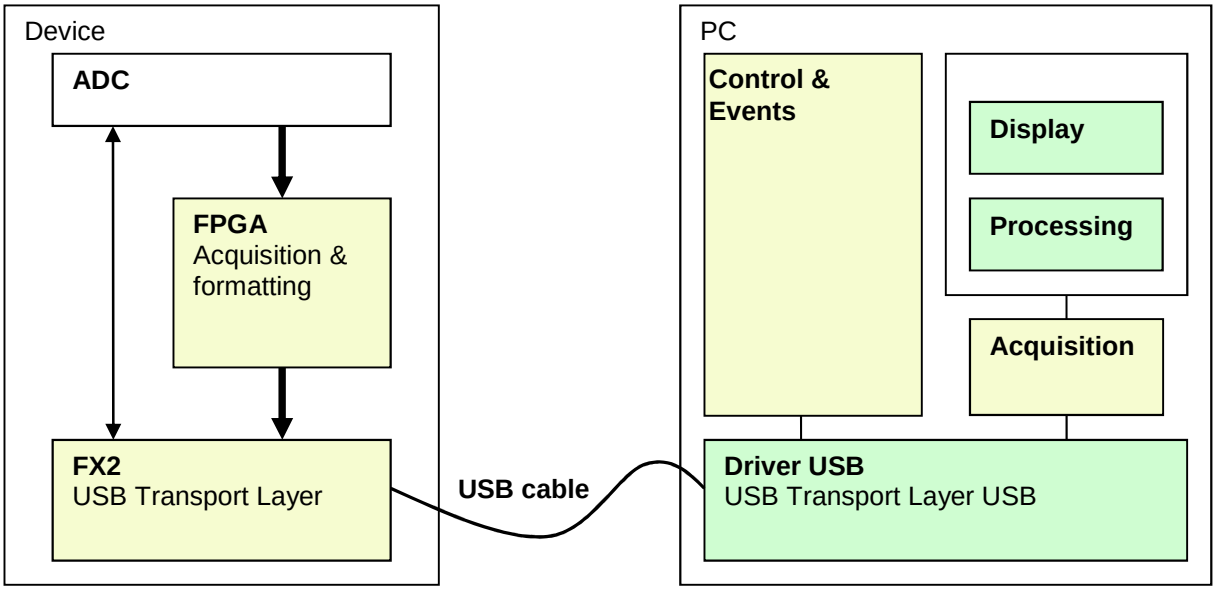
Figure 2. EV12AS200TPY-DK Demo Kit system architecture



The complete system is built with the e2v demo kit.
e2v Demo kit contains the following items :

- Quad 10-bit Demo kit with EV12AS200TPY
- Cables & Power Supply
  - Universal 12V power Adapter & Cables
  - USB Cable to communicate with a PC (control of ADC settings and settings for data acquisition)
- 3 analog inputs with SMA connectors on daughterboard
- 1 clock input with SMA connector (if external clock input is programed)
- CD ROM with GUI Software

Figure 3. EV12AS200TPY-DK Demo Kit functional architecture



Acquisition and formatting of ADC digital output data are done within the FPGA, as maximum of 256K samples can be taken
Data is then transmitted again to the ADC Demo Kit.
A USB driver on the ADC Demo kit allows for transmission of the data to the computer that performs the display and processing of ADC output data (FFT).
Software and Graphical User Interface are provided with the Demo Kit.

The provided software operates using Labview RunTime (no license required).

4. Ordering Information

Table 1. Ordering information

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AS200ZPY-DK	N/A	Ambient	N/A	