

## DATASHEET

### OVERVIEW

EV12AD550 is a dual S-band capable 12-bit ADC intended for space applications that is built using true single core architecture per channel providing high spectral purity.

With a 3dB input bandwidth up to 4.3GHz, it allows for direct digitization in S-band without frequency down-conversion. Synthetic Aperture Radar systems will also be able to operate this ADC with reduced dynamic range at frequencies beyond 5GHz (C-band) without frequency down-conversion.

This device includes a multiple ADC chained synchronization feature. This would help designing large array of synchronous ADCs to support the development of MIMO systems using digital or hybrid analog/digital beam-forming techniques in active antennas.

Multichannel applications will benefit from a cross-talk isolation between inputs in excess of 80dB and Noise Power Ratio performance of 50dB in the first Nyquist zone and better than 45dB in the 4<sup>th</sup> Nyquist zone.

This device comes in a hermetic flip chip CCGA323 package in Aluminum Nitride with improved thermal performance and is planned for QML-V and ESCC certification.

### APPLICATIONS

- Earth observation SAR payload
- Telecommunication satellite payload
- Satellite data links
- Satellite altimeter
- Satellite TWTA compensation system
- Satellite to satellite laser data links

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### FEATURES

#### Dual channel 12-bit 1.6GSps ADC

- Single core architecture ADC per channel
- Differential analog input voltage: 1Vppd
- Full Power Input bandwidth (-3dB): 4.3GHz
- Differential clock input
- Power consumption: 2.3W / channel
- Power supplies: Single Rail 3.4V or Dual rail 3.4V/2.5V
- Low latency output interface: LVDS DEMUX 1:1 or 1:2
- Package: Hermetic CCGA323 21x21mm / 1mm pitch, Aluminum Nitride material
- SPI configuration with space protection control
- Multiple ADC chained synchronization
- Test mode: ramp, flash, PRBS
- Control bit: parity, in-range, trigger
- Clock input up to 3.2GHz

### PERFORMANCE @ 1.5GSps

- 4.3GHz analog input bandwidth (-3dB)
- 50 dB NPR over 1<sup>st</sup> Nyquist
- 47 dB NPR over 2<sup>nd</sup> Nyquist
- 46 dB NPR over 3<sup>rd</sup> Nyquist
- 45 dB NPR over 4<sup>th</sup> Nyquist
- 76 dBFS SFDR at 100MHz, -1dBFS
- 70 dBFS SFDR at 1480MHz, -1dBFS
- 75 dBFS SFDR at 1900MHz, -8dBFS
- 68 dBFS SFDR at 3730MHz, -12dBFS
- 59 dBFS SFDR at 5300MHz, -12dBFS
- Latency < 10ns

DS-1198B, February 2019

# 1 Block Diagrams

## 1.1 DEMUX 1:1

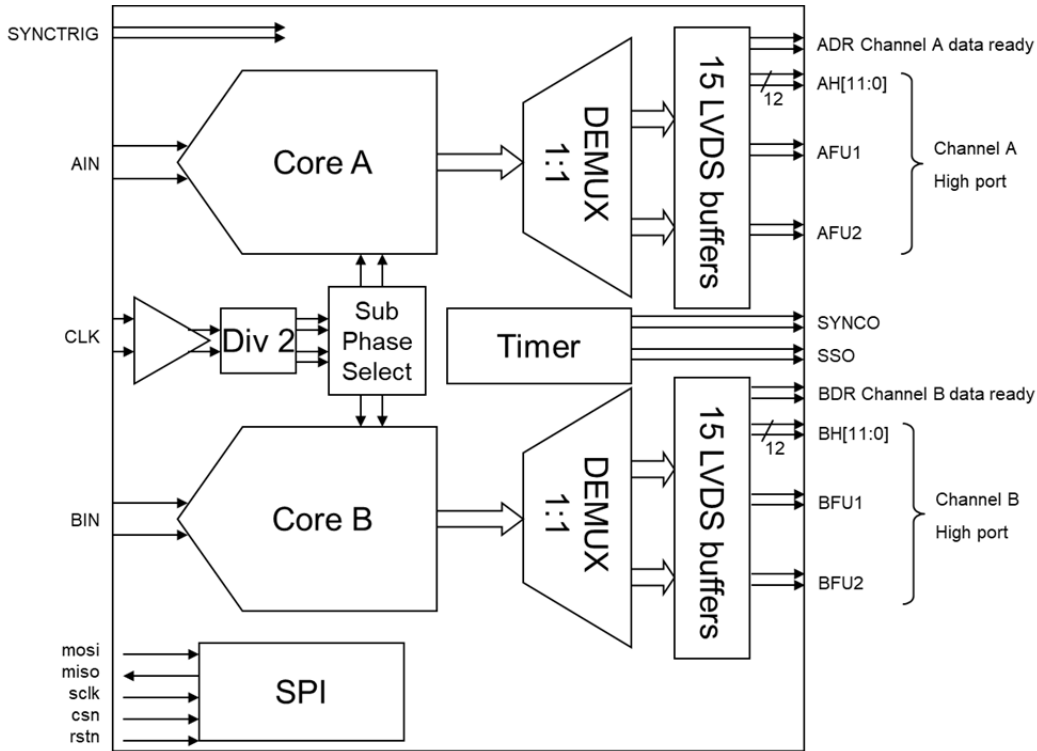


Figure 1: Block diagram in DEMUX 1:1 output mode

## 1.2 DEMUX 1:2

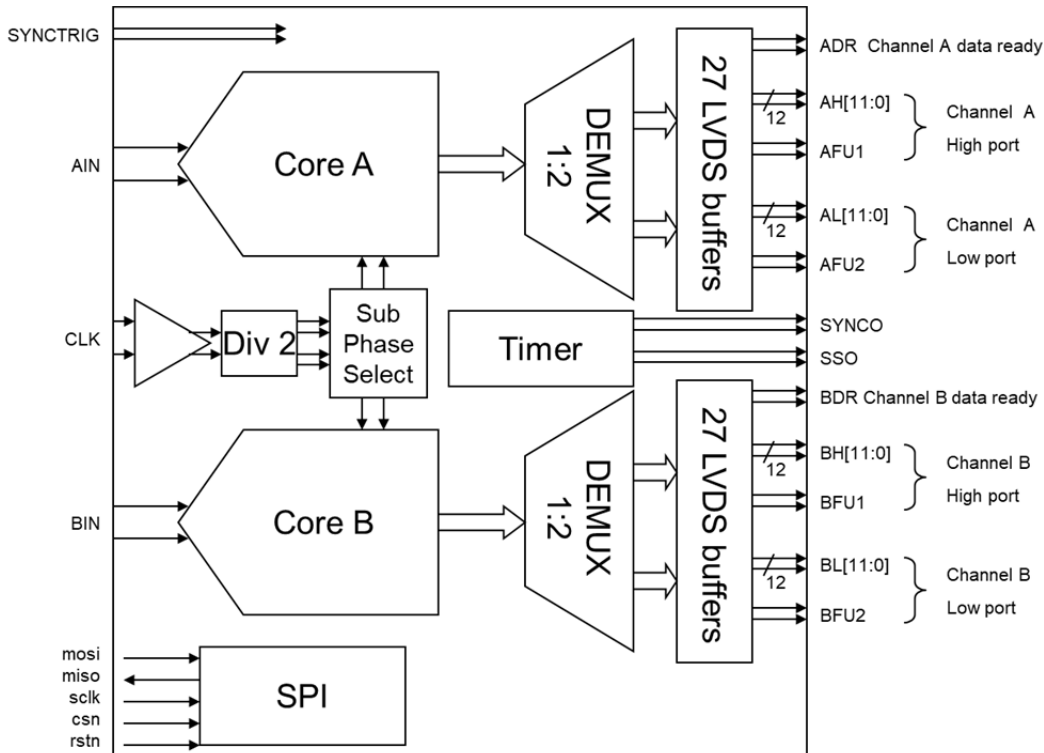


Figure 2: Block diagram in DEMUX 1:2 output mode

## 2 Description

### 2.1 Description

The EV12AD550 is a dual 12-bit 1.6 GSps ADC featuring low latency LVDS parallel outputs with a built-in selectable 1:2 or 1:1 DEMUX to compromise between power consumption and ease of interfacing.

The two channels can operate in phase or in opposition, thus allowing synchronous or interleaved sampling. Each channel is composed of a true single core ADC sampling at up to 1.6 GSps. Based on an innovative architecture without internal interleaving, it provides high spectral purity. It offers an analog input bandwidth of up to 4.3 GHz with 2 selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. It also features a novel synchronization method to ease the synchronization of a large number of ADCs. This device is clocked at twice the sampling rate of each channel. It is controlled through an SPI interface. All sensitive areas of the device have been protected to increase robustness to radiation. This includes, but is not limited to, clock circuitry and SPI registers. A rad hard mode is also provided to increase this robustness of the ADC and prevent potential external influence.

The EV12AD550 is available in a CCGA323 hermetic package using flip-chip assembly and operates over the extended temperature range  $-55^{\circ}\text{C}$  top case temperature( $T_c$ ); junction temperature ( $T_j$ ) under  $+125^{\circ}\text{C}$ . This package is based on Aluminum Nitride material with enhanced thermal interface to ease power dissipation.

### 2.2 Differences between EV12AD550A & EV12AD550B

EV12AD550A and EV12AD550B are fully pin to pin compatible and digitally compatible. REV B offers new features as described below.

Once fully validated and qualified, the EV12AD550B aims at fully replacing the EV12AD550A. For any question, please contact [hotline-bdc@teledyne-e2v.com](mailto:hotline-bdc@teledyne-e2v.com).

#### 1. Sampling Delay Adjust (SDA): increased range

- The revision A offers a SDA range of 10ps. It is improved up to 90ps in the revision B.

#### 2. Multi-ADC synchronization: new features

- Revision B embeds a meta-stability detection flag through SPI on the SYNCTRIG input in SYNC mode.
- Revision B includes a new feature to add one clock cycle delay to the timing restart after a SYNC.

Both these features aim at facilitating synchronization of multiple devices or system needing a deterministic sampling.

#### 3. Performance: improved H2 & H3 linearity

- The linearity performance on the revision B is slightly improved compared to revision A, especially for high input levels.

#### 4. Trigger propagation delay: identical to data path

- The time propagation delay between data path and trigger path is identical in the revision B.

#### 5. Sampling Frequency

- The sampling frequency in revision B is extended up to 1.6 GSps (production tests at 1.5 GSps).

#### 6. Slight I<sub>ccd</sub> Current increase

- Compare to revision A, revision B presents a higher I<sub>ccd</sub> current increase around 50mA-80mA that represents less than 4% of the total power consumption. The thermal model is unchanged.

### 3 Specifications

#### 3.1 Absolute maximum ratings

Absolute maximum ratings are limiting and stressing values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Exposure above those conditions may cause permanent damage. Long exposure to maximum ratings may affect device reliability. Functional operation at any other conditions from those indicated in the operational section may affect devices performance and reliability.

**Table 1:** Absolute maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
VCCA analog supply voltage	V <sub>CCA</sub>	AGND - 0.3	3.8	V
VCCIOx output supply voltage	V <sub>CCIOx</sub>	GNDIO - 0.3	3.8	V
VCCD digital supply voltage	V <sub>CCD</sub>	DGND - 0.3	3.8	V
Analog input swing (mode ON)	AIN <sub>p</sub> - AIN <sub>N</sub>  ,  BIN <sub>p</sub> - BIN <sub>N</sub>		4.8	V <sub>ppd</sub>
Analog input swing (mode OFF)	AIN <sub>p</sub> - AIN <sub>N</sub>  ,  BIN <sub>p</sub> - BIN <sub>N</sub>		1.2	V <sub>ppd</sub>
Analog input voltage	AIN <sub>p</sub> , AIN <sub>N</sub> , BIN <sub>p</sub> , BIN <sub>N</sub>	AGND - 0.3	3.6	V
Clock input swing (mode ON)	[CLK - CLKN]		4	V <sub>ppd</sub>
Clock input swing (mode OFF)	[CLK - CLKN]		1.2	V <sub>ppd</sub>
Clock input voltage	CLK, CLKN	AGND - 0.3	3.75	V
SYNC input voltage	SYNC, SYNCN	AGND - 0.3	VCCA + 0.3	V
SYNC input swing (mode ON)	SYNC - SYNCN		4	V <sub>ppd</sub>
SYNC input swing (mode OFF)	SYNC - SYNCN		1.2	V <sub>ppd</sub>
SPI input voltage	RSTN, SCLK, CSN, MOSI	DGND - 0.3	VCCD + 0.3	V
VDIODEA input voltage	DIODEA	-0.9	0.3	V

Notes: For cold sparing application, see application note AN1200A.

**Table 2:** Absolute maximum ratings (ESD and temperature)

Parameter	Symbol	Value	Unit
Electrostatic discharge (HBM)	ESD HBM	750V	V
ESD classification		CLASS 1B	
Absolute Max junction temperature	T <sub>JMAX</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-65 to +150	°C

Notes: All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damages caused by inappropriate handling or storage could range from performance degradation to complete failure.

### 3.2 Recommended conditions of use

**Table 3:** Recommended conditions of use

Parameter	Symbol	Value	Unit
VCCA analog supply voltage	$V_{CCA}$	3.4	V
VCCIOx output supply voltage 1	$V_{CCIOx1}$	3.4 or 2.5	V
VCCIOx output supply voltage 2	$V_{CCIOx2}$	3.4	V
VCCD digital supply voltage	$V_{CCD}$	3.4 or 2.5	V
External clock frequency	$F_C$	$\leq 3.2$	GHz
Differential analog input full scale swing	$ AIN_P - AIN_N ,$ $ BIN_P - BIN_N $	1.0	Vppd
Differential analog input full scale power	$P_A, P_B$	1	dBm
Differential clock input power	$P_{CLK}$	1	dBm
SPI input voltage	$V_{IL}$	0	V
	$V_{IH}$	VCCD	V

Notes:  $V_{CCIOx1} = 2.5V$  and  $V_{CCD} = 2.5V$  can be used to reduce power consumption. Refer to Table 18 in section [DEMUX 1:1 or 1:2](#) for more information.

**Table 4:** Recommended case (Tc) and junction (Tj) temperature conditions of use

Parameter	Symbol	Value	Unit
Operating temperature range (life time < 10 years)	Tc; Tj	$-55 < T_c ; T_j < +125$	°C
Operating temperature range ( life time < 17 years)	Tc; Tj	$-55 < T_c ; T_j < +110$	°C

Notes: Tj refers to the hot spot junction temperature on the die.

### 3.3 Explanation of test levels

**Table 5:** Explanation of test levels

Test level	Comment
1A	100% tested over specified temperature range and specified power supply range
1B	100% tested over specified temperature range at typical power supplies
1C	100% tested at +25°C over specified supply range
1D	100% tested at +25°C at typical power supplies
2	100% production tested at +25°C and samples tested at specified temperatures.
3	Samples tested only at specified temperatures
4	Parameter value is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design

Only MIN and MAX values are guaranteed

### 3.4 Electrical characteristics for supplies, inputs and outputs

Unless otherwise specified:

- Values are given for typical supplies in single-rail configuration (Refer to Table 18 in section [DEMUX 1:1 or 1:2](#) for more information) at Tamb = +25°C; Value between brackets represents value versus temperature.
- Values are given with SDA disabled and reduced swing mode.
- Sampling frequency (Fs) at 1.5 Gsps.

**Table 6:** Electrical characteristics for supplies, inputs and outputs

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
Resolution			12			bit	
<b>POWER REQUIREMENTS</b>							
Power supply voltage	1A	<ul style="list-style-type: none"> <li>Analog</li> </ul> $V_{CCA}$	3.25	3.4	3.55	V	(1)
<ul style="list-style-type: none"> <li>Output</li> </ul>		$V_{CCIOx1}$ 3.4V	3.25	3.4	3.55	V	
		$V_{CCIOx1}$ 2.5V	2.35	2.5	2.65	V	
<ul style="list-style-type: none"> <li>Digital</li> </ul>		$V_{CCIOx2}$	3.25	3.4	3.55	V	
		$V_{CCD}$ 3.4V	3.25	3.4	3.55	V	
		$V_{CCD}$ 2.5V	2.35	2.5	2.65	V	
Power supply current in DMUX 1:1	1A	<ul style="list-style-type: none"> <li>Analog, VCCA = 3.4V</li> </ul> $I_{CCA}$	950 (930)	1044	1110 (1200)	mA	(2)
<ul style="list-style-type: none"> <li>Output 2</li> </ul> Reduced swing, VCCIOH2 = 3.4V		$I_{CCO2}$	50 (40)	63	75 (90)	mA	
		<ul style="list-style-type: none"> <li>Output 1</li> </ul> Reduced swing, VCCIOH1 = 2.5V Reduced swing, VCCIOH1 = 3.4V	$I_{CCO1}$	80 (63)	100	120 (150)	
<ul style="list-style-type: none"> <li>Digital</li> </ul> VCCD = 3.4V VCCD = 2.5V			$I_{CCD}$	140 (130)	173	190 (200)	
		$I_{CCD}$	130 (120)	170	185 (195)	mA	
Power supply current in DMUX 1:2		1A	<ul style="list-style-type: none"> <li>Analog, VCCA = 3.4V</li> </ul> $I_{CCA}$	950 (930)	1045	1110 (1200)	
<ul style="list-style-type: none"> <li>Output 2</li> </ul> Reduced swing, VCCIOH2 = 3.4V Reduced swing, VCCIOH2 = 3.4V	$I_{CCO2}$		30 (20) 50 (40)	37 64	45 (60) 75 (90)	mA	
	<ul style="list-style-type: none"> <li>Output 1</li> </ul> Reduced swing, VCCIOH1 = 2.5V Reduced swing, VCCIOH1 = 2.5V		$I_{CCO1}$	50 (40) 80 (63)	74 100	90 (100) 120 (150)	mA
<ul style="list-style-type: none"> <li></li> </ul> Reduced swing, VCCIOH1 = 3.4V Reduced swing, VCCIOH1 = 3.4V			$I_{CCO1}$	55 (40) 80 (60)	77 104	90 (100) 120 (153)	mA
	<ul style="list-style-type: none"> <li>Digital</li> </ul> VCCD = 3.4V VCCD = 2.5V		$I_{CCD}$	120 (100)	155	175 (185)	mA
$I_{CCD}$			115 (95)	148	170 (180)	mA	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
Power supply current in full standby mode	1A	<ul style="list-style-type: none"> <li>Analog <math>I_{CCA}</math></li> <li>Output (DMUX 1:1) <math>I_{CCO}</math></li> <li>Output (DMUX 1:2) <math>I_{CCO}</math></li> <li>Digital <math>I_{CCD}</math></li> </ul>	310 (300)	334	360 (400)	mA	(2)
			155 (140)	168	190 (235)	mA	
			250 (200)	278	310 (470)	mA	
			45 (40)	72	85 (94)	mA	
Power dissipation (VCCA = VCCD = VCCIOxx = 3.4V)	1A	$P_D$		4.7	5.0 (5.3)	W	(2)
<ul style="list-style-type: none"> <li>DEMUX1:1 - Reduced swing</li> <li>DEMUX1:2 - Reduced swing</li> </ul>				5.0	5.3 (5.7)	W	
Power dissipation (VCCA = VCCIOx2 = 3.4V, VCCD = VCCIOx1 = 2.5V)	1A	$P_D$		4.4	4.7 (5.0)	W	(2)
<ul style="list-style-type: none"> <li>DEMUX1:1 - Reduced swing</li> <li>DEMUX1:2 - Reduced swing</li> </ul>				4.7	5 (5.3)	W	
Power dissipation in full standby mode (VCCA = VCCD = VCCIOxx = 3.4V)	1A	$P_D$		1.6	2.1 (2.2)	W	(2)
<ul style="list-style-type: none"> <li>DEMUX1:1</li> <li>DEMUX1:2 -</li> </ul>				1.9	2.5 (2.6)	W	
<b>ANALOG INPUTS</b>							
Analog input coupling			AC or DC				(3)
Analog input common mode voltage	4	$V_{INCM}$		2.4		V	(4)
Analog differential input full scale voltage	4	$ A_{INp} - A_{INn} $ , $ B_{INp} - B_{INn} $			1	Vppd	
Analog differential input full scale power (100Ω differential termination)	4	$P_{IN}$			1	dBm	
Analog input leakage current	5	$I_{IN}$		40		μA	
Analog input resistance	4	$R_{IN}$	80	100	120	Ω	(5)
<ul style="list-style-type: none"> <li>Without trimming</li> <li>With trimming</li> </ul>			95	100	105	Ω	
Crosstalk between analog inputs	4	Xtalk		80		dB	(6)
<b>CLOCK INPUTS</b>							
Clock common mode voltage	4	$V_{CCM}$	2.40	2.57	2.75	V	
Clock differential input power (100Ω differential termination)	4	$P_{CLK}$	-3	1	7	dBm	
Clock input capacitance (including die and package)	5	$C_{CLK}$		1		pf	
Clock differential input resistance	4	$R_{CLK}$	80	100	120	Ω	
Clock slew rate		$SR_{CLK}$	8	12		GV/s	
Clock jitter (3GHz sine wave) Integrated from 10MHz to 10GHz		Jitter			100	$fs_{rms}$	
Intrinsic clock jitter	5	Intrinsic jitter		135		$fs_{rms}$	
<ul style="list-style-type: none"> <li>- SDA off</li> <li>- SDA on</li> </ul>				200			
Clock duty cycle	4	Duty cycle	45	50	55	%	
<b>SYNCTRIG INPUTS</b>							
SYNCTRIG common mode voltage	1B	$V_{ICM}$	1.125	1.25	1.8	V	
SYNCTRIG differential swing	1B	$V_{IH} - V_{IL}$	100	350	450	mVp	
SYNCTRIG input capacitance	5	$C_{SYNC}$		1		pf	
SYNCTRIG input resistance	4	$R_{SYNC}$	80	100	120	Ω	
SYNCTRIG slew rate	5	$SR_{SYNC}$	500			MV/s	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
<b>SPI INPUTS (RSTN, SCLK, CSN, MOSI)</b>							
CMOS Schmitt trigger low level threshold	1C	$V_{IL}$			$0.3V_{CCD}$	V	
CMOS Schmitt trigger high level threshold	1C	$V_{IH}$	$0.6V_{CCD}$			V	
CMOS Schmitt trigger hysteresis	5	$V_{th}$	$0.1V_{CCD}$			V	
CMOS low level input current	5	$I_{IL}$			300	nA	
CMOS high level input current	5	$I_{IH}$			1000	nA	
<b>SPI OUTPUT (MISO)</b>							
CMOS low level output voltage	1C	$V_{OL}$			$0.2V_{CCD}$	V	
CMOS high level output voltage	1C	$V_{OH}$	$0.8V_{CCD}$			V	
<b>LVDS OUTPUT</b>							
Full swing - Common mode voltage - Swing - Logic low - Logic high	4	$VO_{CM}$	1.2	1.36	1.55	V	(7)
		$V_{OH} - V_{OL}$	230	320	480	mVp	
		$V_{OL}$			1.30	V	
		$V_{OH}$	1.40			V	
Reduced swing - Common mode voltage - Swing - Logic low - Logic high	1B	$VO_{CM}$	1.2	1.36	1.55	V	
		$V_{OH} - V_{OL}$	200	290	350	mVp	
		$V_{OL}$			1.40	V	
		$V_{OH}$	1.35			V	

- Notes:
1. Refer to Table 18 in section [DEMUX 1:1 or 1:2](#) for more information on power supplies management.
  2. Enabling SDA increases power consumption by 80mW (23mA on VCCA).
  3. The DC analog common mode voltage is provided by the CMIREF output of the ADC.
  4. See section [Input common mode trimming](#) for more information on the range available.
  5. For optimal performance, in terms of VSWR, the input impedance must be  $100\Omega \pm 5\%$  and the analog input impedance must be digitally trimmed to cope with process deviation. Refer to section [Input impedance trimming](#) for more information.
  6. Refer to Figure 21 in section [Characterization results](#) for more results on the crosstalk performance.
  7. The full swing mode will increase respectively  $I_{CCO1}$  by 50mA in DMUX1:1 and by 80mA in DMUX1:2.



### 3.5 Converter characteristics

Unless otherwise specified:

- Values are given for typical supplies in single-rail configuration (Refer to Table 18 in section [DEMUX 1:1 or 1:2](#) for more information) at  $T_{amb} = +25^{\circ}\text{C}$ ; Value between brackets represents value versus temperature.
- Values are given with SDA disabled and reduced swing mode.
- Sampling frequency ( $F_s$ ) at 1.5Gsps.
- Both cores comply with the below specification when the OTP have been loaded.

**Table 7:** Static characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
DC accuracy / $F_s = 1.5\text{Gsps}$ , $F_{in} = 100\text{MHz}$ , $-1\text{dBFS}$							
Gain variation	5	$G_0$	-1.5	0	1.5	dB	(1)
Gain variation versus temperature	4	$G(T)$	-0.5	0	0.5	dB	
DC offset	1B		2045	2048	2051	LSB	(2)
			No missing code				
Differential Non Linearity	4	DNL	-0.9		+1.5	LSB	
DNL rms	4	DNLrms		0.2	0.5	LSB	
Integral Non Linearity	1B	INL	-6.5		6.5	LSB	
INL rms	1B	INLrms		0.6	1.6	LSB	

Notes: 1. This value corresponds to the maximum deviation from part to part.

2. Mid code at ADC output after DC offset calibration.

**Table 8:** Dynamic characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
<b>ANALOG INPUT</b>							
Full power input bandwidth							
<ul style="list-style-type: none"> <li>Nominal bandwidth (NBW)</li> </ul>	4			3.7		GHz	(1)
<ul style="list-style-type: none"> <li>Extended bandwidth (EBW)</li> </ul>	4			4.3		GHz	
Gain flatness (+/- 0.5dB)							
<ul style="list-style-type: none"> <li>Nominal bandwidth (NBW)</li> </ul>	4			900		MHz	
<ul style="list-style-type: none"> <li>Extended bandwidth (EBW)</li> </ul>	4			1000		MHz	
Input voltage standing wave ratio							
<ul style="list-style-type: none"> <li>Up to 2.4GHz</li> </ul>	4	VSWR		1.2:1	1.28:1		
<ul style="list-style-type: none"> <li>Up to 5GHz</li> </ul>	4			2:1			
<b>DYNAMIC PERFORMANCE</b>							
Noise Power Ratio (600MHz noise bandwidth, 5MHz notch centered at $F_s/4$ )							
<ul style="list-style-type: none"> <li>1<sup>st</sup> Nyquist zone</li> </ul>	4	NPR		50		dB	(2)
<ul style="list-style-type: none"> <li>2<sup>nd</sup> Nyquist zone</li> </ul>	4			47		dB	
<ul style="list-style-type: none"> <li>3<sup>rd</sup> Nyquist zone</li> </ul>	4			46		dB	
<ul style="list-style-type: none"> <li>4<sup>th</sup> Nyquist zone</li> </ul>	4			45		dB	
<b>Spurious Free Dynamic Range</b>							
Output level $-1\text{dBFS}$							
<ul style="list-style-type: none"> <li><math>F_{in} = 100\text{MHz}</math>, NBW</li> </ul>	4	SFDR		76		dBFS	(3)

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
• Fin = 1480MHz, NBW	4			70		dBFS	
• Fin = 1900MHz, NBW	4			68		dBFS	
Output level -3dBFS							
• Fin = 100MHz, NBW	4			77		dBFS	
• Fin = 1480MHz, NBW	4			70		dBFS	
• Fin = 1900MHz, NBW	4			69		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW	4			74		dBFS	
• Fin = 1480MHz, NBW	4			74		dBFS	
• Fin = 1900MHz, NBW	1B		69 (66)	75 (73)		dBFS	(3)
• Fin = 2980MHz, EBW	1B		64 (63)	73 (68)		dBFS	
• Fin = 3730MHz, EBW	4	SFDR		62		dBFS	
• Fin = 5300MHz, out-of-band	4			51		dBFS	
Output level -12dBFS							
• Fin = 100MHz, NBW	4			77.5		dBFS	
• Fin = 1480MHz, NBW	4			74		dBFS	
• Fin = 1900MHz, NBW	1B		66 (64)	76 (72)		dBFS	
• Fin = 2980MHz, EBW	1B		67 (63)	77 (71)		dBFS	
• Fin = 3730MHz, EBW	4			68		dBc	
• Fin = 5300MHz, out-of-band	4			59		dBFS	
<b>3rd order highest intermodulation products</b>		IMD3					(3)
Fin = 374MHz & ΔFin = 5MHz / -7dBFS	4			78.5		dBFS	
Fin = 1024MHz & ΔFin = 5MHz / -7dBFS	4			72.7		dBFS	
Fin = 1870MHz & ΔFin = 5MHz / -7dBFS	4			69.2		dBFS	
Fin = 2620MHz & ΔFin = 5MHz / -9dBFS	4			71.6		dBFS	
<b>Total Harmonic Distortion</b>							
Output level -1dBFS							
• Fin = 100MHz, NBW	4			68		dBFS	
• Fin = 1480MHz, NBW	4			65		dBFS	
Output level -3dBFS							
• Fin = 100MHz, NBW	4			71		dBFS	
• Fin = 1480MHz, NBW	4			67		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW	4			69		dBFS	
• Fin = 1480MHz, NBW	4	THD		69		dBFS	(3)
• Fin = 1900MHz, NBW	1B		63 (61)	69 (67)		dBFS	
• Fin = 2980MHz, EBW	1B		62 (58)	68 (63)		dBFS	
• Fin = 3730MHz, EBW	4			60		dBFS	
• Fin = 5300MHz, out-of-band	4			48		dBFS	
Output level -12dBFS							
• Fin = 100MHz, NBW	4			71		dBFS	
• Fin = 1480MHz, NBW	4			70		dBFS	
• Fin = 1900MHz, NBW	1B		62 (59)	70 (66)		dBFS	
• Fin = 2980MHz, EBW	1B		62 (60)	70 (66)		dBFS	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
• Fin = 3730MHz, EBW	4			65		dBFS	
• Fin = 5300MHz, out-of-band	4			55		dBFS	
<b>Signal to Noise Ratio</b>							
Output level -1dBFS							
• Fin = 100MHz, NBW	4	SNR		58		dBFS	
• Fin = 1480MHz, NBW	4			56.5		dBFS	
Output level -3dBFS							
• Fin = 100MHz, NBW	4			58.5		dBFS	
• Fin = 1480MHz, NBW	4			57.5		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW	4			59			
• Fin = 1480MHz, NBW	4			58.5			
• Fin = 1900MHz, NBW	1B		57 (55)	58 (57)			
• Fin = 2980MHz, EBW	1B		54.5 (53.5)	56 (55.5)			
• Fin = 3730MHz, EBW	4	SNR		55.5			
• Fin = 5300MHz, out-of-band	4			54			
Output level -12dBFS							
• Fin = 100MHz, NBW	4			59		dBFS	
• Fin = 1480MHz, NBW	4			59		dBFS	
• Fin = 1900MHz, NBW	1B		57 (55.5)	59 (57.5)		dBFS	
• Fin = 2980MHz, EBW	1B		55.5 (54)	57 (56.5)		dBFS	
• Fin = 3730MHz, EBW	4			56		dBFS	
• Fin = 5300MHz, out-of-band	4			55		dBFS	
<b>Signal to Noise And Distortion</b>							
Output level -1dBFS							
• Fin = 100MHz, NBW	4			58		dBFS	
• Fin = 1480MHz, NBW	4			56		dBFS	
Output level -3dBFS							
• Fin = 100MHz, NBW	4			58.5		dBFS	
• Fin = 1480MHz, NBW	4			56.5		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW	4			58.5			
• Fin = 1480MHz, NBW	4			58			
• Fin = 1900MHz, NBW	1B	SINAD	56 (54)	58 (56.5)			
• Fin = 2980MHz, EBW	1B		54 (51)	56 (54)			
• Fin = 3730MHz, EBW	4			55			
• Fin = 5300MHz, out-of-band	4			49			
Output level -12dBFS							
• Fin = 100MHz, NBW	4			58.5		dBFS	
• Fin = 1480MHz, NBW	4			58.5		dBFS	
• Fin = 1900MHz, NBW	1B		56.5 (54)	58.5 (57)		dBFS	
• Fin = 2980MHz, EBW	1B		55 (53)	57 (55.5)		dBFS	
• Fin = 3730MHz, EBW	4			56		dBFS	
• Fin = 5300MHz, out-of-band	4			54		dBFS	

Parameter	Test level	Symbol	Value			Unit	Note	
			Min	Typ	Max			
<b>Effective Number Of Bits</b>								
Output level -1dBFS								
• Fin = 100MHz, NBW	4	ENOB		9.4		bit FS		
• Fin = 1480MHz, NBW	4			9.0		bit FS		
Output level -3dBFS								
• Fin = 100MHz, NBW	4			9.4		bit FS		
• Fin = 1480MHz, NBW	4			9.2		bit FS		
Output level -8dBFS								
• Fin = 100MHz, NBW	4			9.5		bit FS		
• Fin = 1480MHz, NBW	4			9.4		bit FS		
• Fin = 1900MHz, NBW	1B			9 (8.8)	9.3 (9.1)	bit FS		
• Fin = 2980MHz, EBW	1B			8.8 (8.4)	9.0 (8.7)	bit FS		
• Fin = 3730MHz, EBW	4				8.5	bit FS		
• Fin = 5300MHz, out-of-band	4				7.5	bit FS		
Output level -12dBFS								
• Fin = 100MHz, NBW	4				9.5	bit FS		
• Fin = 1480MHz, NBW	4				9.5	bit FS		
• Fin = 1900MHz, NBW	1B			9.1 (8.7)	9.4 (9.2)	bit FS		
• Fin = 2980MHz, EBW	1B		9 (8.6)	9.2 (9.0)	bit FS			
• Fin = 3730MHz, EBW	4			9.0	bit FS			
• Fin = 5300MHz, out-of-band	4			8.5	bit FS			
<b>Noise Spectral density at -1dBFS</b>								
• 1 <sup>st</sup> Nyquist zone, NBW	4	NSD		-147		dBm/Hz		
• 2 <sup>nd</sup> Nyquist zone, NBW	4			-145		dBm/Hz		
• 3 <sup>rd</sup> Nyquist zone, EBW	4			-144		dBm/Hz		
• 4 <sup>th</sup> Nyquist zone, EBW	4			-141		dBm/Hz		
<b>Noise Spectral density at -8dBFS</b>								
• 1 <sup>st</sup> Nyquist zone, NBW	4				-147	dBm/Hz		
• 2 <sup>nd</sup> Nyquist zone, NBW	4				-146	dBm/Hz		
• 3 <sup>rd</sup> Nyquist zone, EBW	4				-146	dBm/Hz		
• 4 <sup>th</sup> Nyquist zone, EBW	4			-144	dBm/Hz			

Notes: 1. Optimal bandwidth selection depends on signal characteristic; the bandwidth selection allows optimizing noise and linearity trade-off. For signal below 2.0GHz, the bandwidth selection must be set to nominal, for large signal beyond 2GHz the bandwidth selection must be set to extended. The extended bandwidth degrades noise floor up to 1dB, but brings lower signal attenuation with high frequency input.

2. The values indicated in this table indicate the NPR value obtained at optimum loading factor value.

3. Linearity at high frequency is dominated by low order odd harmonics (especially H3). Phase difference on the differential inputs should be reduced as much as possible to optimize the 2<sup>nd</sup> harmonic (H2) level. Stepping back 3 or 6 dB on input signal gives significant improvement on SFDR figures.

### 3.6 Transient and switching characteristics

Unless otherwise specified:

- Typical values are given for typical supplies in dual-rail configuration (Refer to Table 18 in section [DEMUX 1:1 or 1:2](#) for more information) at Tamb = +25°C.
- Both cores comply with the below specification when the OTP have been loaded.
- Values are specified at Fs = 1.5GSps.
- Values are given with SDA disabled.

**Table 9:** Transient characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
ADC Code Error Rate at 1.5 GSps (3GHz CLK)	4	CER		10 <sup>-12</sup>			(1)
ADC Code error rate at 1.25 GSps (2.5GHz CLK)	4	CER		10 <sup>-15</sup>			(2)
Overvoltage Recovery Time	4	ORT		666		ps	

Notes: 1. Output error amplitude > 128 LSB (3% of the full-scale). At Fs = 1.5 GSps, ambient temperature.  
2. Output error amplitude > 64 LSB (1.5% of the full-scale). At Fs = 1.25 GSps, ambient temperature.

**Table 10:** Switching characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
External clock frequency	4	F <sub>CLK</sub>	400		3200	MHz	
Sampling frequency for performance							
• DEMUX 1:1	4	F <sub>S1:1</sub>	200		1500	MSps	(1)
• DEMUX 1:2		F <sub>S1:2</sub>	200		1600	MSps	
Sampling frequency for operation							
• DEMUX 1:1	4	F <sub>S1:1</sub>	200		1500	MSps	(1)
• DEMUX 1:2	4	F <sub>S1:2</sub>	200		1600	MSps	
Aperture delay (SDA disabled)	4	T <sub>A</sub>		135		ps	
Aperture delay tuning range (SDA enabled)	4	T <sub>A</sub>	120	175		ps	
<b>LVDS OUTPUT</b>							
Rise time for data (20-80%)	4	T <sub>R</sub>		165		ps	(1), (2)
Fall time for data (20-80%)	4	T <sub>F</sub>		165		ps	(1), (2)
Rise time for data ready (20-80%)	4	T <sub>R</sub>		135		ps	(1), (2)
Fall time for data ready (20-80%)	4	T <sub>F</sub>		135		ps	(1), (2)
Output data pipeline delay (latency)							
• Port high	4	T <sub>PDH</sub>		22		T <sub>CLK</sub>	(3)
• Port low	4	T <sub>PDL</sub>		20		T <sub>CLK</sub>	
Output data propagation delay	4	T <sub>OD</sub>		2.5		ns	(3)
Output data to data ready delay in DMUX1:1	4	T <sub>D1</sub>		1		T <sub>CLK</sub>	(3)
DMUX1:2				2			
Output data ready to data delay in DMUX1:1	4	T <sub>D2</sub>		1		T <sub>CLK</sub>	(3)
DMUX1:2				2			
Output data ready A to data ready B skew	4	T <sub>DRsk</sub>		43		ps	
Output data skew within 1 port reference to data ready	4	T <sub>dxsk</sub>	-23		+14.5		
SYNC to data ready pipeline delay	4						

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
• DEMUX 1:1	4	$T_{RDR}$		26		$T_{CLK}$	(4)
• DEMUX 1:2	4	$T_{RDR}$		27		$T_{CLK}$	
SYNC pulse width	4	$T_{SYNC}$	16			$T_{CLK}$	
SYNC to SYNCO pipeline delay	4	$T_{PS}$		1		$T_{CLK}$	
SYNC to SYNCO propagation delay	4	$T_{ODS}$		1		ns	
SYNC signal valid timing	4	$T_1$ $T_2$		140 125		ps ps	(5)
Trigger data pipeline delay							
• Core A high	4	$T_{PDA}$		22		$T_{CLK}$	(6)
• Core B	4	$T_{PDB}$		23		$T_{CLK}$	
TRIG propagation delay	4	$T_{ODT}$		4.34		ns	

- Notes: 1. Performance only guaranteed at 1.5 GSps max in DEMUX 1:2 mode and 1.3 GSps max in DEMUX 1:1 mode although devices still exhibit very good performance at 1.6Gsps.  
 2. Simulated with 50Ω lines modeled by 2.5nH in parallel with 1pF.  
 3. Refer to timing diagrams in Figure 3 and 4.  
 4. Refer to timing diagram in Figure 5.  
 5. Refer to timing diagram in Figure 6. T1 and T2 correspond to setup and hold times of the SYNCTRIG input seen at the package input.  
 6. Measured in interleaved mode.

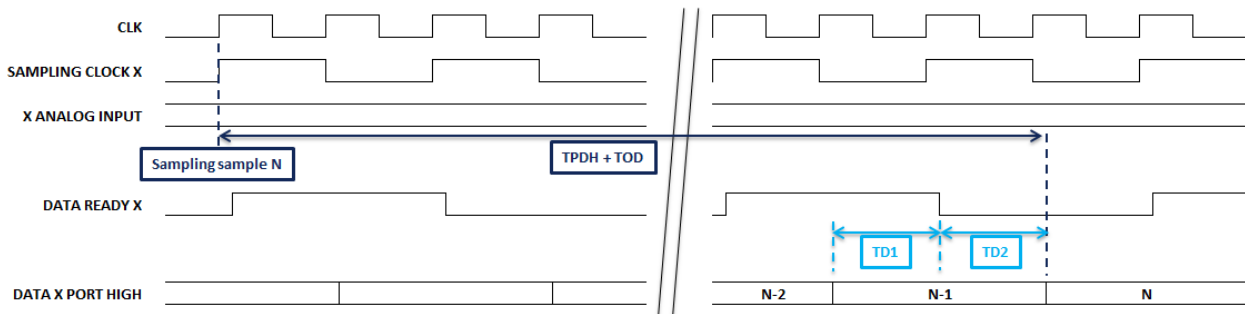


Figure 3: Timing diagram in DEMUX 1:1

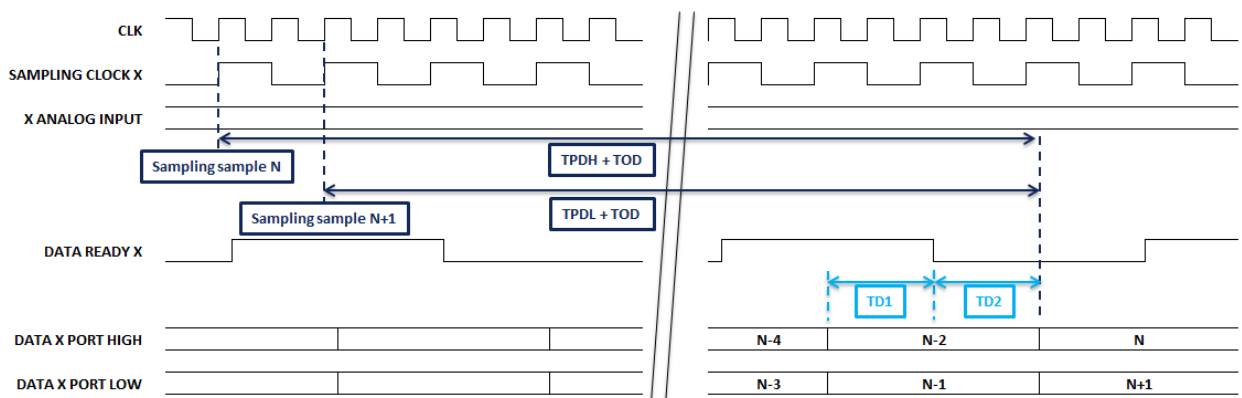


Figure 4: Timing diagram in DEMUX 1:2

For both figures 3 and 4, X represents either channel A or B. If channel A and B are interleaved, the internal sampling clocks of channel A and B are in opposition and their output data and data ready are delayed by 1 external CLK cycle.

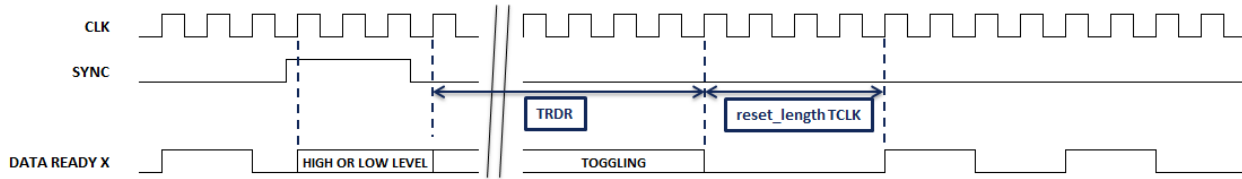


Figure 5: SYNC timing diagram in DEMUX 1:1

Notes: In DEMUX 1:2 the only difference from the timing diagram above is the frequency of the data ready.

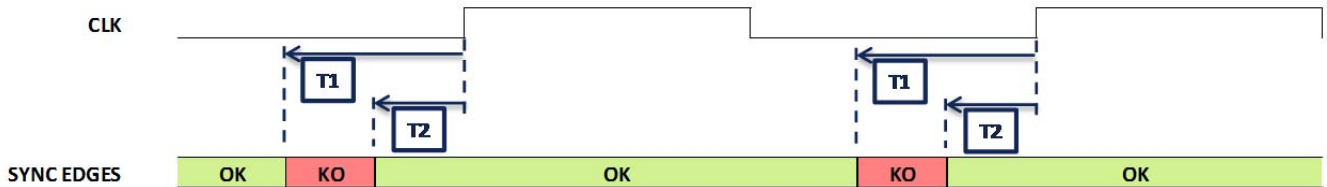


Figure 6: SYNC edges forbidden zone

Notes: The timing diagram assumes that bit ESEL in register SYNC control is at '0'. If ESEL = '1', T1 and T2 have to be referenced to the falling edge of CLK. See section [SYNCTRIG input](#) for more information.

Table 11: SPI switching characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
RSTN pulse length	5	$T_{RSTN}$	10			$\mu s$	
SCLK frequency	5	$F_{SCLK}$			30	MHz	
CSN to SCLK delay	5	$T_{CSN-SCLK}$	0.5			$T_{SCLK}$	(1)
MOSI setup time	5	$T_{setup}$	3			ns	(1,2)
MOSI hold time	5	$T_{hold}$	3			ns	(1,2)
MISO output delay	5	$T_{delay}$			4	ns	(1,2,3)

Notes:

1. Refer to timing diagram in Figure 7.
2. ADC is considered as the slave.
3. Taking into account 5pF as load.

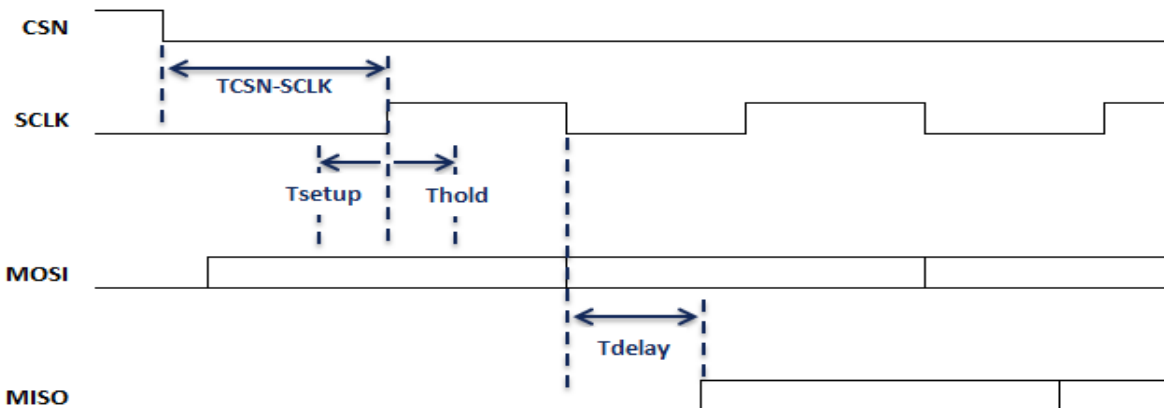


Figure 7: SPI timing diagram

### 3.7 Digital output coding

Table 12: ADC digital output coding table

Differential analog input	Voltage level	Binary MSB (bit 11).....LSB(bit 0) In-range
> +499.756 mV	> Top end of full scale	1111 1111 1111 0
+499.756 mV +499.512 mV	Top end of full scale Top end of full scale -1 LSB	1111 1111 1111 1 1111 1111 1110 1
0 mV -0.244 mV	Mid-scale Mid-scale – 1 LSB	1000 0000 0000 1 0111 1111 1111 1
-499.756 mV -500 mV	Bottom of full scale + 1 LSB Bottom of full scale	0000 0000 0001 1 0000 0000 0000 1
< -500 mV	< Bottom of full scale	0000 0000 0000 0

### 3.8 Characterized radiation level

<b>TID</b>	150Krad(Si) at Low Dose Rate (36rad(Si)/h, 10mrad(Si)/s)
<b>SEE</b>	SEL and SEFI immune up to a LET of 80MeV.cm <sup>2</sup> /mg (No tilt)

### 3.9 Definition of terms

Table 13: Definition of terms

Abbreviation	Term	Definition
CER	<i>Code Error Rate</i>	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate.
DNL	<i>Differential non-linearity</i>	The Differential Non Linearity for an output code “i” is the difference between the measured step size of code “i” and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification higher than -1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
ENOB	<i>Effective Number Of Bits</i>	$\text{ENOB} = \frac{\text{SINAD} - 1.76 + 20 \log (A / \text{FS}/2)}{6.02}$ Where A is the input amplitude and FS is the full scale range of the ADC under test.
FPBW	<i>Full Power Input Bandwidth</i>	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at -1dBFS (Full scale – 1dB).
IMD3	<i>Intermodulation Distortion</i>	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
INL	<i>Integral non-linearity</i>	The Integral Non Linearity for an output code “i” is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all  INL (i) .
JITTER	<i>Aperture uncertainty</i>	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
LF	<i>Loading Factor</i>	The loading factor is 20log(1/k), where k is the rms value of the broadband signal. This parameter relates to the NPR measurement. The optimum loading factor for a 12bits converter is k = 5 corresponding to a loading factor of -14dB.
NPR	<i>Noise Power Ratio</i>	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC



Abbreviation	Term	Definition
		under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
NSD	<i>Noise Spectral Density</i>	The NSD is the power spectral density magnitude of the ADC expressed in dBm/Hz.
ORT	<i>Overvoltage Recovery Time</i>	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
OTP	<i>One Time Programmable</i>	OTP are fuses used to set circuit default configuration and calibrations.
SFDR	<i>Spurious Free Dynamic Range</i>	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SINAD	<i>Signal to Noise And Distortion ratio</i>	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SNR	<i>Signal to Noise Ratio</i>	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the 25 <sup>th</sup> first harmonics. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
T1, T2	<i>SYNC forbidden zone</i>	T1 and T2 represents setup and hold time on the SYNC input brought back to the input of the package.
TA	<i>Aperture delay</i>	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (XAI, XAIN where X = A, B) is sampled.
TF	<i>Fall time</i>	Time delay for the output DATA signals to fall from 20% to 80% of delta between high level and low level.
THD	<i>Total Harmonic Distortion</i>	Ratio expressed in dB of the RMS sum up to 25 <sup>th</sup> harmonic components, to the RMS input signal amplitude. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
TOD	<i>Digital data output delay</i>	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
TPD	<i>Pipeline delay / latency</i>	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking into account TOD).
TR	<i>Rise time</i>	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
TRDR	<i>Data ready reset delay</i>	Delay between the edge of the external clock after reset (SYNC, SYNCN) and the reset to digital zero transition of the data ready output signal (XDR, where X = A, B)?
TSYNC	<i>SYNC duration</i>	External SYNC pulse width needed for SYNC function.
VSWR	<i>Voltage Standing Wave Ratio</i>	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e. 99% power transmitted and 1% reflected).

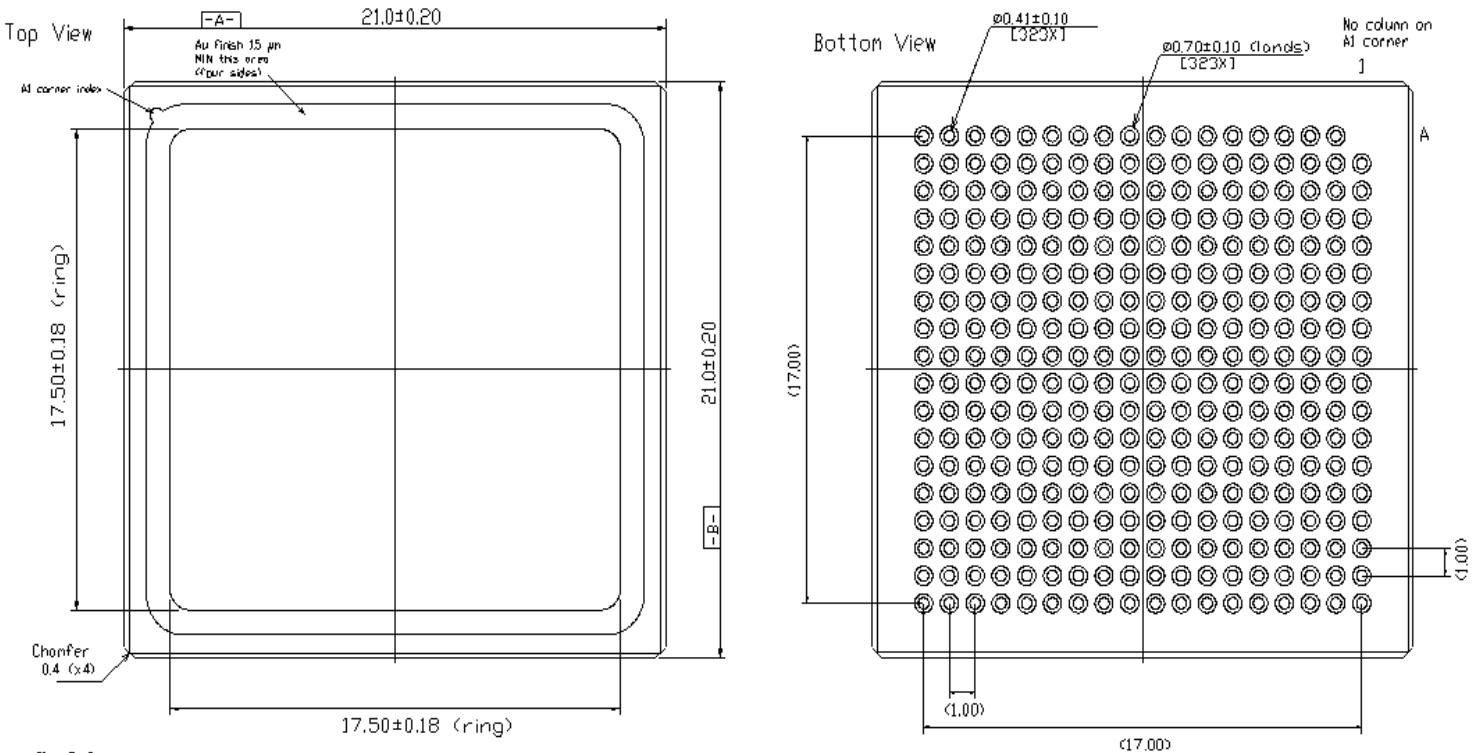
4 Package description

Hermetic Ceramic Column Grid Array CCGA323  
 Body size: 21mmx21mm  
 Mass: 7g including columns  
 Substrate type: Aluminum nitride (AlN)

Lid: Kovar polarized at AGND  
 Pitch: 1.0mm  
 Pins count: 323

4.1 Package Drawings

Figure 8: Package drawings

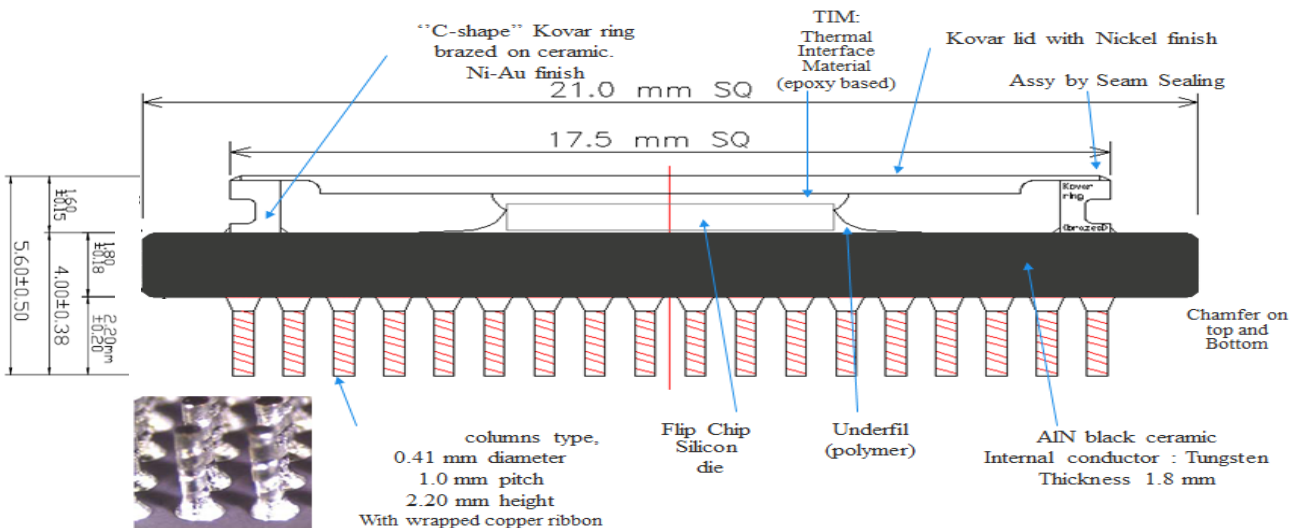


e2v

Note1  
 Initial column core composition (prior to column wire manufacturing): Sn15–Pb85 (wt %).  
 Final column core composition (after column attach on CLGA packages): 55 ≤ Pb wt% ≤ 85

All units in mm

Figure 9: Package cross-section



## 4.2 Thermal characteristics

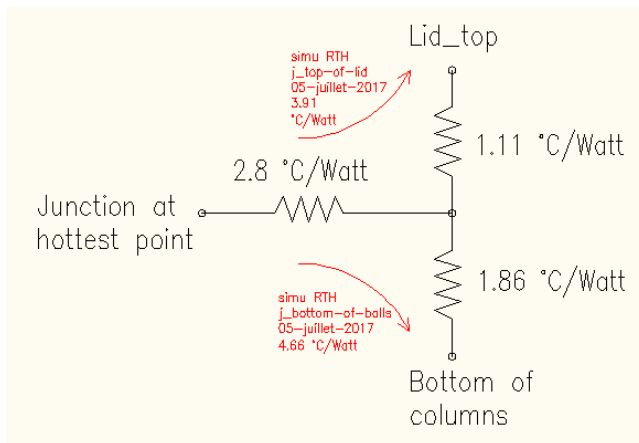
**Table 14:** Package thermal characteristic

Parameter	Symbol	Value	Unit	Note
Thermal Resistance	$\Theta_{\text{Junction-Bottom of columns}}$	4.7	°C/Watt	See note 1, 6
Thermal Resistance	$\Theta_{\text{Junction-top of lid}}$	3.9	°C/Watt	See note 2, 6
Thermal Resistance	$\Theta_{\text{Junction-Ambient}}$	17.5	°C/Watt	See note 3
Thermal Resistance	$\Theta_{\text{Junction-Board}}$	6.25	°C/Watt	See note 4
Delta Temp Hot Spot – Temp sensed by Vdiode		+10	°C	See note 5

Notes: Thermal resistances are calculated from hot spot, not from average temperature.

These figures are thermal simulation results (finite elements method in ANSYS) in nominal cases.

- Infinite heat sink at bottom of columns. No dissipation from lid top to external heatsink. 100% of thermal heat flux is between die and bottom of columns.
- Infinite heat sink at top of lid. No dissipation through columns. 100% of thermal heat flux is between die and top of lid.
- Typical Assumptions:
  - Convection according to JEDEC JESD51
  - Still air
  - Horizontal 2s2p board
  - Board size 114.3 × 76.2 mm, 1.6 mm thickness
- According to Jedec JESD51-8, 2s2p board. Board ref point is at middle of edge package footprint on board.
- Device has a diode as temperature sensor on die. Diode location is not at hot spot due to design constraints, thus Hot spots blocs have temperature higher than sensed at diode location.
- When both thermal path to top of lid and bottom-of-columns are used a three resistors model should be used:



4.3 Pinout top view

Figure 10: Pinout top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AGND	SYNC TRIGP	AGND	AGND	AGND	AGND	AGND	CLK N	CLK P	AGND	AGND	AGND	AGND	AGND	DIODE_C	AGND	AGND	A
B	AGND	AGND	SYNC TRIGN	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DIODE_A	AGND	AGND	B
C	SSO P	SSO N	AGND	AGND	AGND	AIN N	AIN P	AGND	AGND	AGND	AGND	BIN P	BIN N	AGND	AGND	AGND	SYNCO N	SYNCO P	C
D	AH11P	AH11N	AGND	AGND	CMIREFA	AGND	AGND	AGND	VCCA	VCCA	AGND	AGND	AGND	CMIREFB	AGND	AGND	BH11N	BH11P	D
E	AH10P	AH10N	AFU1P	AFU1N	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCA	VCCA	AGND	AGND	BFU1N	BFU1P	BH10N	BH10P	E
F	AH8P	AH8N	AH9P	AH9N	GNDIO	GNDIO	AGND	AGND	VCCA	VCCA	AGND	AGND	GNDIO	GNDIO	BH9N	BH9P	BH8N	BH8P	F
G	AH6P	AH6N	AH7P	AH7N	VCCIO H2A	GNDIO	VCCIO H2A	AGND	AGND	AGND	AGND	VCCIO H2B	GNDIO	VCCIO H2B	BH7N	BH7P	BH6N	BH6P	G
H	AH4P	AH4N	AH5P	AH5N	VCCIO H1A	GNDIO	VCCIO H1A	VCCA	AGND	AGND	VCCA	VCCIO H1B	GNDIO	VCCIO H1B	BH5N	BH5P	BH4N	BH4P	H
J	AH2P	AH2N	AH3P	AH3N	GNDIO	GNDIO	VCCIO H2A	AGND	VCCA	VCCA	AGND	VCCIO H2B	GNDIO	GNDIO	BH3N	BH3P	BH2N	BH2P	J
K	AH0P	AH0N	AH1P	AH1N	GNDIO	GNDIO	VCCIO H1A	VCCA	VCCD	GNDD	VCCA	VCCIO H1B	GNDIO	GNDIO	BH1N	BH1P	BH0N	BH0P	K
L	ADRP	ADRN	AFU2P	AFU2N	VCCIO L1A	GNDIO	VCCIO L1A	GNDIO	VCCD	GNDD	GNDIO	VCCIO L1B	GNDIO	VCCIO L1B	BFU2N	BFU2P	BDRN	BDRP	L
M	AL0P	AL0N	AL1P	AL1N	GNDIO	VCCIO L2A	GNDIO	VCCIO L2A	VCCIO L1A	VCCIO L1B	VCCIO L2B	GNDIO	VCCIO L2B	GNDIO	BL1N	BL1P	BL0N	BL0P	M
N	AL2P	AL2N	AL3P	AL3N	GNDIO	GNDIO	VCCIO L2A	GNDIO	GNDIO	GNDIO	GNDIO	VCCIO L2B	GNDIO	GNDIO	BL3N	BL3P	BL2N	BL2P	N
P	AL4P	AL4N	AL5P	AL5N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL5N	BL5P	BL4N	BL4P	P
R	AL6P	AL6N	AL7P	AL7N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL7N	BL7P	BL6N	BL6P	R
T	AL8P	AL8N	AL9P	AL9N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL9N	BL9P	BL8N	BL8P	T
U	AL10P	AL10N	AL11P	AL11N	GNDIO	TESTA	VCCFUSEC	GNDIO	GNDIO	GNDIO	GNDIO	SCLK	RSTN	GNDIO	BL11N	BL11P	BL10N	BL10P	U
V	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	SCAN	VCCFUSEB	VCCFUSEA	GNDIO	GNDIO	GNDIO	MISO	MOSI	CSN	GNDIO	GNDIO	GNDIO	GNDIO	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

4.4 Pinout table

Table 15: Pinout table

Pin label	Pin number	Description	I/O	Simplified electrical schematics
<b>Power supplies</b>				
AGND	A2, A4, A5, A6, A7, A8, A11, A12, A13, A14, A15, A17, A18, B1, B2, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B17, B18, C3, C4, C5, C8, C9, C10, C11, C14, C15, C16, D3, D4, D6, D7, D8, D11, D12, D13, D15, D16, E5, E6, E9, E10, E13, E14, F7, F8, F11, F12, G8, G9, G10, G11, H9, H10, J8, J11	Analog ground		
VCCA	D9, D10, E7, E8, E11, E12, F9, F10, H8, H11, J9, J10, K8, K11	Analog power supply		
GNDD	K10, L10	Digital ground		
VCCD	K9, L9	Digital power supply		
GNDIO	F5, F6, F13, F14, G6, G13, H6, H13, J5, J6, J13, J14, K5, K6, K13, K14, L6, L8, L11, L13, M5, M7, M12, M14, N5, N6, N8, N9, N10, N11, N13, N14, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, U5, U8, U9, U10, U11, U14, V1, V2, V3, V4, V5, V9, V10, V11, V15, V16, V17, V18	I/O ground		
VCCIOH1	H5, H7, H12, H14, K7, K12	Output power supply for LVDS port high		
VCCIO L1	L5, L7, L12, L14, M9, M10	Output power supply for LVDS port low		
VCCIOH2	G5, G7, G12, G14, J7, J12	Output power supply for LVDS port high		
VCCIO L2	M6, M8, M11, M13, N7, N12	Output power supply for LVDS port low		
<b>Clock</b>				
CLKP CLKN	A10 A9	Input clock signal	I	
<b>Analog signals</b>				

Pin label	Pin number	Description	I/O	Simplified electrical schematics
AINP AINN	C7, C6	Analog input for ADC A	I	
BINP BINN	C12, C13	Analog input for ADC B	I	
CMIREFA CMIREFB	D5, D14	Input signal common mode reference for A and B cores.  In AC coupling operation this output must be left floating (not used) In DC coupling operation, these pins provide an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	
<b>Digital output (LVDS)</b>				
AH0P, AH0N AH1P, AH1N AH2P, AH2N AH3P, AH3N AH4P, AH4N AH5P, AH5N AH6P, AH6N AH7P, AH7N AH8P, AH8N AH9P, AH9N AH10P, AH10N AH11P, AH11N	K1, K2 K3, K4 J1, J2 J3, J4 H1, H2 H3, H4 G1, G2 G3, G4 F1, F2 F3, F4 E1, E2 D1, D2	High port channel A output data AH0 is the LSB, AH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O	
AFU1P, AFU1N	E3, E4	Channel A control bit 1	O	
AL0P, AL0N AL1P, AL1N AL2P, AL2N AL3P, AL3N AL4P, AL4N AL5P, AL5N AL6P, AL6N AL7P, AL7N AL8P, AL8N AL9P, AL9N AL10P, AL10N AL11P, AL11N	M1, M2 M3, M4 N1, N2 N3, N4 P1, P2 P3, P4 R1, R2 R3, R4 T1, T2 T3, T4 U1, U2 U3, U4	Low port channel A output data AL0 is the LSB, AL11 is the MSB. (in DEMUX 1:1, this channel is disabled)	O	
AFU2P, AFU2N	L3, L4	Channel A control bit 2	O	
ADRP, ADRN	L1, L2	Channel A data ready	O	
BH0P, BH0N BH1P, BH1N BH2P, BH2N BH3P, BH3N BH4P, BH4N BH5P, BH5N BH6P, BH6N BH7P, BH7N BH8P, BH8N BH9P, BH9N BH10P, BH10N BH11P, BH11N	K18, K17 K16, K15 J18, J17 J16, J15 H18, H17 H16, H15 G18, G17 G16, G15 F18, F17 F16, F15 E18, E17 D18, D17	High port channel B output data BH0 is the LSB, BH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O	
BFU1P, BFU1N	E16, E15	Channel B control bit 1	O	

Pin label	Pin number	Description	I/O	Simplified electrical schematics
BL0P, BL0N BL1P, BL1N BL2P, BL2N BL3P, BL3N BL4P, BL4N BL5P, BL5N BL6P, BL6N BL7P, BL7N BL8P, BL8N BL9P, BL9N BL10P, BL10N BL11P, BL11N	M18, M17 M16, M15 N18, N17 N16, N15 P18, P17 P16, P15 R18, R17 R16, R15 T18, T17 T16, T15 U18, U17 U16, U15	Low port channel B output data BL0 is the LSB, BL11 is the MSB (in DEMUX 1:1, this channel is disabled)	O	
BFU2P, BFU2N	L16, L15	Channel B control bit 2	O	
BDRP, BDRN	L18, L17	Channel B data ready	O	
SSOP, SSON	C1, C2	Slow Synchronization Output clock	O	
SYNCO, SYNCON	C18, C17	Synchronization output signal	O	
<b>SPI digital I/O (CMOS)</b>				
CSN	V14	Chip Select signal (active low) Internal pull-up	I	
SCLK	U12	SPI clock Internal pull-up	I	
MOSI	V13	SPI Master Out Slave In Internal pull-up	I	
RSTN	U13	SPI asynchronous reset (active low) Internal pull-up	I	
MISO	V12	SPI Master In Slave Out	O	
<b>DIGITAL INPUT (LVDS)</b>				

Pin label	Pin number	Description	I/O	Simplified electrical schematics
SYNCTRIGP SYNCTRIGN	A3, B3	Differential input synchronization or trigger signal (LVDS)  Active high signal	I	
<b>Miscellaneous</b>				
scan	V6	RESERVED PIN <b>Must be pulled-down with 10kΩ</b>		
TESTA	U6	RESERVED PIN <b>Should be left unconnected</b>		
VCCFuseA, VCCFuseB VCCFuseC	V8 V7 U7	RESERVED PIN <b>Should be left unconnected</b>		
DiodeA, DiodeC	B16 A16	Junction temperature monitoring diode anode and cathode	I	

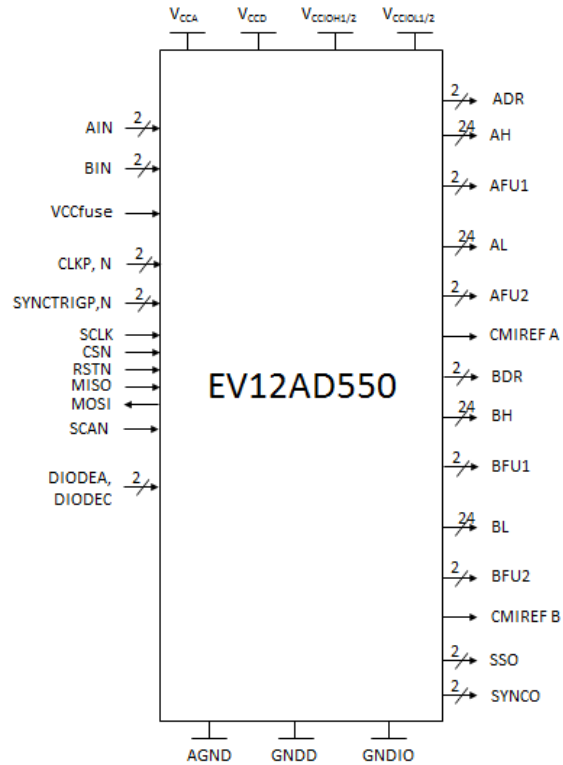


## 5 Theory of operation

### 5.1 Overview

Table 16: Functional description

Name	Function		
V <sub>CCA</sub>	Analog power supply		
V <sub>CCD</sub>	Digital power supply		
AGND	Analog ground		
GNDD	Digital ground		
V <sub>CCIOL/H1</sub>	Output buffers power supplies		
V <sub>CCIOL/H2</sub>			
GNDIO	Ground for output buffers		
AINP, AINN	Analog input for ADC core A		
BINP, BINN	Analog input for ADC core B		
CLKP, CLKN	Differential clock input		
[AHOP:AH11P] [AHON:AH11N]	High port channel A output data (active in both DEMUX modes)		
AFU1P, AFU1N	Channel A control bit 1		
[ALOP:AL11P] [ALON:AL11N]	Low port channel A output data (inactive in DEMUX 1:1 mode)		
AFU2P, AFU2N	Channel A control bit 2		
ADRP, ADRN	Channel A data ready		
[BHOP:BH11P] [BHON:BH11N]	High port channel B output data (active in both DEMUX modes)		
BFU1, BFU1N	Channel B control bit 1		
[BLOP:BL11P] [BLON:BL11N]	Low port channel B output data (inactive in DEMUX 1:1 mode)		
BFU2, BFU2N	Channel B control bit 2		
BDRP, BDRN	Channel B data ready		
CSN	SPI chip select input (active low)	SYNCTRIGP, SYNCTRIGN	Differential input synchronization or trigger signal (LVDS)
RSTN	SPI asynchronous reset input (active low)		
SCLK	SPI input clock	SYNCO, SYNCON	Synchronization output signal
MOSI	SPI Master Out Slave In	SSOP, SSON	Slow Synchronization Output clock
MISO	SPI Master In Slave Out	CMIRefA CMIRefB	Output voltage for input common mode reference of ADC A and B
DIODEA, DIODEC	Diode anode and cathode inputs for die junction temperature monitoring	TESTA	RESERVED PIN Should be left unconnected
SCAN	RESERVED PIN Must be pulled-down with 10kΩ	VCCfuse	RESERVED PIN Should be left unconnected



## 5.2 Digital Reset and start up procedure

RSTN is an asynchronous active low global reset for the SPI and OTP (One Time Programmable registers). It is mandatory to put RSTN at low level during a minimum of 10 $\mu$ s at power-up of the device. It sets all SPI registers to their default values. The SPI interface can be used or not; if it is not used, the OTP value and default SPI configurations will be automatically loaded (see section [Using the SPI interface](#) and [Without using the SPI interface](#) for more information).

### 5.2.1 Using the SPI interface

Figure 11 presents the reset and synchronization to realize after power-up when the SPI interface is used (see section [Serial Peripheral Interface](#) for more information on the SPI interface).

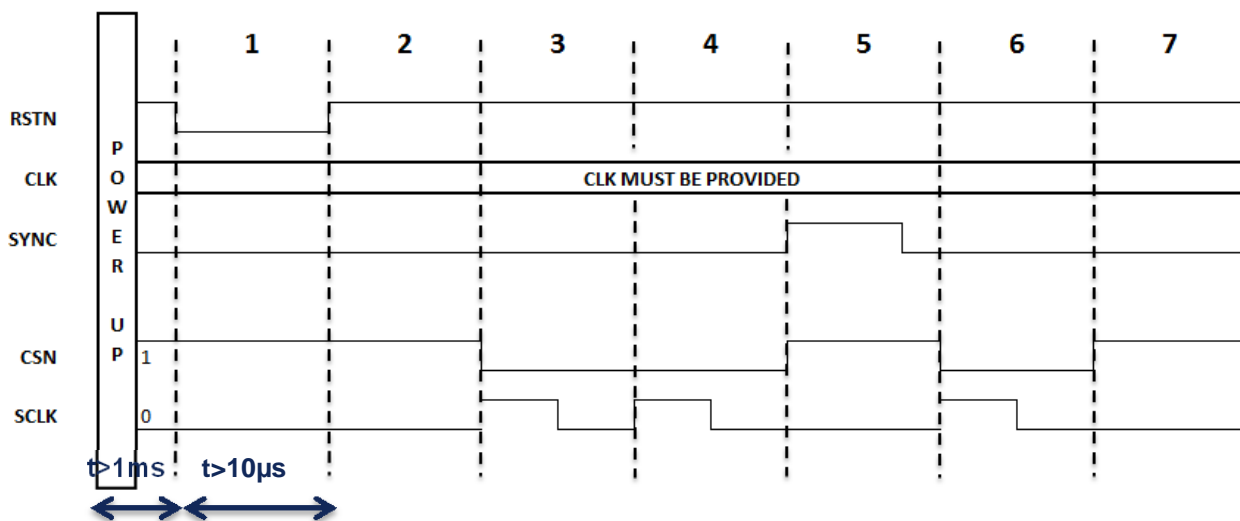


Figure 11: Start-up sequence when using the SPI interface

1. It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least 10 $\mu$ s. During the RSTN pulse, CSN must be held high and SCLK held low. The CLK must be provided before the RSTN pulse. The CLK can start before or after the power-up;
2. The fuses need 1ms to wake up;
3. The SPI instruction WRITE @0x7E 0x0001 must be sent to the ADC. The OTP are loaded into the SPI registers at this point. There must be at least 1ms between the RSTN pulse and this SPI instruction;
4. The ADC is configured through the SPI interface;
5. A pulse is applied onto the SYNC input to reset the internal clocks (SYNC signal in Figure 11). At this stage the bit 7 of register CHIP\_CTRL must be at '0' (trigger mode disabled) – see section [SYNCTRIG input](#);
6. The ADC can be configured in trigger mode enable and the SE\_protect register can be activated – see section [Extra SEE protect](#) ;
7. Normal operation of the ADC.

### 5.2.2 Without using the SPI interface

The figure below presents the reset and synchronization to realize after power-up of the device when the SPI interface is not used. In this case, the configuration of the ADC cannot be changed and corresponds to the SPI default values (refer to [Register mapping and default configuration](#)). Due to the internal pull-up of the SPI inputs, this is the default mode when the SPI inputs are floating.

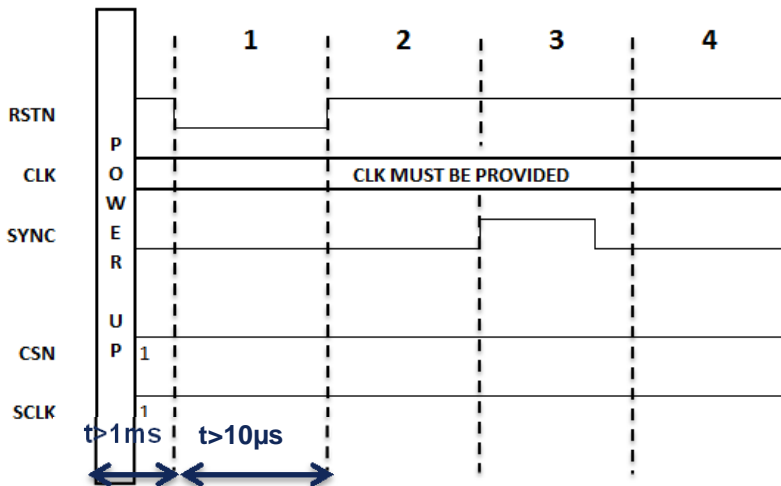


Figure 12: Start-up sequence when the SPI interface is not used

1. It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least  $10\mu\text{s}$ . During the RSTN pulse, CSN must be held high and SCLK held high. The CLK must be provided before the RSTN pulse. It can start either before or after the power-up;
2. The fuses need 1ms to wake up;
3. A pulse is applied onto the SYNCTRIG input to reset the internal clocks (SYNC signal in Figure 12) ;
4. Normal operation of the ADC.

Refer to section [Register mapping and default configuration](#) for more information on the ADC configuration when the SPI interface is not used.

## 5.3 Serial Peripheral Interface

### 5.3.1 SPI Characteristics

The SPI interface uses the 5 following input/output signals:

- RSTN: asynchronous reset active low;
- SCLK: SPI clock;
- CSN: Chip Select active low;
- MISO: Master In Slave Out;
- MOSI: Master Out Slave In.

And is a standard SPI with:

- 8 address bits from the MSB A[7] to A [0], with A[7] being the R/W bit;
- 16 data bits from the MSB D[15] to D[0]

The MOSI sequence should start (A[7] bit) with '0' for a read procedure and '1' for a write procedure.

The following diagrams (Figure 13 and 14) show a write and read procedure address and data sequencing. For more information on the timing between signals refer to Figure 7.

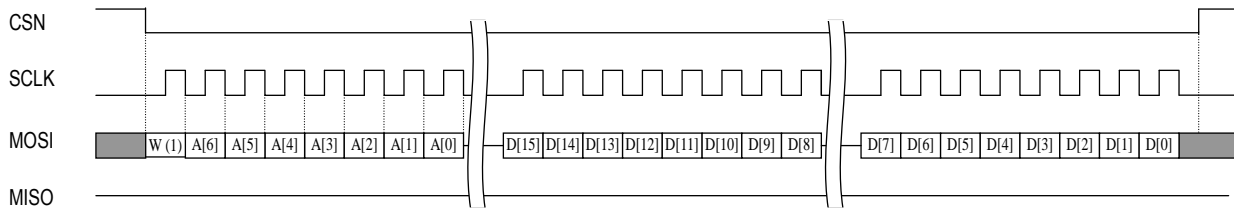


Figure 13: SPI write procedure

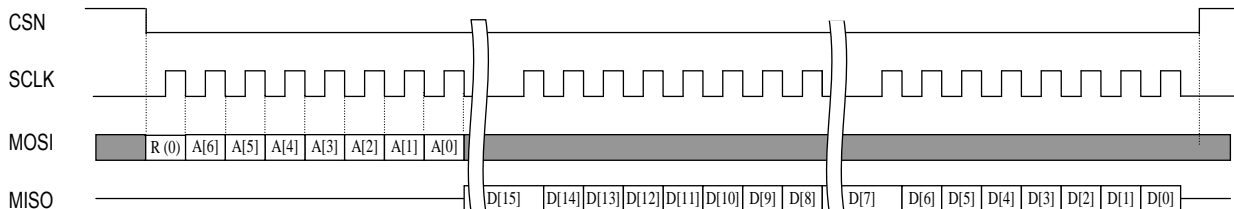


Figure 14: SPI read procedure

### 5.3.2 Register mapping and default configuration

Table 17: Register mapping

Address	Register	Access	Bit	Default value	Description	Refer to section
0x01	CHIP_ID	R	[15..0]		Chip ID	
0x02	S_N	R	[15..0]		Chip serial number	
0x04	CHIP_CTRL	W/R	[15..9]	0x00	Reserved	
			8	0b0	SSO and SYNCO swing adjust 1: full swing 0: reduced swing	<a href="#">5.7</a>
			7	0b0	Trigger enable 1: enabled 0: disabled	<a href="#">5.4.2</a>
			6	0b0	LVDS swing adjust 1: full swing 0: reduced swing	<a href="#">5.4.3</a>
			5	0b1	Bandwidth selection 1: nominal 0: extended	<a href="#">5.5.2</a>
			4	0b1	Reserved	
			3	0b0	Temperature calibration selection 1: high temperature 0: low and ambient temperature	<a href="#">5.8</a>
			2	0b0	Reserved	
			1	0b0	Reserved	
0x1E	A_CMIREF	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input common mode trimming for channel A	<a href="#">5.5.3</a>
0x1F	A_RIN	W/R	[15..5]	0x000	Reserved	

Address	Register	Access	Bit	Default value	Description	Refer to section
			[4..0]	0x10	Input impedance trimming for channel A	<a href="#">5.5.1</a>
0x20	A_SDA_CTRL	W/R	[15..13]	0x0	Reserved	
			12	0b1	SDA control for channel A 0: enabled 1: disabled	<a href="#">5.12</a>
			[11..0]	0x000	SDA value for channel A	<a href="#">5.12</a>
0x21	A_GAIN_CAL	W/R	[15..10]	0x00	Reserved	
			[9..0]	0x0200	gain calibration for channel A	<a href="#">5.11.2</a>
0x22	A_PHASE_CAL	W/R	[15..8]	0x00	Reserved	
			[7..0]	0x80	Interleaving phase calibration for channel A	<a href="#">5.11.2</a>
0x23	A_OFFSET_CAL	W/R	[15..9]	0x00	Reserved	
			[8..0]	0x0100	offset calibration for channel A	<a href="#">5.11.2</a>
0x3D	B_CMIREF	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input common mode trimming for channel B	<a href="#">5.5.3</a>
0x3E	B_RIN	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input impedance trimming for channel B	<a href="#">5.5.1</a>
0x3F	B_SDA_CTRL	W/R	[15..13]	0x00	Reserved	
			12	0b1	SDA control for channel B 0: enabled 1: disabled	<a href="#">5.12</a>
			[11..0]	0x000	SDA value for channel B	<a href="#">5.12</a>
0x40	B_GAIN_CAL	W/R	[15..10]	0x00	Reserved	
			[9..0]	0x0200	gain calibration for channel B	<a href="#">5.11.2</a>
0x41	B_PHASE_CAL	W/R	[15..8]	0x00	Reserved	
			[7..0]	0x80	Interleaving phase calibration for channel B	<a href="#">5.11.2</a>
0x42	B_OFFSET_CAL	W/R	[15..9]	0x00	Reserved	
			[8..0]	0x0100	Interleaving offset calibration for channel B	<a href="#">5.11.2</a>
0x62	STDBY	W/R	[15..6]	0x000	Reserved	
			5	0b0	Channel B analog standby 1: enabled 0: disabled	<a href="#">5.13</a>
			4	0b0	Channel A analog standby 1: enabled 0: disabled	<a href="#">5.13</a>
			[3..2]	0b00	Reserved	
			1	0b0	Channel B full standby 1: enabled 0: disabled	<a href="#">5.13</a>
			0	0b0	Channel A full standby 1: enabled 0: disabled	<a href="#">5.13</a>
0x63	LVDS_PRBS_CTRL	W/R	[15..2]	0x0000	Reserved	

Address	Register	Access	Bit	Default value	Description	Refer to section
			[1..0]	0b00	PRBS on LVDS output 00: data only 01: data xor PRBS 11: PRBS only	<a href="#">5.4.4</a>
0x64	CTRL_BIT_CFG	W/R	[15..4]	0x000	Reserved	
			[3..2]	0b00	XFU2 selection: 00: In-range 01: parity bit 10: trigger	<a href="#">5.4.2</a>
			[1..0]	0b00	XFU1 selection: 00: In-range 01: parity bit 10: trigger	<a href="#">5.4.2</a>
0x65	Reserved	W/R	[15..0]	0x0000	Reserved	
0x66	TEST_MODE	W/R	[15..5]	0x000	Reserved	
			4	0b0	Ramp 1: enabled 0: disabled	<a href="#">5.9.2</a>
			3	0b0	Flash 1: enabled 0: disabled	<a href="#">5.9.3</a>
			[2..1]	0b00	Reserved	
			0	0b0	Test mode 1: enabled 0: disabled	<a href="#">5.9.1</a>
0x67	FLASH_RST_LENGTH	W/R	[15..12]	0x0	Reserved	
			[11..6]	0x10	Number of clock cycle when data ready is driven low after a SYNC	<a href="#">5.6</a>
			[5..0]	0x18	Flash pattern length	<a href="#">5.9.3</a>
0x68	OUT_SEL	W/R	[15..1]	0x0000	Reserved for optional features	
			0	0b0	DEMUX selection 0: DEMUX 1:1 1: DEMUX 1:2	<a href="#">5.4.1</a>
0x69	A_CALC_CRC	R	[15..0]		CRC value for channel A	<a href="#">5.10.2</a>
0x6A	B_CALC_CRC	R	[15..0]		CRC value for channel B	<a href="#">5.10.2</a>
0x74	SYNC_CTRL	W/R	[15..2]	0x0000	Reserved	
			1	0b0	One clock period added on internal SYNC 1: Yes 0: No	<a href="#">5.6</a>
			0	0b0	Edge selection for SYNC recovery 1: Clock falling edge 0: Clock rising edge	<a href="#">5.6</a>

Address	Register	Access	Bit	Default value	Description	Refer to section
0x75	SYNC_FLAG	R	0		When at '1' indicates that the last SYNC pulse entered in a metastable zone. Reset to '0' when read.	<a href="#">5.6</a>
0x76	A_CAL_CRC1	R	16		CRC channel A low & Ambient temperature calibration	<a href="#">5.10.2</a>
0x77	A_CAL_CRC2	R	16		CRC channel A high temperature calibration set 1	<a href="#">5.10.2</a>
0x78	B_CAL_CRC1	R	16		CRC channel B low & Ambient temperature calibration set 2	<a href="#">5.10.2</a>
0x79	B_CAL_CRC2	R	16		CRC channel B high temperature calibration set 1	<a href="#">5.10.2</a>
0x7E	LOAD_CAL	W	[15..1]	0x0000	Reserved	
			0		Load calibration when written 1	<a href="#">5.8</a>
0x7F	EXTRA_SEE_PROTECT	W/R	[15..0]	0x0000	Reserved	
			0	0	SE protect 1: enabled 0: disabled	<a href="#">5.10.1</a>

## 5.4 Output selection

### 5.4.1 DEMUX 1:1 or 1:2

The output of the ADC is an LVDS with either a DMUX 1:1 or 1:2 configurable through the SPI register OUT\_SEL at address 0x68:

OUT_SEL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															DMUX_SEL

Setting DMUX\_SEL to “0” configures the output in DEMUX 1:1, which is the default configuration. Setting it to “1” configures the output in DEMUX 1:2.

When in DEMUX 1:1, the output low port for A and B channels should be grounded.  
Depending on the output mode of interest, the supplies should be configured as follows:

**Table 18:** Power supplies configuration

		Single rail		Dual rail	
		DMUX 1:1	DMUX 1:2	DMUX 1:1	DMUX 1:2
Analog supply	VCCA	3.4V		3.4V	
	AGND	GND		GND	
Digital supply	VCCD	3.4V		2.5V	
	DGND	GND		GND	
I/O Supplies	VCCIOH1	3.4V		2.5V	
	VCCIOH2	3.4V		3.4V	
	VCCIO1	GND	3.4V	GND	2.5V
	VCCIO2	GND	3.4V	GND	3.4V
	GNDIO	GND		GND	

Note: In dual-rail configuration, the power consumption is reduced.

#### 5.4.2 Control bit XFU1 and XFU2

Three different control bits can be output on XFU1 and XFU2: in-range, parity or trigger. In DEMUX 1:1, XFU1 and XFU2 relate both to the high port output. In DEMUX 1:2, XFU1 relates to the sample output on the high port and XFU2 on the low port. The configuration of the control bits is done through the register CTRL\_BIT\_CFG selection at address 0x64:

CTRL_BIT_CFG															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
														XFU2_SEL	XFU1_SEL

XFU1 and XFU2 control bits are set for both channels. All control bits are output at the same time as the sample they control.

##### 5.4.2.1 IN-RANGE

The in-range control bit output '1' when the ADC input is not saturated and '0' when it is. To set XFUn as the in-range, XFUn\_SEL must be set to "00".

##### 5.4.2.2 PARITY BIT

The parity bit is a XOR between the 12 bits of the sample. To set XFUn as the parity, XFUn\_SEL must be set to "01". This function allows users to detect rapidly any communication issues between ADC and the data receiver.

##### 5.4.2.3 TRIGGER

The trigger bit is a copy of the SYNCTRIG input with the same pipeline delay as the sampled data (refer to timing diagram in Figure 15 below) To set XFUn as the trigger, XFUn\_SEL must be set to "10" and TREN in register CHIP\_CTRL at 0x04 set to '1'.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								TREN							

Note: When TREN is set to '1', the SYNCTRIG input is used as a trigger input, when at '0' it is used as a SYNC input. See section [SYNCTRIG input](#) for more information.



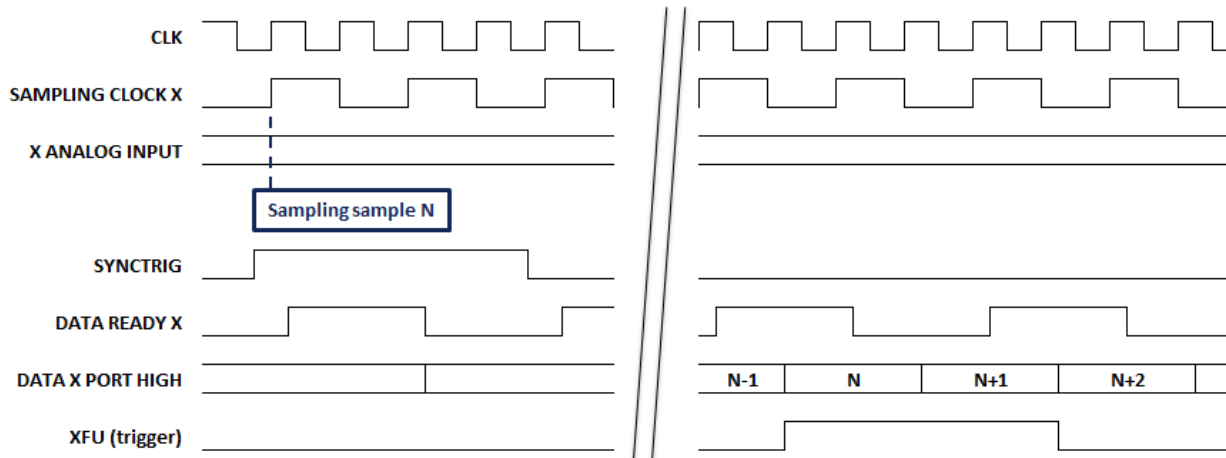


Figure 15: Trigger mode timing diagram

5.4.3 Swing adjust

By default the swing of the data output is reduced to optimize power consumption. Typical differential reduced swing amplitude is 290mVpeak. If required, user could set the LSSA bit to “1” to get a wider swing with typical amplitude around 320 mVp (see Table 8: **Dynamic characteristics**).

This “full swing option” will increase Icco1 by 50mA in DMUX1:1 and by 80mA in DMUX1:2.

It is configured through register CHIP\_CTRL at 0x04:-

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
									LSSA						

When LSSA is at ‘0’, the output swing of LVDS data and data ready are reduced which is the default configuration as well. When set to ‘1’ LVDS output data and data ready are in full swing configuration.

5.4.4 PRBS on data output

A PRBS (Pseudo Random Bit Sequence) can be generated for the LVDS output. It can either be disabled, scrambling the data or output alone. The implemented PRBS sequence is based on the sequence  $X7 + X6 + 1$ . The same sequence is output on all bits of the LVDS ports (12 bits of data and the XFU1 and XFU2 bits).

It is configured through the LVDS\_PRBS\_CTRL register at address 0x63.

LVDS_PRBS_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															PRBS_ctrl

PRBS\_ctrl = “00” by default and the PRBS is disabled; the output data corresponds to the ADC samples plus control bit. Setting PRBS\_ctrl to “01” configures the LVDS output in scrambling mode. In that case, the output corresponds to the ADC samples plus control bit XOR the PRBS value. The PRBS value is the same on all output.

Setting PRBS\_ctrl to “11” configures the LVDS output so that the PRBS alone is output. The PRBS value is the same on all output.

## 5.5 Input configuration

### 5.5.1 Input impedance trimming

Impedance matching is important to maximize power transmission and minimize reflection. The DC resistance of each channel can be trimmed digitally and individually to 100Ω through register X\_RIN at address 0x1F for channel A and 0x3E for channel B:

X_RIN															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
											RIN_TRIM				

The default value is 0x10. Trimming the input impedance allows to achieve a 100Ω +/-2.4Ω precision.

Min register 0x00 value gives the max resistance value. Max register value 0x3F gives the min resistance value. Trimming step is around ~2.4Ω.

### 5.5.2 Input bandwidth selection

The ADC has a tunable bandwidth selectable through SPI with register CHIP\_CTRL at 0x04:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
											BW				

Refer to Table 8: Dynamic characteristics to consider Nominal and extended bandwidth cut off frequency.

Nominal bandwidth is set by default (BW = '1'). This mode should be preferred to improve noise performance. When working with high input frequency (>3.4GHz), it is optimal to use the extended bandwidth mode (BW = '0').

### 5.5.3 Input common mode trimming

The ADC can work with DC coupling analog inputs. Its input common mode (CMIREF) for each channel can be trimmed individually. It can also be used to optimize linearity performance. It is controlled through the register X\_CMIREF at address 0x1E for channel A and 0x3D for channel B:

X_CMIREF															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
											CMIN_TRIM				

The default value is 0x10. Each increment of the value adds 11mV; each decrement reduces the common mode by 11mV. The 31 possible steps thus allow 341mV range.

## 5.6 SYNC Mode and TRIGGER mode

The selection between the two modes is controlled through bit7 of SPI register CHIP\_CTRL at address 0x04.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								TREN							

TREN = '0' is the SYNC mode (default mode).

TREN = '1' is the trigger mode (see section [Control bit XFU1 and XFU2](#) for more information).

Both modes share the same input SYNCTRIG pin (LVDS).

### SYNC Mode

SYNC mode is mandatory in order to have deterministic timing for the 2 cores synchronization and for multiple ADCs time alignment. Thus it is necessary to send a SYNC pulse after power-up so that the ADC timing circuitry starts in a deterministic way. This pulse resets the different dividers on the clock path and ensures that all the timing circuitry restarts deterministically. It also resets the test modes to their initial value.

The SYNC signal can be synchronous or asynchronous to the external clock, is active high and should be compliant with the timing specified in Table 10.

Two SPI registers are used to help detect and avoid meta-stability at the SYNC input:

- SYNC\_FLAG; bit 0 at address 0x75:

SYNC_FLAG															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															SFL

SFL is at '1' when meta-stability has occurred on the SYNC input. Its value should be reset after being read.

- SYNC\_CTRL; bit 1 and 0 at address 0x74:

SYNC_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
														SDEL	ESEL

The SDEL bit can be used to add one clock cycle delay to the internal SYNC path. This allows delaying the restart of the timing of the ADC by one clock cycle. This is useful for multiple devices synchronization (refer to section [Multiple ADC chaining synchronization](#)).

Please refer to specific Application Note for more information on how to synchronize ADCs using those flags.

SYNC_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															ESEL

The ESEL bit is used to configure which edges of the input clock recovers the SYNCTRIG input. By default, the SYNCTRIG input is recovered on rising edges of the clock (ESEL = '0'); when ESEL = '1', the SYNCTRIG input is recovered on falling edges of the input clock. In any case, the reset of the timing circuitry of the ADC is done on rising edges of the input clock. This feature is useful to avoid the meta-stability zone of the SYNCTRIG input specified in Table 10.

When a SYNCTRIG input pulse is sent in SYNC mode, the timing circuitry is reset; thus the data ready output will stop. The time before it restarts can be configured through the FLASH\_RST\_LENGTH register at address 0x67.

FLASH_RST_LENGTH																	
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
				reset_length													

By default, reset\_length is at 16. Refer to timing diagram in Figure 5 to see an example with reset\_length = 4. For a deterministic timing, reset\_length value must be within 2 (0b000010) and 64 (0b111111).

### Trigger Mode

(Please refer section [Control bit XFU1 and XFU2 TRIGGER](#) for more information).

In trigger mode, a copy of the SYNCTRIG input is outputted on XFUn pin with the same pipeline delay as the sampled data (refer to Figure 15: Trigger mode timing diagram).

### 5.7 SYNCO output and Slow Synchronization Output (SSO)

SYNCO output is a copy of the SYNCTRIG input resampled onto the CLK signal. It can be used to synchronize multiple devices with a chained SYNCO to SYNCTRIG interface.

The SSO output signal is an asynchronous clock signal, made by a division by 16 of the master clock input. It is never stopped, reset nor interrupted as long as the master clock is provided to the ADC. It can be used as a slow reference clock to synchronize the sampling of multiple devices or provide a synchronous clock source to other elements in the system.

Both SYNCO and SSO are LVDS output signals; their swing can be configured through the bit 8 of register CHIP\_CTRL at address 0x04.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							SOSA								

When SOSA is at '0', the LVDS output swing of SSO and SYNCO are reduced which is the default configuration. When set to '1' SSO and SYNCO are in full swing configuration.

### 5.8 Temperature calibration set selection

A factory calibration is performed on every part during industrial test. During this process, two sets of factory calibration (over temperature) are saved in on-chip One Time Programmable registers (OTP). To optimize performance of the device, hot

temperature calibration should be chosen when working with diode temperature over 65°C and cold temperature should be chosen when working with diode temperature below 65°C. (Refer to diode characteristic)

To choose which factory temperature calibration set to load, bit 3 of register CHIP\_CTRL at address 0x04 should be considered:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
												CAL_S			

By default, ambient temperature calibration set is selected (CAL\_S = '0'). To change to hot temperature calibration, CAL\_S should be written to '1'. Whenever this bit is modified, the calibration should be loaded into the SPI register through writing '1' in bit 0 of register LOAD\_CAL at address 0x7E:

LOAD_CAL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															L_CAL

## 5.9 Test mode

### 5.9.1 Enabling test mode

Two test modes on the ADC output are offered to help validate the interface with the ADC: flash and ramp patterns. The test modes are enabled through the TEST\_MODE register at address 0x66:

TEST_MODE															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
												RPEN	FLEN		TMEN

To enable any test mode, it is necessary to put TMEN at '1' (test mode is disabled by default). Then to activate ramp pattern mode, RPEN must be set to '1' and to activate a flash pattern output, FLEN must be set to '1'. If both RPEN and FLEN are set to '1', the output is in normal operation and none of the test modes is output. Refer to the 2 following sections for more information on the test modes.

### 5.9.2 Ramp test mode

In ramp test mode, the data output on the LVDS is a 12 bit ramp on both channels XH (and XL in DEMUX 1:2). The same value is output on both ports in DEMUX 1:2. The 2 control bits XFU1 and XFU2 are toggling. See the timing diagram below for more information (X represents channel A or B).

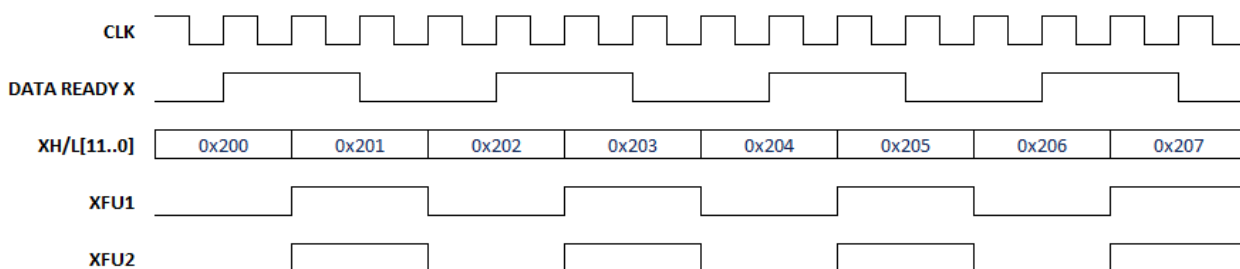


Figure 16: Ramp test mode timing diagram

The ramp value is reset to 0x000 when a pulse is sent on the SYNCTRIG input in SYNC mode (See section [SYNCTRIG input](#) for more information).

### 5.9.3 Flash test mode

The flash mode is useful to align the interface between FPGA and ADC. The flashing pattern consists of one data at 0xFF followed by [flash\_length-1] data at 0x000. The control bit XFU1 and XFU2 follows the same sequence. The flash\_length value can be configured through the FLASH\_RST\_LENGTH register at address 0x67. Its default value is 24.

FLASH_RST_LENGTH															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															Flash_length

See below the timing diagram for the LVDS output when in flashing mode. It is the same for both channels and all ports used (X represents channel A or B).

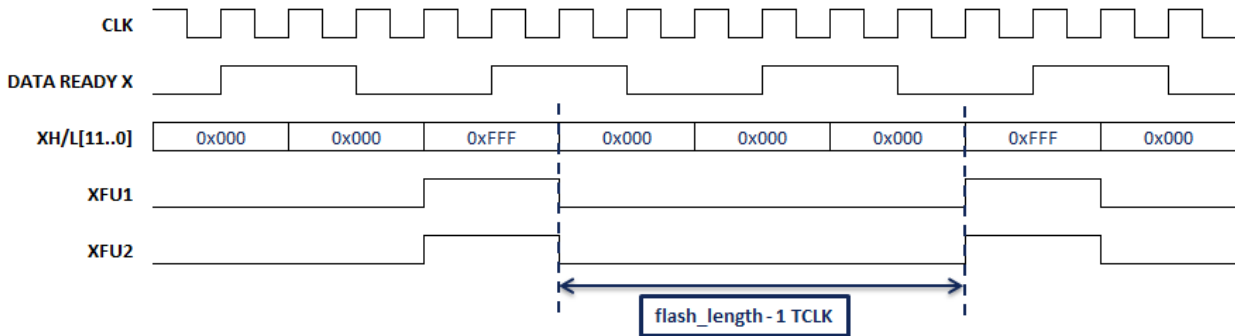


Figure 17: Flashing test mode timing diagram

## 5.10 Single event protection

### 5.10.1 Extra SEE protect

All sensitive areas of the device have been protected to increase robustness against to radiation effects. This includes but is not limited to clock circuitry and SPI registers. To improve even more the robustness, an extra protection mode has been implemented. It can be activated through the following register EXTRA\_SEE\_PROTECT at address 0x7F:

EXTRA_SEE_PROTECT															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															SEP

Enabling register SEP by writing '1' disables the SYNCTRIG input when in SYNC mode and thus prevents unwanted timing reset of the ADC (See section [SYNCTRIG input](#) for more information). It prevents as well any modification on the SPI registers. The SPI clock (SCLK) can be provided from time to time to refresh the SPI (and flush out any SE that would have impacted one branch of the TMR). When it is necessary to modify the configuration of the device or synchronize the ADC, this register needs to be set back to '0'.

Use of this register is not mandatory, but improves the robustness of the device against radiation effects.

### 5.10.2 CRC checking

An option to verify that the calibration has been successfully loaded is available through SPI registers. The CRC reference value is stored in the OTP (One Time Programmable registers) during industrial testing of the part respectively for each channel and each calibration set at the following addresses:

- 0x76 for channel A and ambient & cold temperature calibration;
- 0x77 for channel A and hot temperature calibration;
- 0x78 for channel B and ambient & cold temperature calibration;
- 0x79 for channel B and hot temperature calibration;

When the calibration is loaded into the SPI, the CRC of the loaded set is automatically calculated for each channel and can be read in registers 0x69 for channel A and 0x6A for channel B. If the calculated CRC value and the reference value (corresponding to the loaded calibration) are equal, the load has been successful; if not, the desired calibration set should be reloaded. Refer to section [Temperature calibration set selection](#) for more information.

## 5.11 Interleaving the cores

### 5.11.1 Interleaving or aligning the sampling clocks

The sampling clocks of channel A and B can be interleaved (default configuration) or aligned. This is controlled through bit 0 of register CHIP\_CTRL at address 0x04.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															CLKINT

When CLKINT = '0', the sampling clocks of channel A and B **are in phase**;

When CLKINT = '1' (default configuration), the sampling clocks of channel A and B are **in phase opposition** to allow interleaving.

### 5.11.2 Interleaving calibration

To improve interleaving performance, the offset, gain and phase of each core can be corrected thanks to embedded DACs. These settings are available through SPI commands and are application dependent.

The offset calibration is available in register X\_OFFSET\_CAL at address 0x23 for channel A and 0x42 for channel B.

X_OFFSET_CAL																	
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
							Offset_calibration										

These offset calibration registers offer a tuning range of +/- 27.4LSB by step of 0.11LSB. The default value is 0x100; the minimum value 0x000 corresponds to +27.4LSB correction; the maximum value 0x1FF corresponds to -27.4LSB correction.

The gain calibration is available in register X\_GAIN\_CAL at address 0x21 for channel A and 0x40 for channel B.

X_GAIN_CAL																	
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
							Gain_calibration										

These gain calibration registers offer a tuning range of +260/-226LSB by step of 0.47 LSB. The default value is 0x200. Min register value 0x000 corresponds to +260 LSB while max register value 0x3FF corresponds to -226LSB.

The phase calibration is available in register X\_PHASE\_CAL at address 0x22 for channel A and 0x41 for channel B.

X_PHASE_CAL																	
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
							Phase_calibration										

These phase calibration registers offer a tuning range of +/- 0.9ps by step of 7fs. The default value is 0x80; the minimum value 0x00 corresponds to -900fs correction; and the maximum value 0xFF corresponds to +900fs correction. For wider range of phase correction, SDA could be used (refer to section [Sampling Delay Adjust \(SDA\)](#)).

## 5.12 Sampling Delay Adjust (SDA)

The effective sampling instant of each ADC cores is adjustable independently thanks to built-in fine clock shifters. They provide 4095 steps of ~21fs delay to achieve a **total tuning range of ~90ps**. The delay is configured through the SPI register X\_SDA\_CTRL at address 0x20 for channel A and 0x3F for channel B.

X_SDA_CTRL																	
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
			DIS	SDA_value													

For proper operation, when used, the SDA mode has to be enabled for both cores.

To enable the SDA, the bit 12 should be set to '0', and the value of delay added on the sampling time will be SDA\_value x 10 fs. The SDA is disabled by default (DIS = '1'). It should be noted that enabling the SDA has an impact on the jitter performance of the ADC.

Enabling the SDA automatically adds ~30ps delay on the sampling clock path. Moreover, the SDA must be either enabled on both channels or disabled on both channels for the ADC to work. The SDA\_value can be different between channels.

### 5.13 Stand-by modes

The stand-by modes are controlled through the STDBY register at address 0x62:

STDBY															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
										SAB	SAA			SFB	SFA

Both channels can be put in full stand-by independently. Writing '1' in the register SFA (respectively SFB) will put the channel A (respectively B) in stand-by.

A standby of the analog part of the ADC can also be done through writing '1' in the register SAA (respectively SAB) on channel A (respectively B). Its advantage is that it reduces the power consumption while keeping the output interface running.

### 5.14 Die temperature monitoring diode

Two pins are provided so that the temperature diode can be probed using standard temperature sensors. Diode C must be connected to GND.

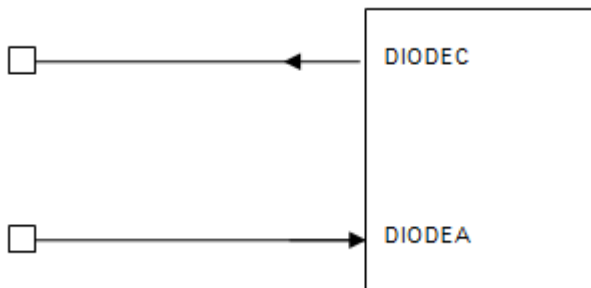
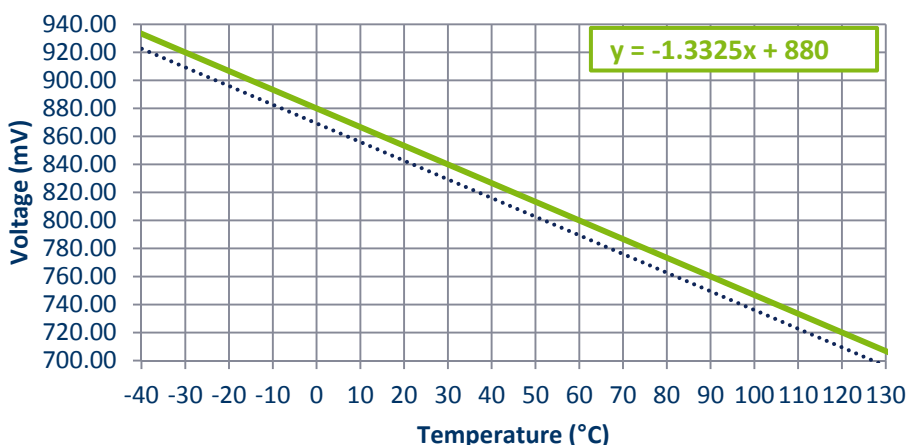


Figure 18: Temperature diode connection

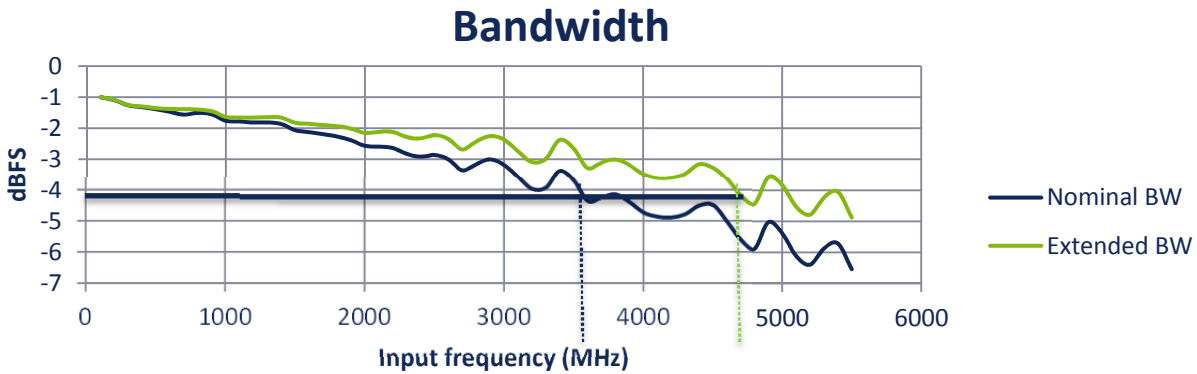
To characterize the temperature diode, a maximum current of 1 mA is applied on the DIODEA pin. The voltage across the DIODEA pin and the GND pin gives the junction temperature using the intrinsic diode characteristics below. The green and blue dashed lines represent diode voltage versus hot spot junction temperature and diode voltage versus diode temperature, respectively.

Figure 19: Diode voltage temperature



### 6 Characterization results

Figure 20: Bandwidth up to 5.5GHz



The bandwidth is measured with a constant input level calibrated at DC to obtain -1dBFS.

Figure 21: Crosstalk between channels

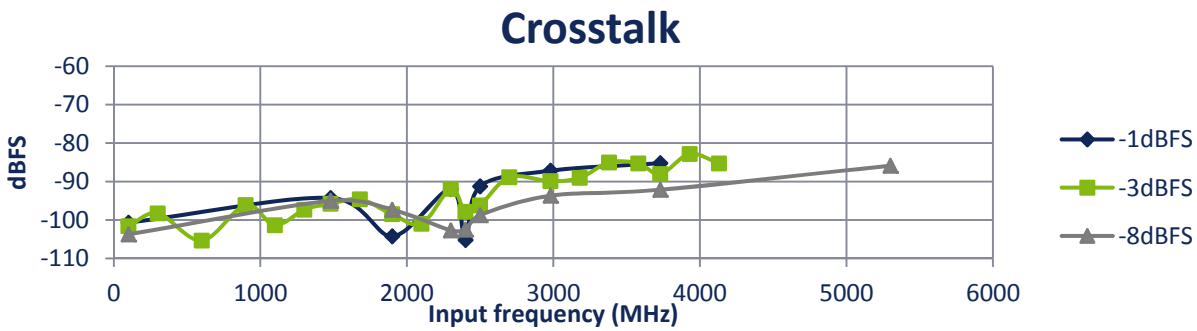


Figure 22: INL performance at Fclock = 3 GHz (Fs = 1.5 GSps)

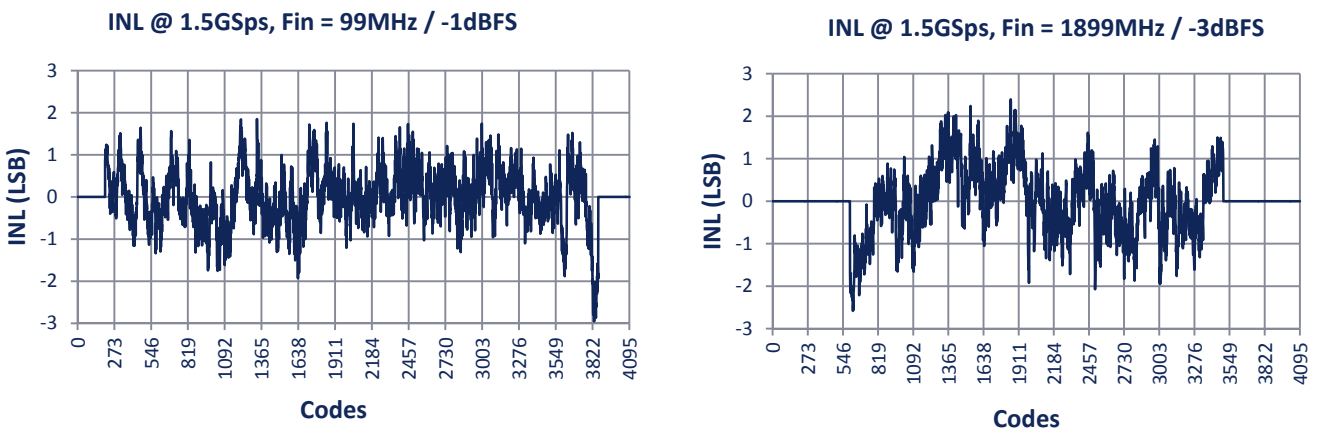




Figure 23: FFT performance vs input frequency in typical conditions @ Fclock = 3 GHz & Fclock = 3.2GHz

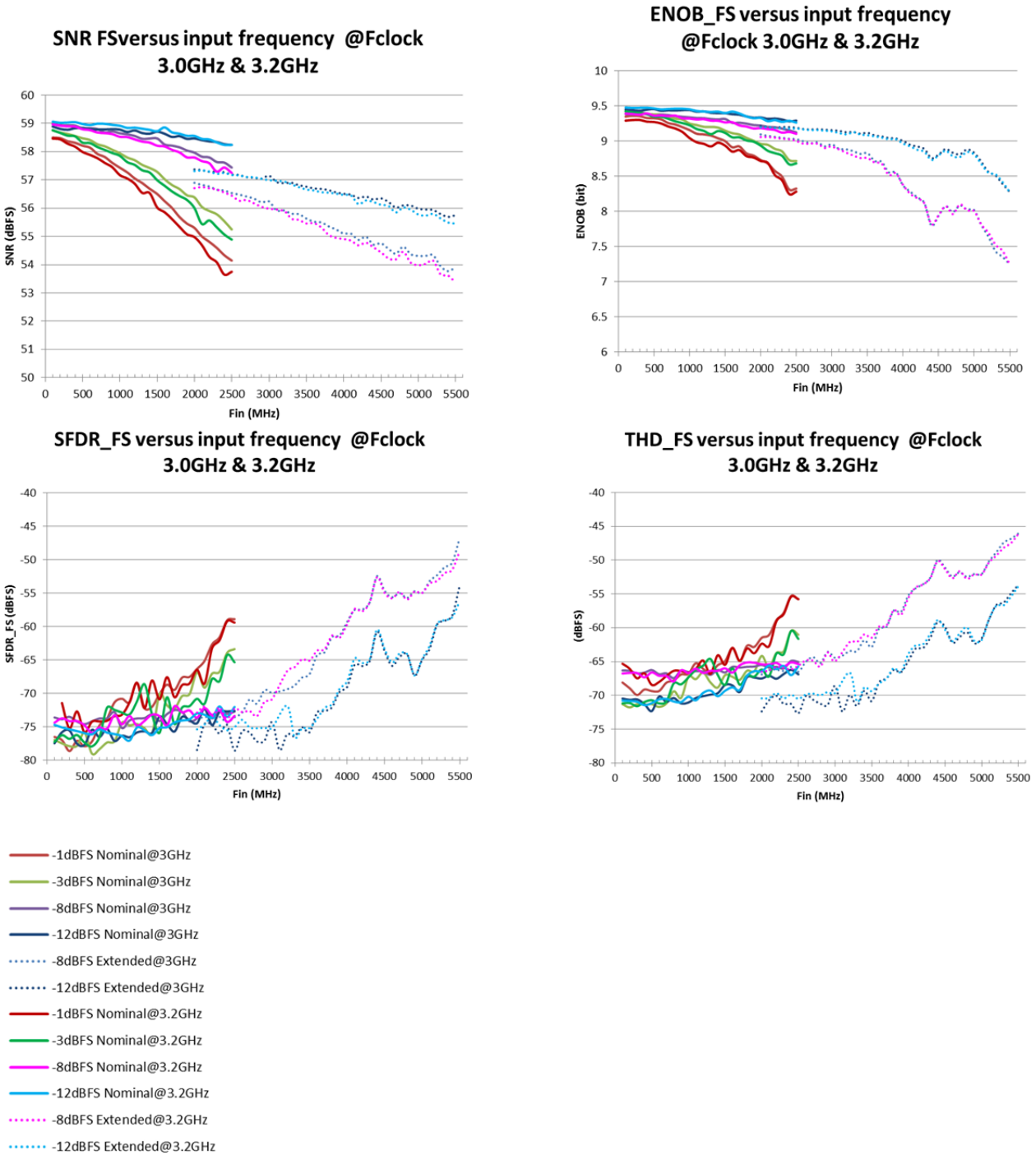


Figure 24: FFT performance vs temperature @ Fclock = 3.2GHz

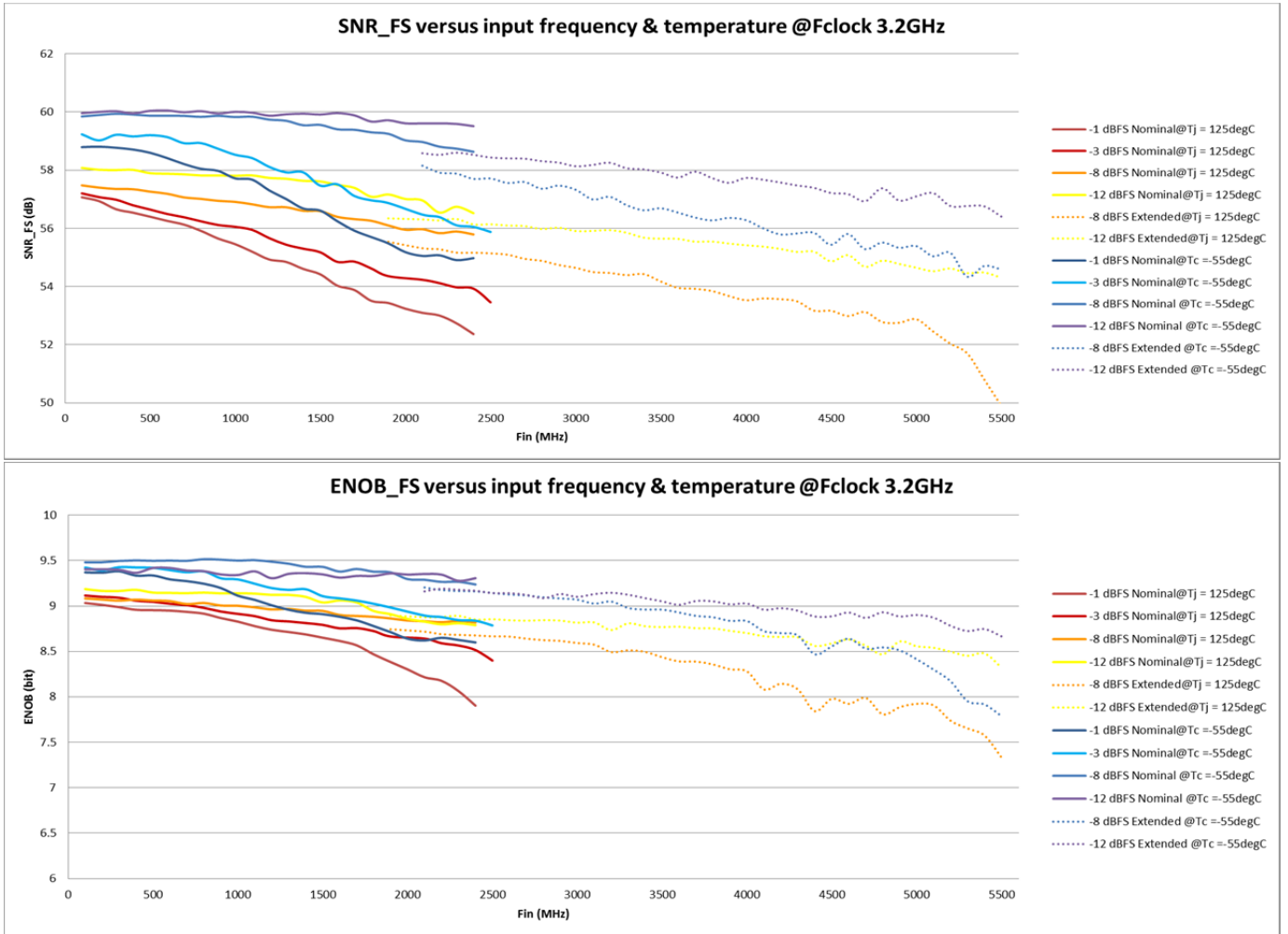


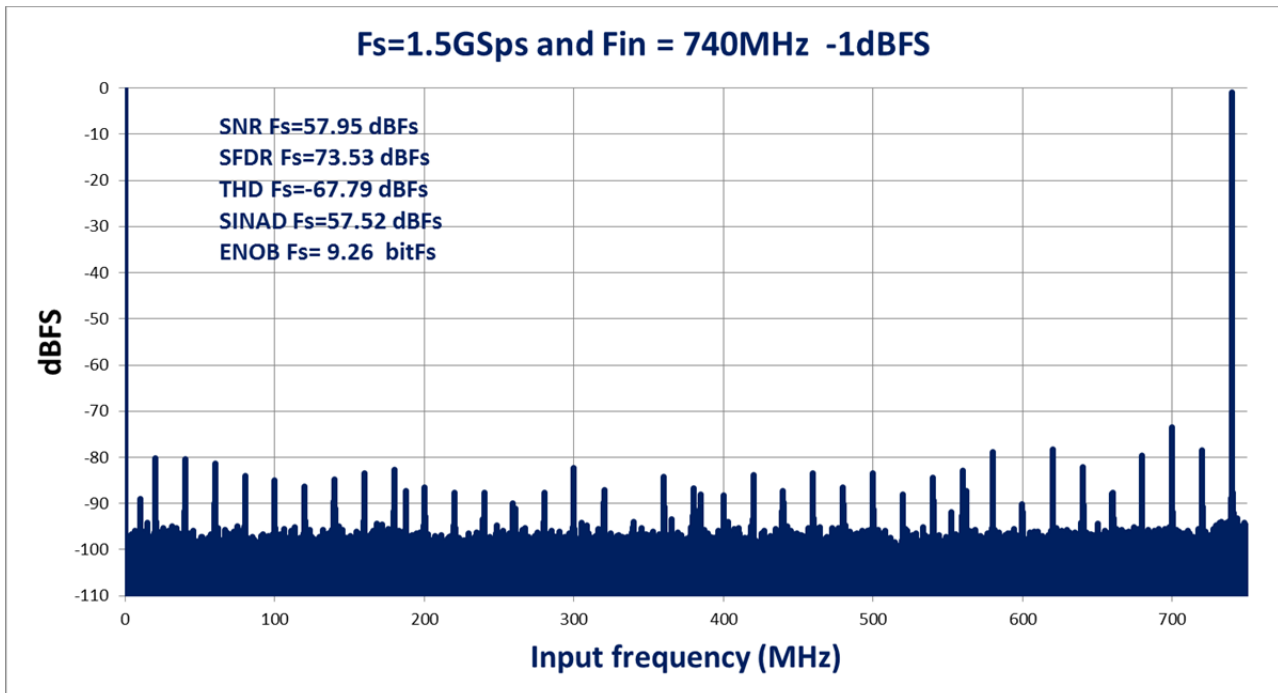
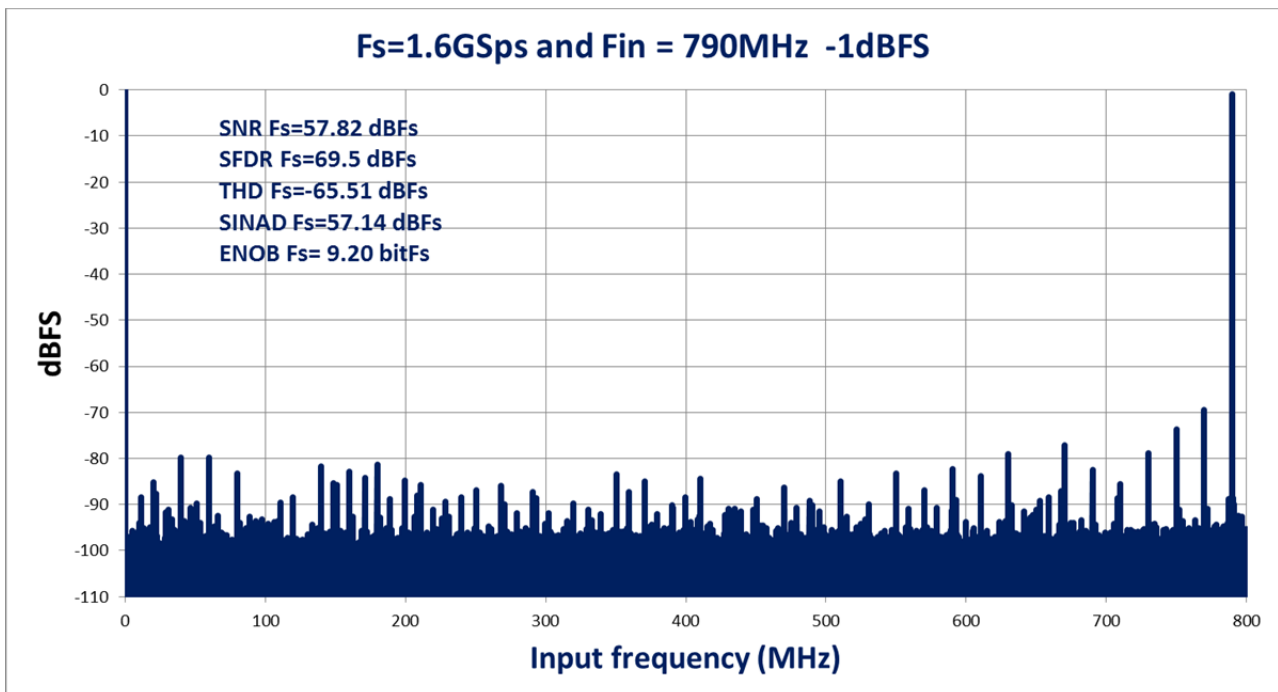
Figure 25 FFT at 1.5GSps and  $F_{in} = 740\text{MHz} / -1\text{dBFS}$ Figure 26 FFT at 1.6GSps and  $F_{in} = 790\text{MHz} / -1\text{dBFS}$ 

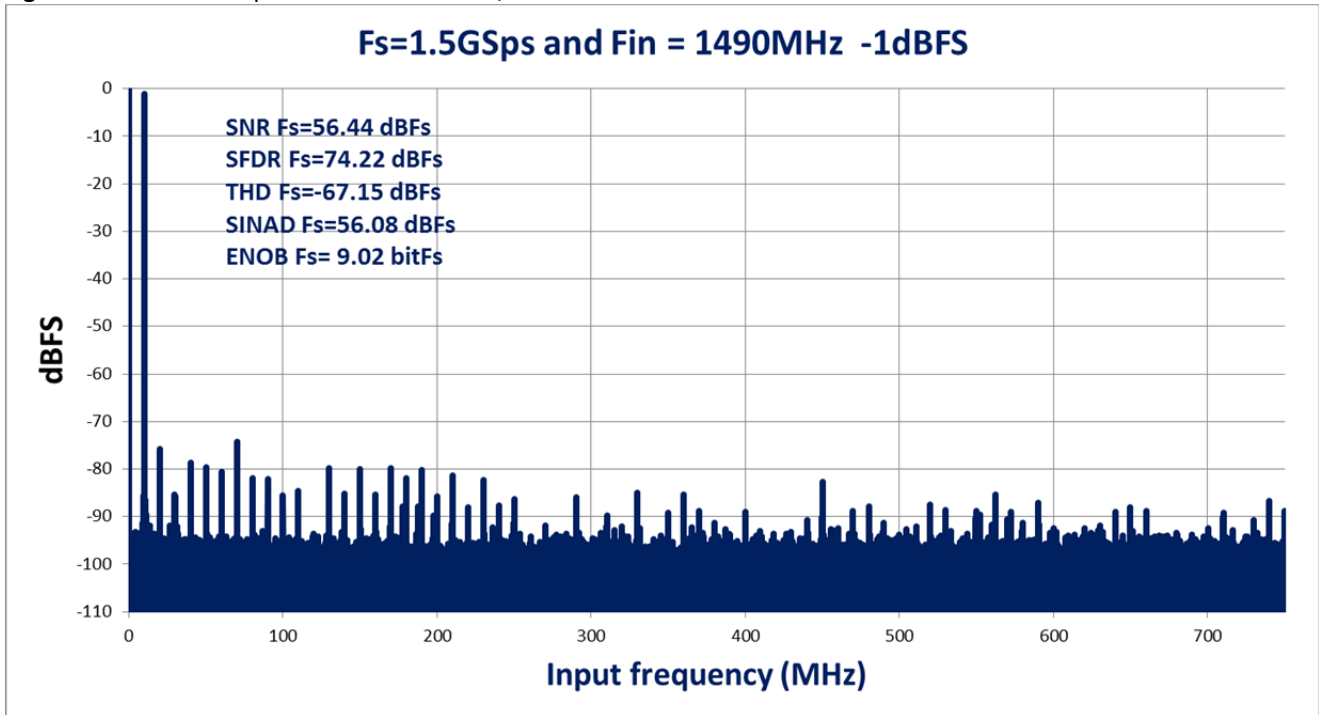
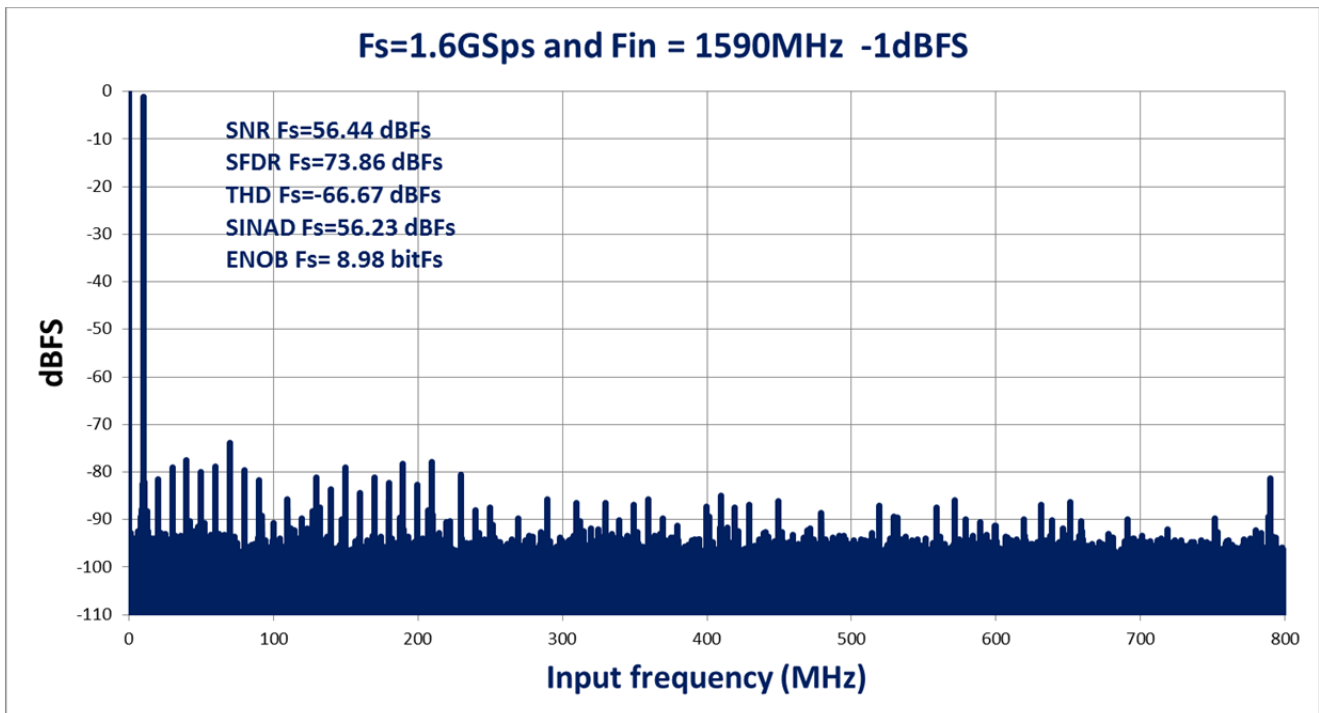
Figure 27: FFT at 1.5GSps and  $F_{in} = 1490\text{MHz} / -1\text{dBFS}$ Figure 28 FFT at 1.6GSps and  $F_{in} = 1590\text{MHz} / -1\text{dBFS}$ 

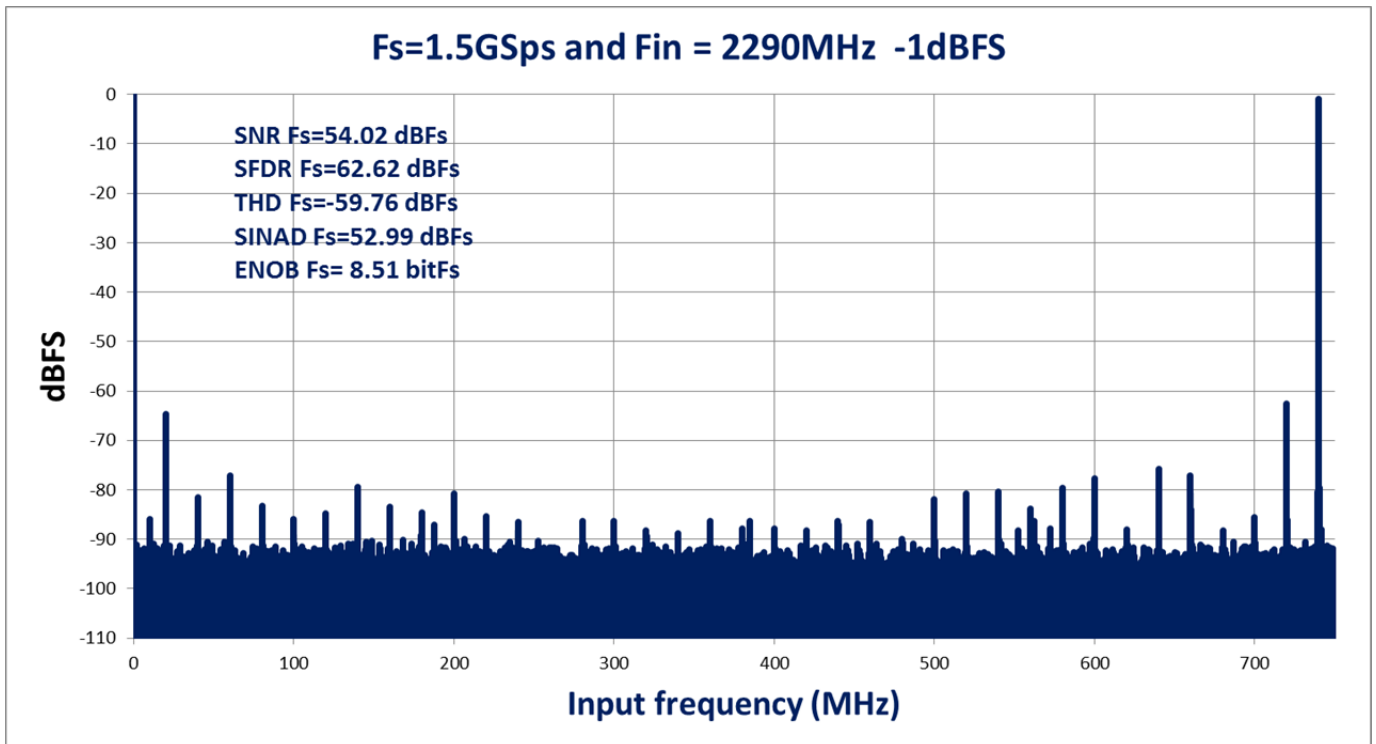
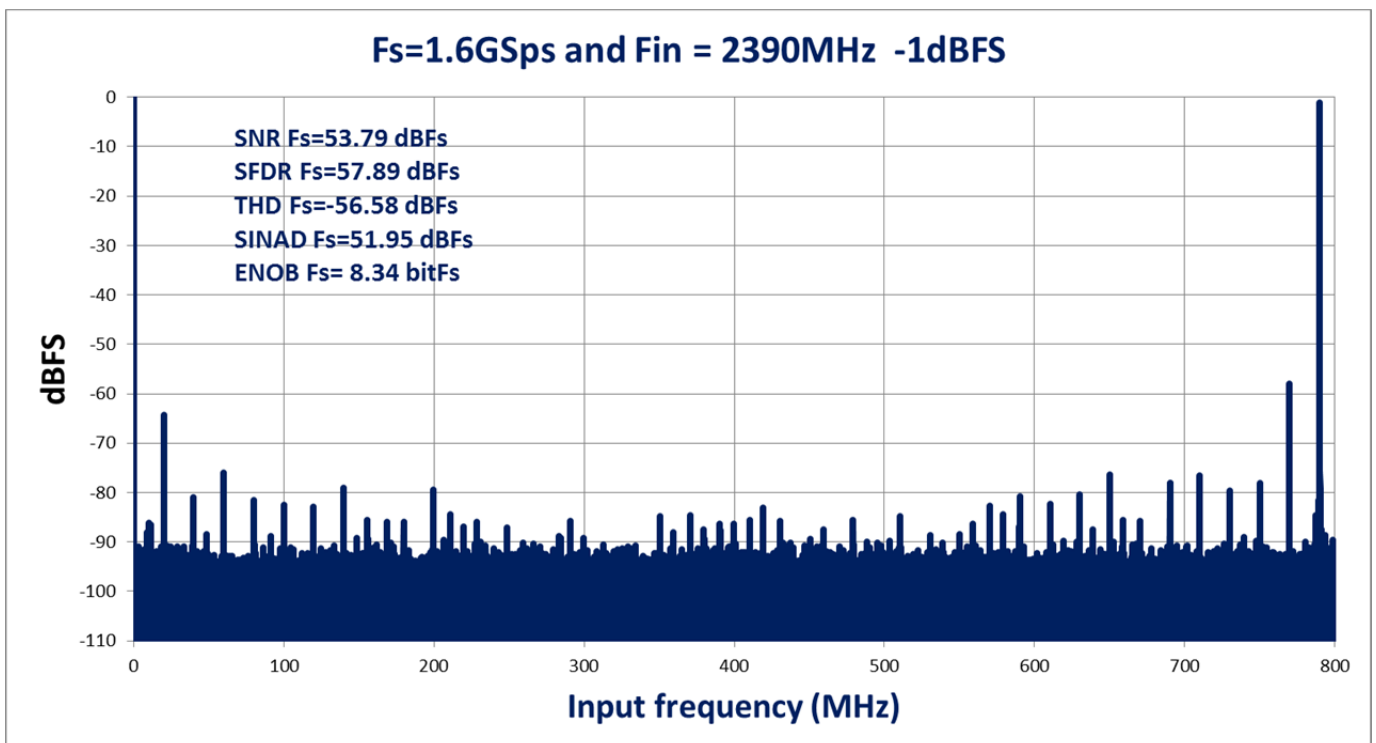
Figure 29 FFT at 1.5GSps and  $F_{in} = 2290\text{MHz} / -1\text{dBFS}$ Figure 30 FFT at 1.6GSps and  $F_{in} = 2390\text{MHz} / -1\text{dBFS}$ 

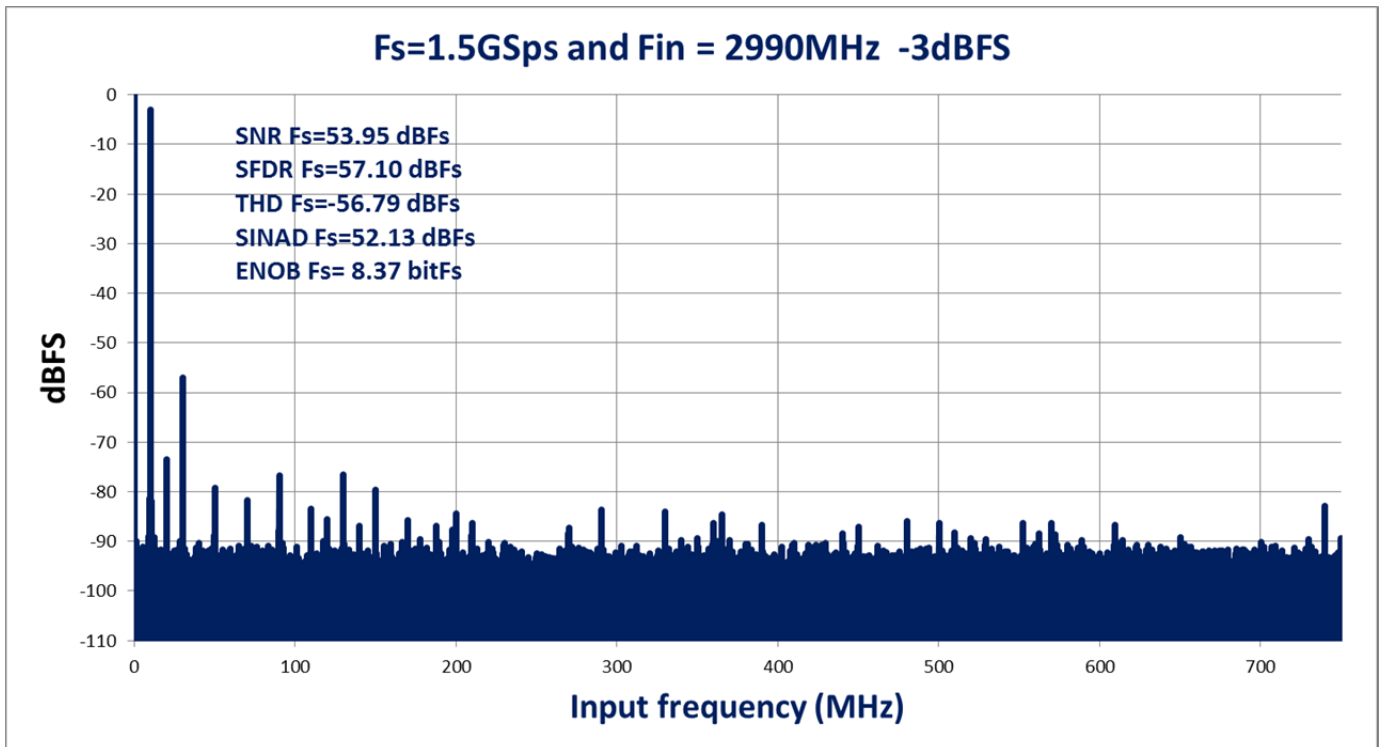
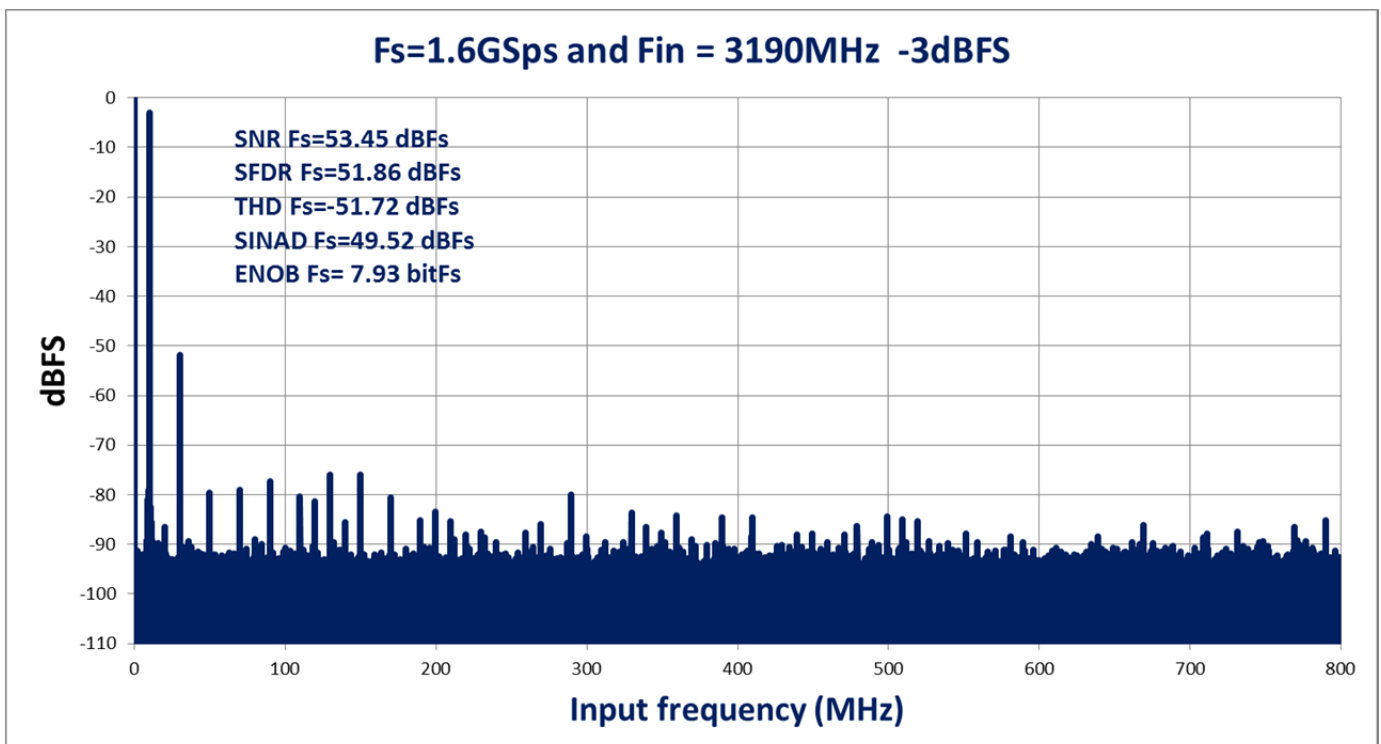
Figure 31 FFT at 1.5GSps and  $F_{in} = 2990\text{MHz} / -3\text{dBFS}$ Figure 32 FFT at 1.6GSps and  $F_{in} = 3190\text{MHz} / -3\text{dBFS}$ 

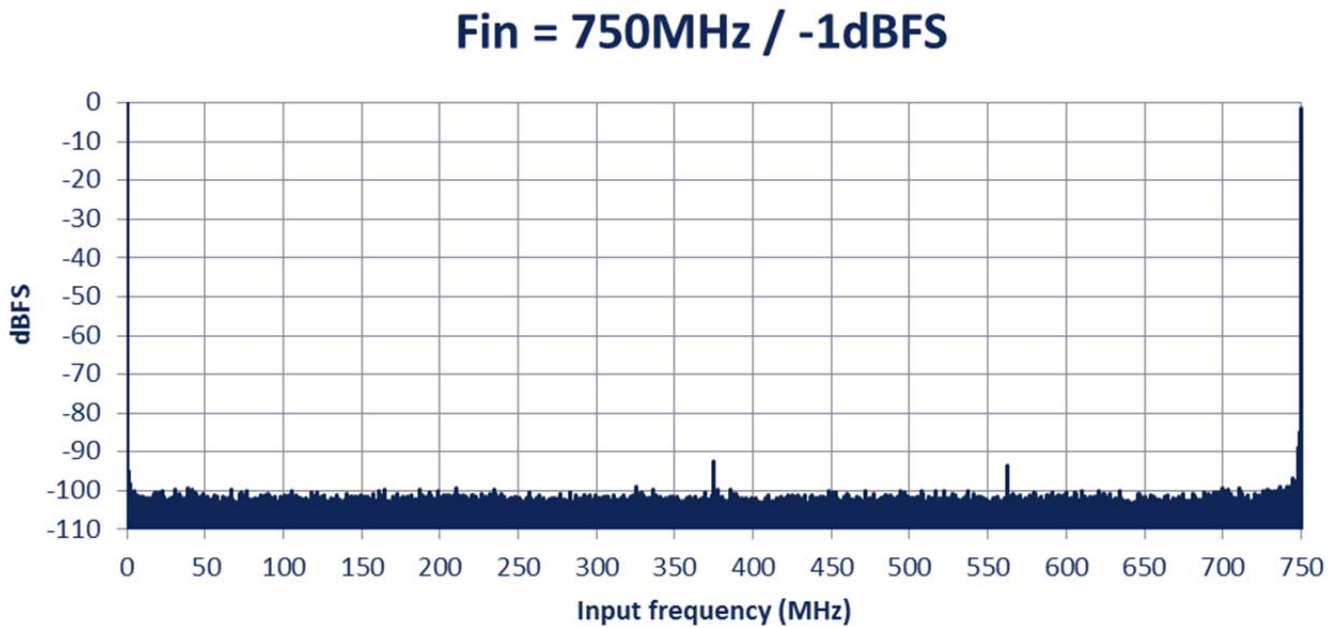
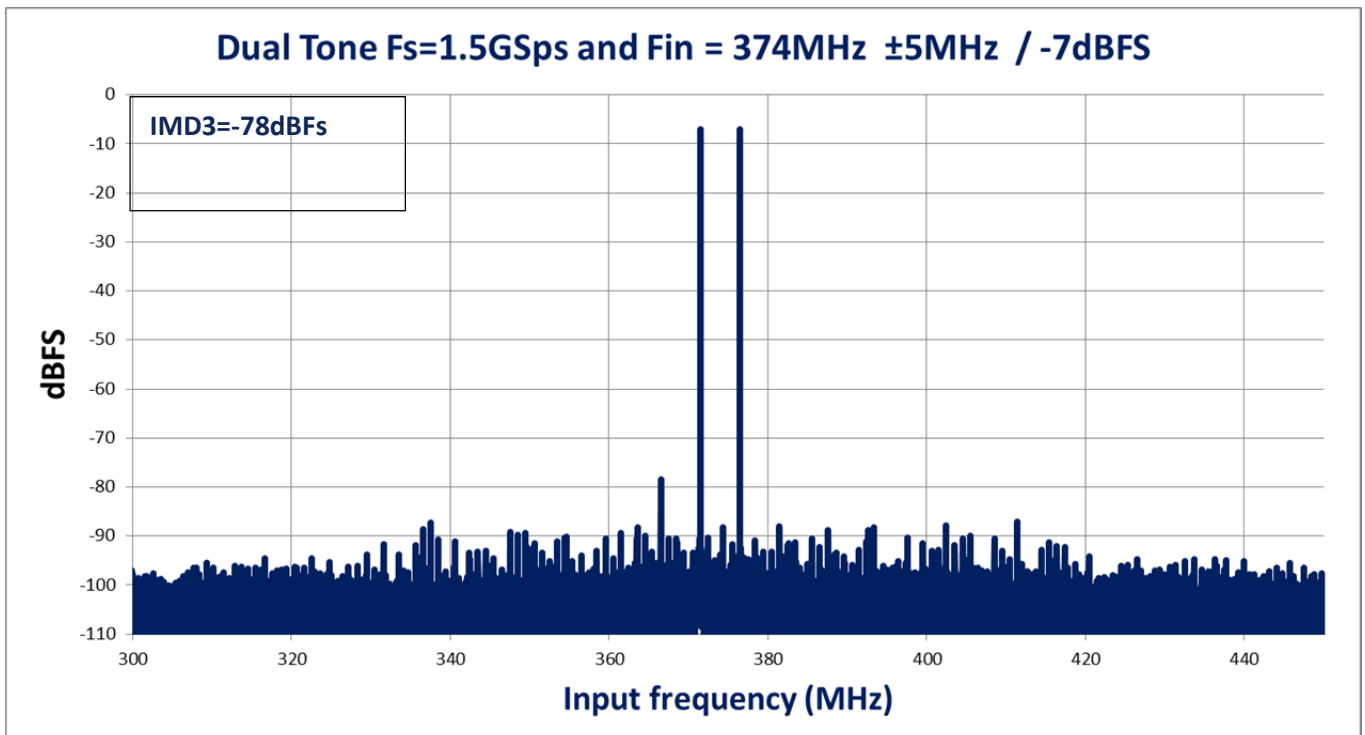
Figure 33: Spectral purity at  $F_s=1.5\text{GSps}$  and  $F_{in} = 750\text{MHz} / -1\text{dBFS}$ Figure 34 IM3 at  $F_s=1.5\text{GSps}$  and  $F_{in} = 374\text{MHz} \pm 5\text{MHz} / -7\text{dBFS}$ 

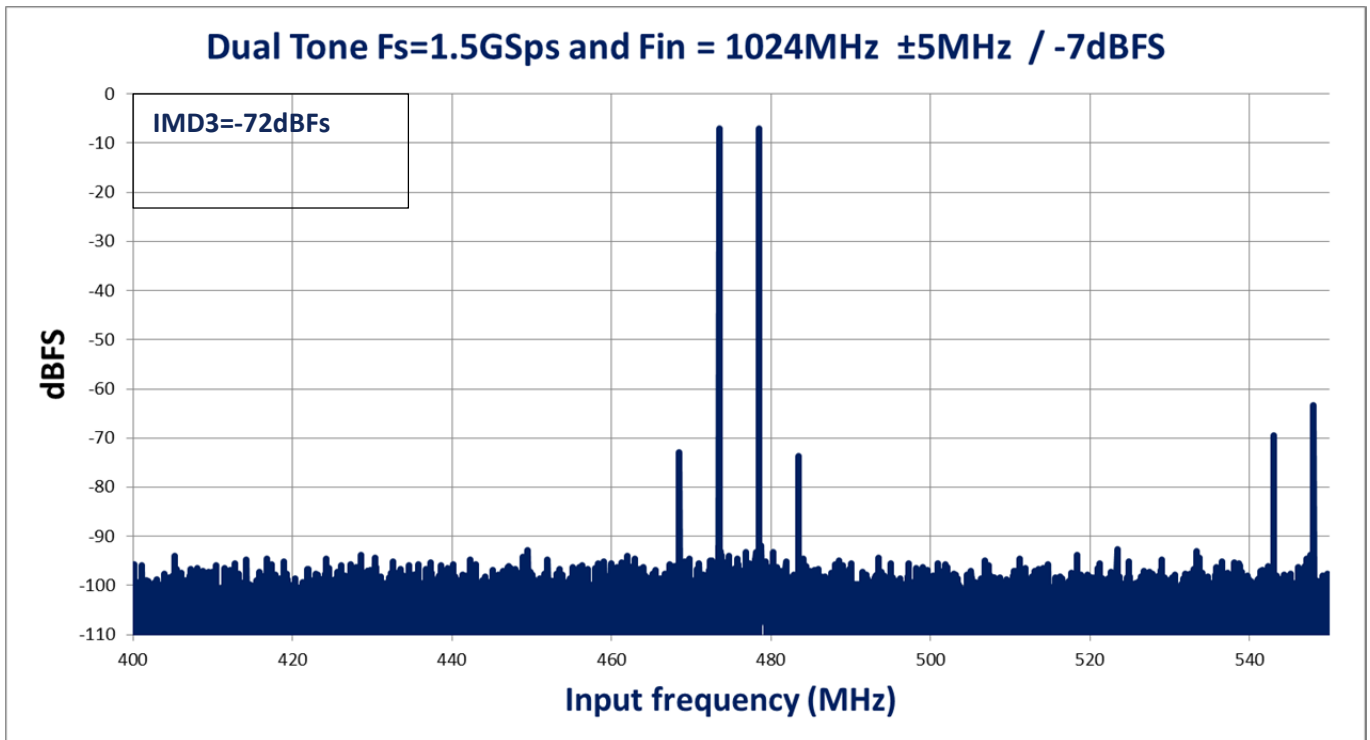
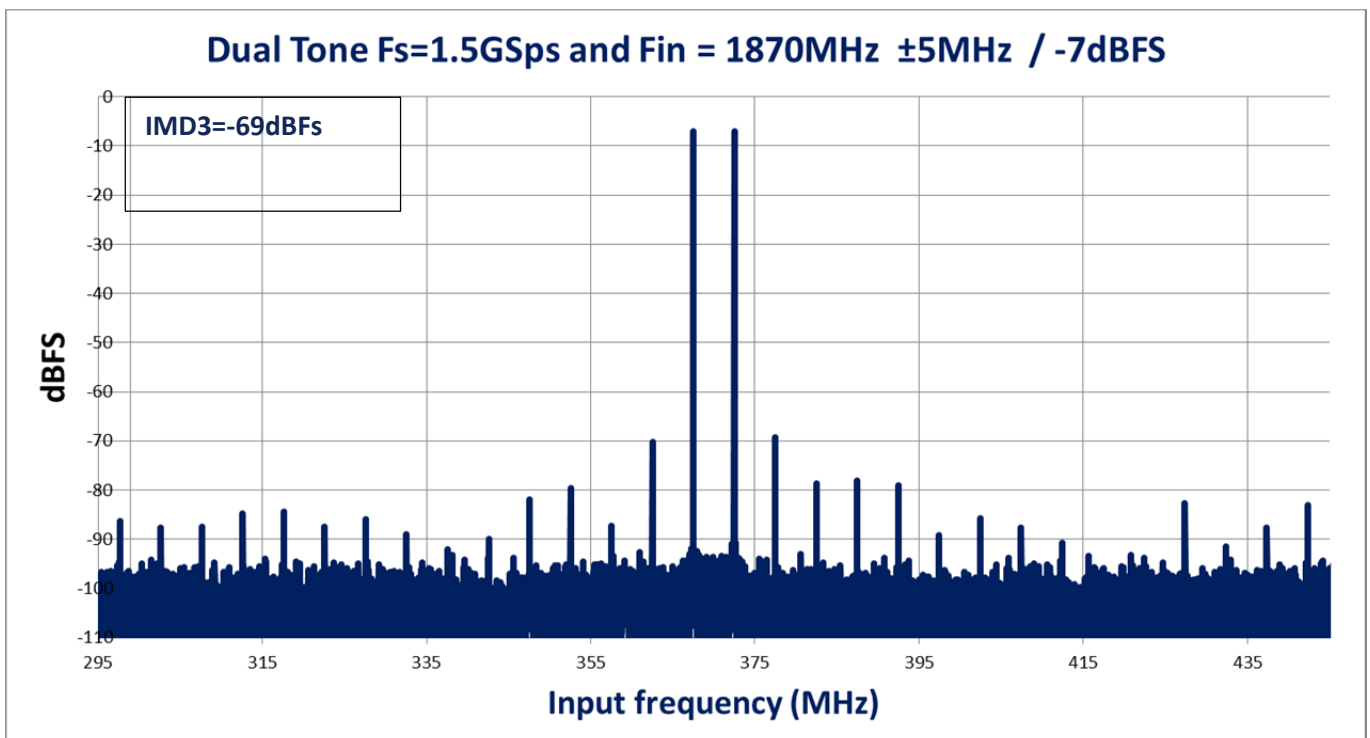
Figure 35 IM3 at  $F_s=1.5\text{GSps}$  and  $F_{in} = 1024\text{MHz} \pm 5\text{MHz} / -7\text{dBFS}$ Figure 36 IM3 at  $F_s=1.5\text{GSps}$  and  $F_{in} = 1870\text{MHz} \pm 5\text{MHz} / -7\text{dBFS}$ 



Figure 37 IM3 at  $F_s=1.5\text{GSps}$  and  $F_{in} = 2620\text{ MHz } \pm 5\text{MHz} / -9\text{dBFS}$

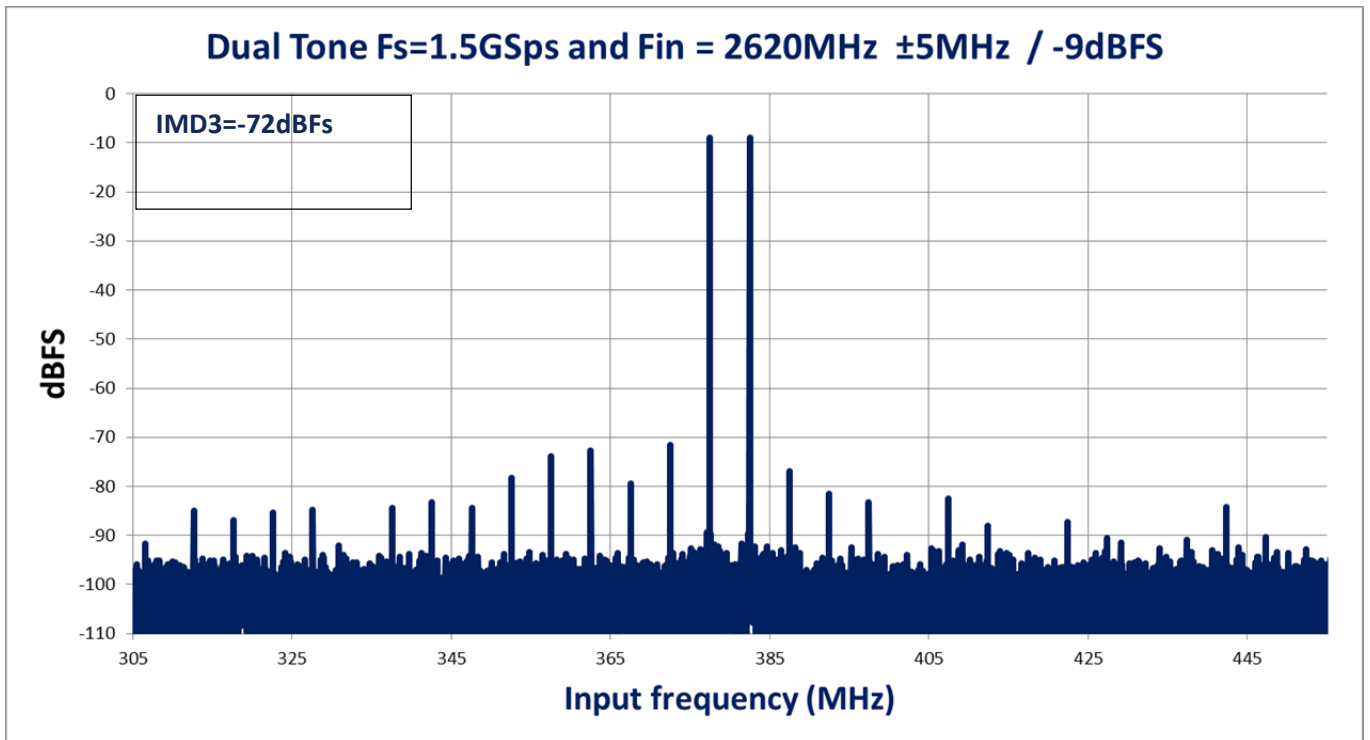
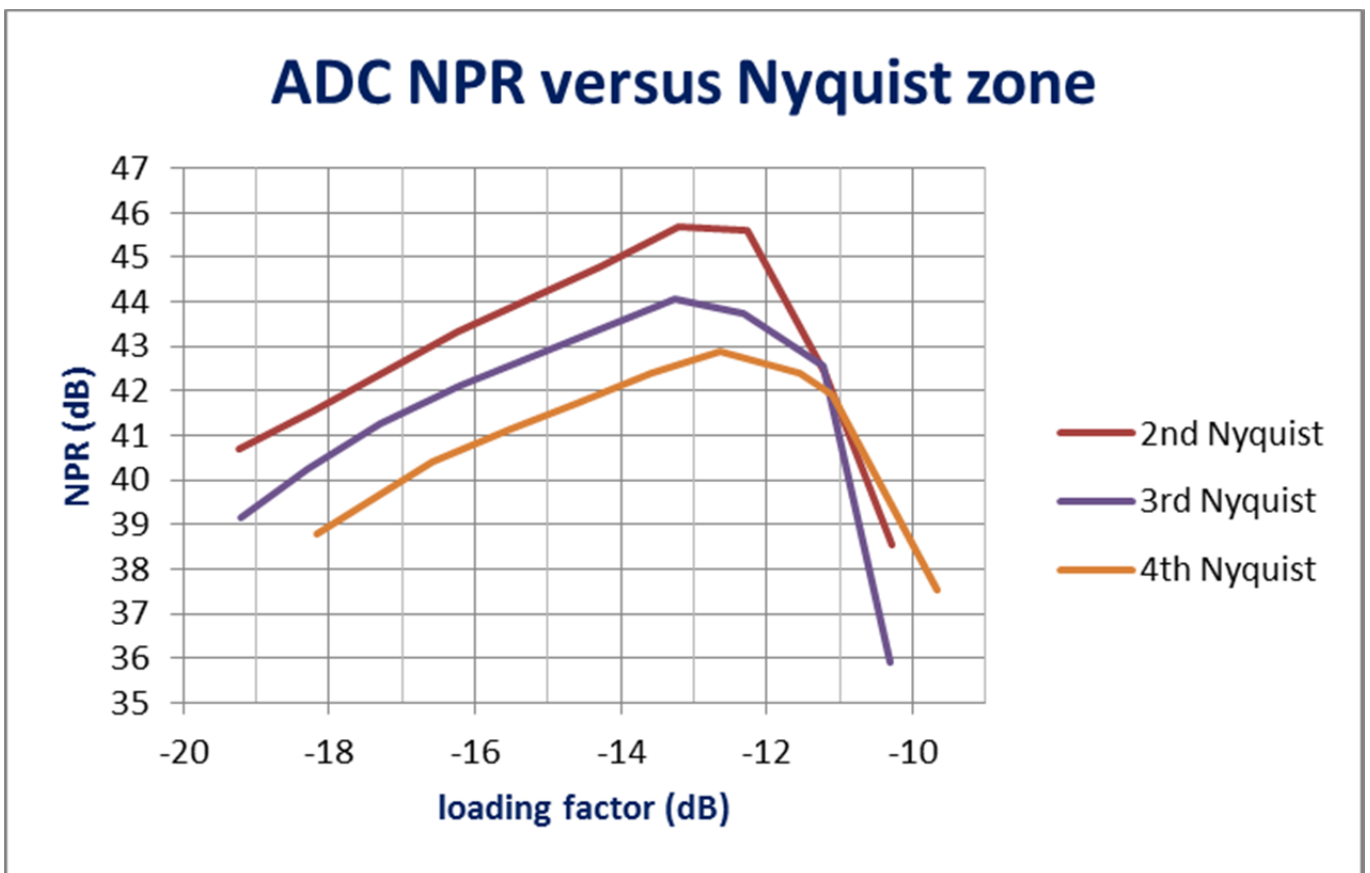


Figure 38 ADC NPR versus Nyquist zone and loading factor



## 7 Application information

### 7.1 Power supplies recommendation and decoupling

The ADC can work with a single rail. It is recommended to use ferrite and decoupling capacitance to avoid power supply pollution.

For VCCIOXn (X = H or L; n = 1 or 2), each supply should have 6x10nF decoupling capacitor. This means that in DEMUX 1:1, there are a total of 12x10nF decoupling capacitor on the VCCIO supplies and 24x10nF decoupling capacitor in DEMUX 1:2.

All grounds pins have to be connected on PCB but locally under the component, a slit between AGND and DGND (analog and digital ground) is preferred. Merging ground plane is also possible.

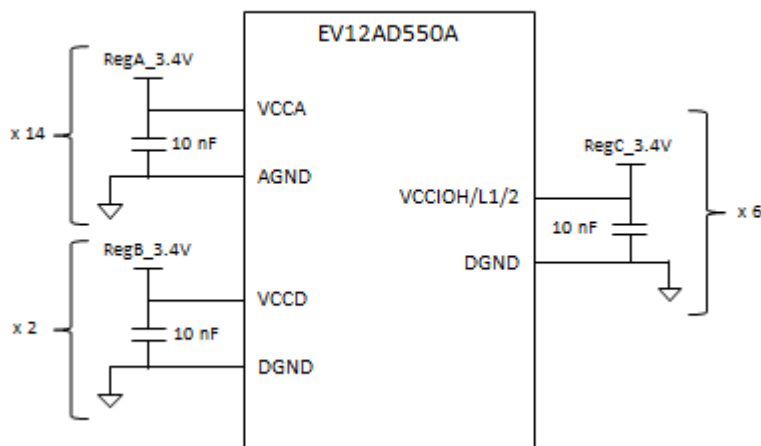


Figure 39: Decoupling with separate supplies

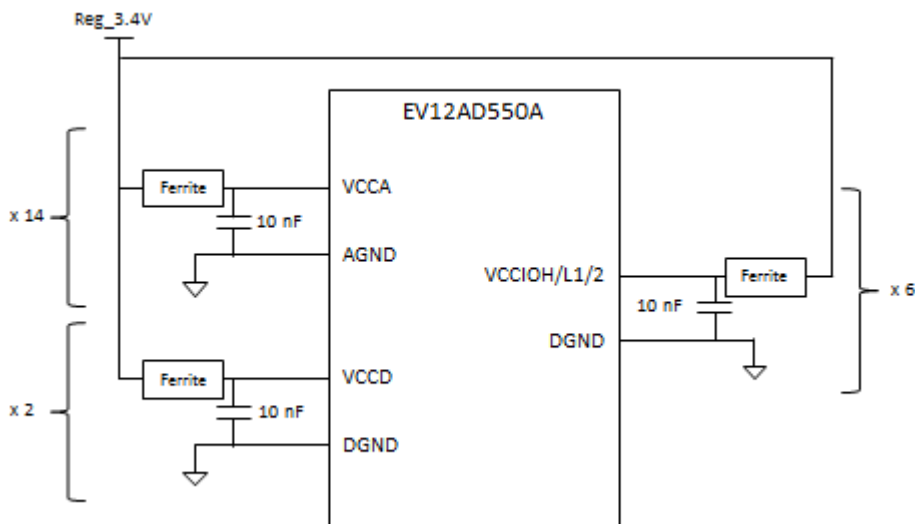
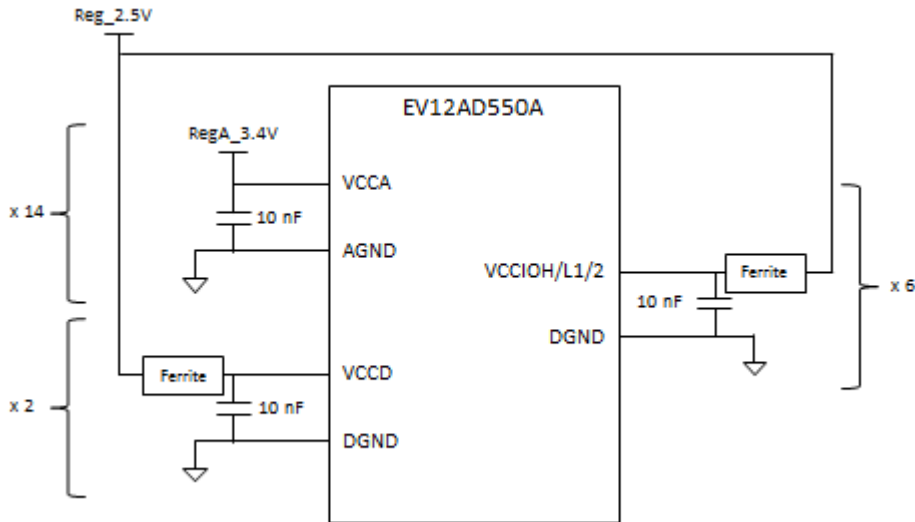


Figure 40: Decoupling with single supply at 3.4V



**Figure 41:** Decoupling with dual supplies at 3.4V and 2.5V

Supplies settling time should be faster than 10ms. No specific power sequencing is required.

## 7.2 Analog inputs

The analog inputs  $AIN_p$ ,  $AIN_N$  and  $BIN_p$ ,  $BIN_N$  can be DC coupled or AC coupled. The phase and amplitude imbalance on the inputs ( $XIN_p$  compared to  $XIN_N$ ) have an impact on the linearity performance of the device. The input driver should be chosen to minimize these effects and the trace length should be matched between  $XIN_p$  and  $XIN_N$ .

## 8 Ordering information

Table 19: Prototypes

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12AD550BLG	LGA	Ambient	Prototype	
EVX12AD550BGC	CCGA	Ambient	Prototype	

Table 20: Engineering models (EM)

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AD550BMLG	LGA	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	Standard	
EV12AD550BMGC	CCGA, Sn15Pb85	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	Standard	

Table 21: Engineering and qualification models (EQM):

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AD550BMLGD/T	LGA	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	Standard + 168h burn-in	
EV12AD550BMGCD/T	CCGA, Sn15Pb85	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	Standard + 168h burn-in	

Table 22: Flight models (FM):

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AD550BMLG-V	LGA	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	ESCC9000, QML-V compliant	
EV12AD550BMGC-V	CCGA, Sn15Pb85	T <sub>c</sub> -55°C, T <sub>j</sub> +125°C	ESCC9000, QML-V compliant	

## 9 Revision history

Issue	Date	Comments
A	February 2018	Issued from DATASHEET 1173D EV12AD550A
B	February 2019	<p>All pages modified for typos or miscellaneous precisions. Particularly performance tables updated vs characterization results.</p> <p>§3.4, table 6:            Power supply current in DEMUX 1:1, 1:2 and full standby mode: <math>I_{CCA}</math> and (<math>I_{CCD}</math> min) improved.            Power dissipation in full standby mode: updated typical from 1.9 to 1.6 W and max from 2.0 to 2.1 W (DEMUX 1:1) and typical from 2.3 to 1.9 W (DEMUX 1:2).</p> <p>LVDS OUTPUT</p> <p>Full swing: test condition updated            Common mode voltage <math>V_{OCM}</math> from 1.23 to 1.2 V min and from 1.48 to 1.55 V max</p> <p>Reduced swing:            Common mode voltage <math>V_{OCM}</math> from 1.25 to 1.2 V min and from 1.5 to 1.55 V max            Logic low: from 1.35 V to 1.4 V max            Logic high: from 1.4 V to 1.35 V min</p> <p>§3.5, table 7: Differential Non Linearity improved from (-0.9/+3 LSB) to (-0.5/+1.5 LSB)</p> <p>§3.5, table 8:            Gain flatness (+/- 0.5dB) updated from 1000 to 900 MHz for NBW and from 1100 to 1000 MHz for EBW.</p>

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