Atmel ADCs and DMUXes Synchronization in the Case of a Multi-channel Application

1. Introduction

In the case of a multichannel application, it might be necessary to synchronize two (ADC + DMUX) subsystems or more within the same system. This requires some care with regards to both the design of the application board and of course the reset sequence considering all the timing issues and constraints.

This document applies to the:

- AT84CS001 10-bit 2.2 Gsps DMUX
- TS83102G0B 10-bit 2 Gsps ADC
- AT84AS008 10-bit 2.2 Gsps ADC
- AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX
- AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX

ADCs and DMUXes Synchronization

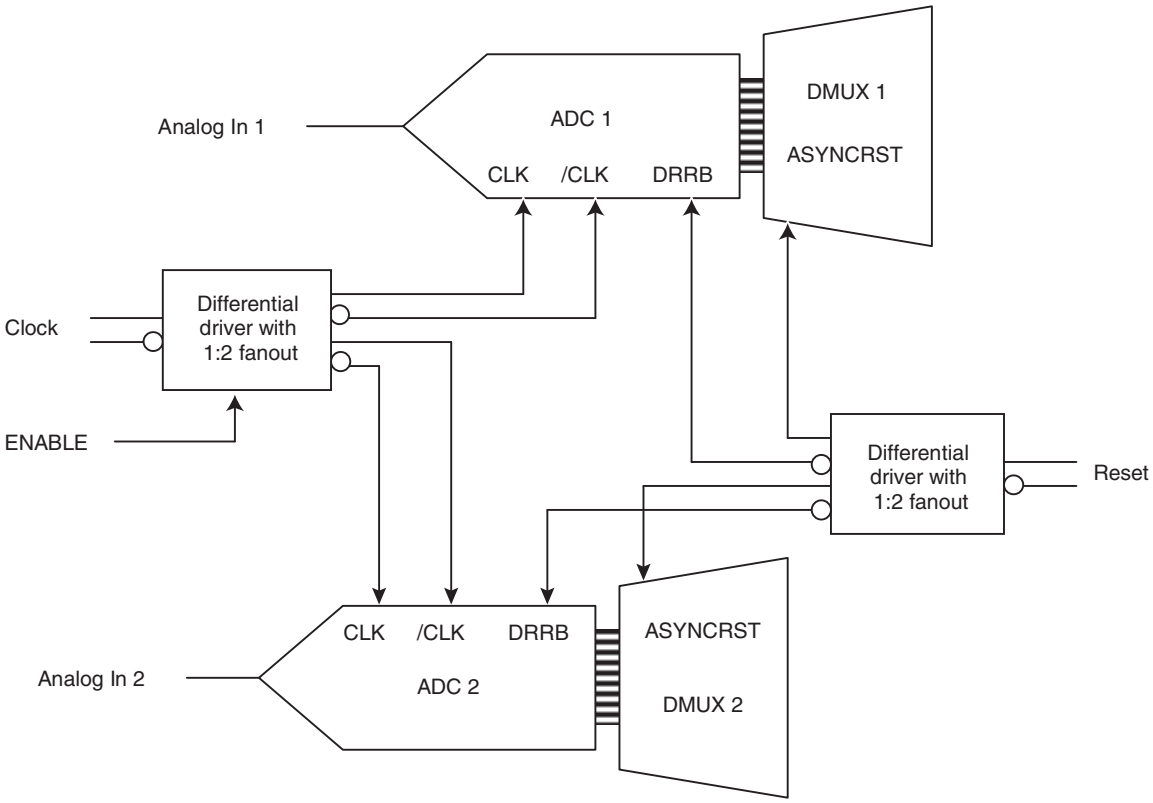
Application Note

5442A–BDC–11/05

2. Case Study: Double Channel Application

2.1 Block Diagram

Figure 2-1. Double Channel Application Principle Diagram

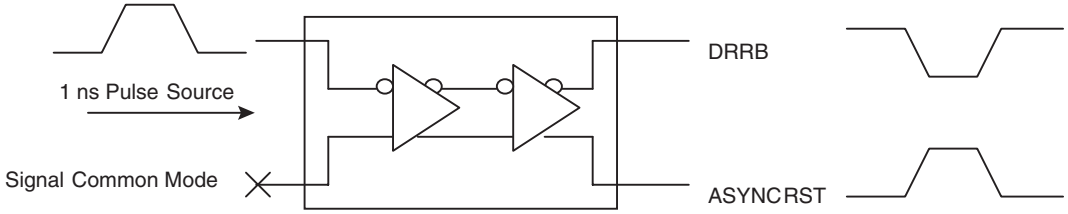


In this scheme, two drivers are necessary, one for the clock and one for the reset signals for both the ADCs and the DMUXes.

This driver used for the reset signals has to be a 1:2 fanout differential driver, allowing to use the positive output signal for the ASYNCRST reset of the DMUXes and the negative signal of the differential pair for the DRRB reset of the ADCs.

Each reset signal indeed works in phase opposition, allowing to use the two signals of the same differential pair to provide the reset signals to both the ADC and the DMUX at the same time (see Figure 2-2).

Figure 2-2. DRRB and ASYNCRST Driver Scheme



Although this seems more convenient as shown previously, it is not mandatory to apply the ADC and DMUX reset signals simultaneously. If not, the DRRB signals have to be asserted prior to the ASYNCRST and unasserted after the ASYNCRST is unasserted, as shown in Figure 2-3

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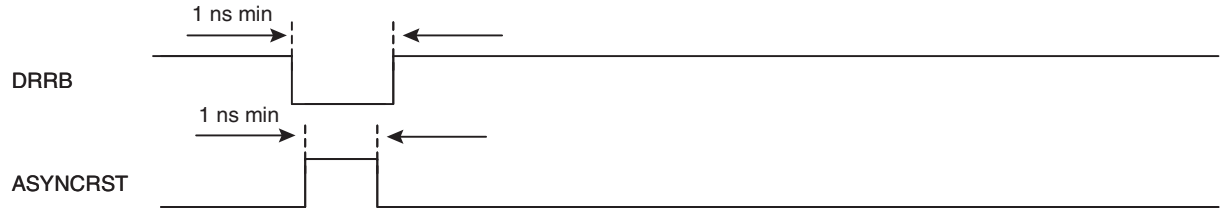
Figure 2-3. Reset Sequence (DRRB and ASYNCRST Not Simultaneous)



2.2 Reset Sequencing (Input Clock Held Low During Reset)

In this sequence, the most important thing is to ensure the setup and hold times of the ADC reset with respect to the sampling clock.

Note: It is the same sequence for standalone ADCs and DMUXes or for ADCs and DMUXes in the same package.

Since this sampling clock can be well above 1 Gsps (1.5 Gsps maximum with the AT84AS003 ADC, 2 Gsps maximum with the TS83102G0B and AT84AS004 ADCs, 2.2 Gsps maximum with the AT84AS008), corresponding to a clock period of less than 1 ns. Compared to the 400 ps setup and 500 ps hold times, it might be very tricky to ensure that both ADCs are reset at the same time within a few tens of ps. We therefore recommend to hold the input clock low during reset so that the setup and hold times are always satisfied for both ADCs and that the ADCs will restart synchronously after reset and after restart of the clock. It is indeed possible that after power up the two ADCs start with out of phase output clocks (as illustrated as an example on Figure 2-4 on page 4).

The DRRB reset applied to both ADCs at the same time while the input clock is held low ensures that the ADCs output clocks will be in phase after reset.

On the DMUX side, the ASYNCRST is required in the following cases:

- Modification of the DMUX settings (switching from 1:2 to 1:4 ratio for example)
- Ensure that the first data will be on port A

It is not required to start the DMUX after power up.

In the case of a synchronization of multiple channels, the ASYNCRST is used to ensure that the first data to be processed will be output on port A then port B, C and D (in the case of a 1:4 ratio).

Figure 2-4. Timing Diagram (ADC and DMUX in the Same Package)

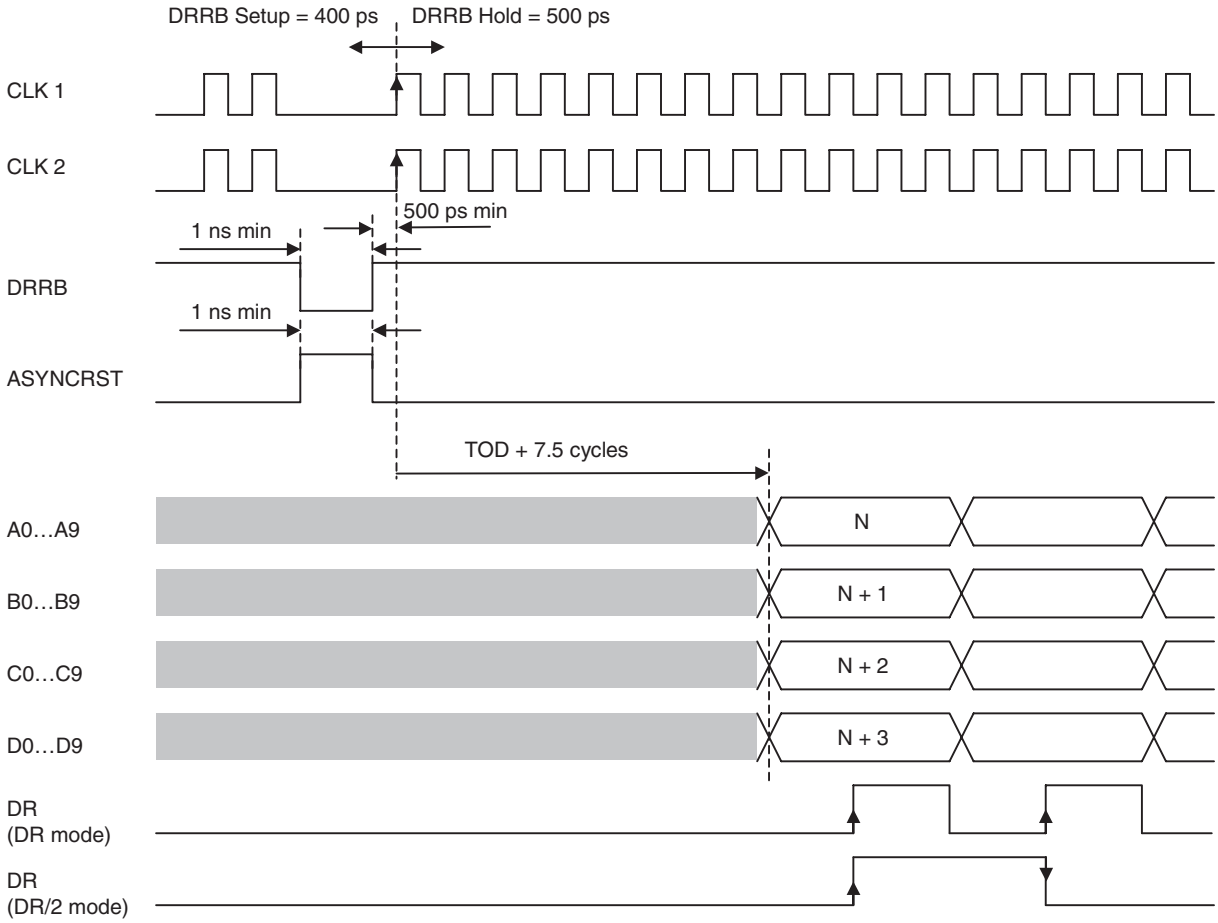
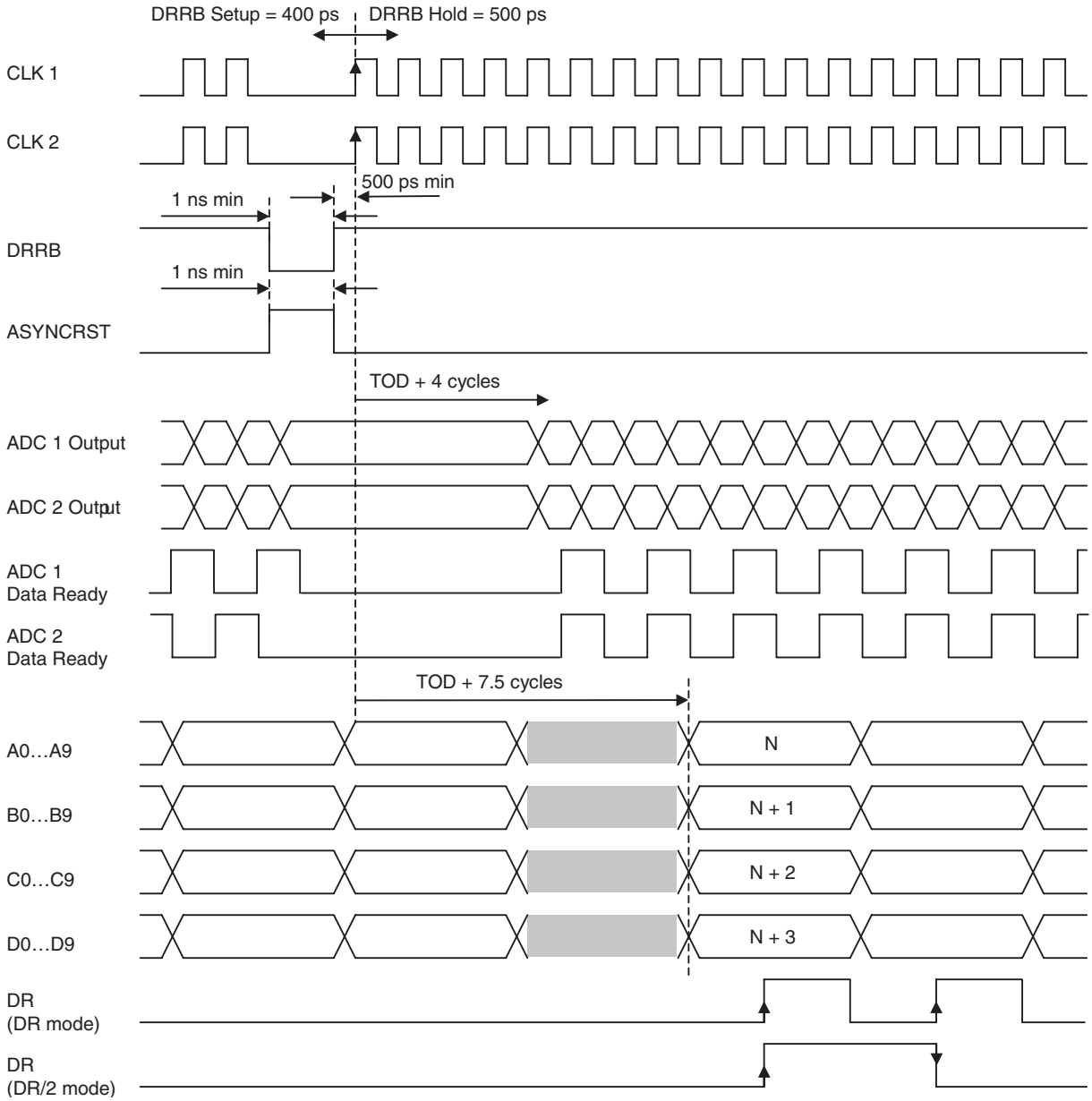


Figure 2-5. Timing Diagram (Standalone ADCs and DMUXes)



The advantage of this method is to relax the constraints on the timing between the reset signals and the clock but the main disadvantage is to add some jitter on the clock.

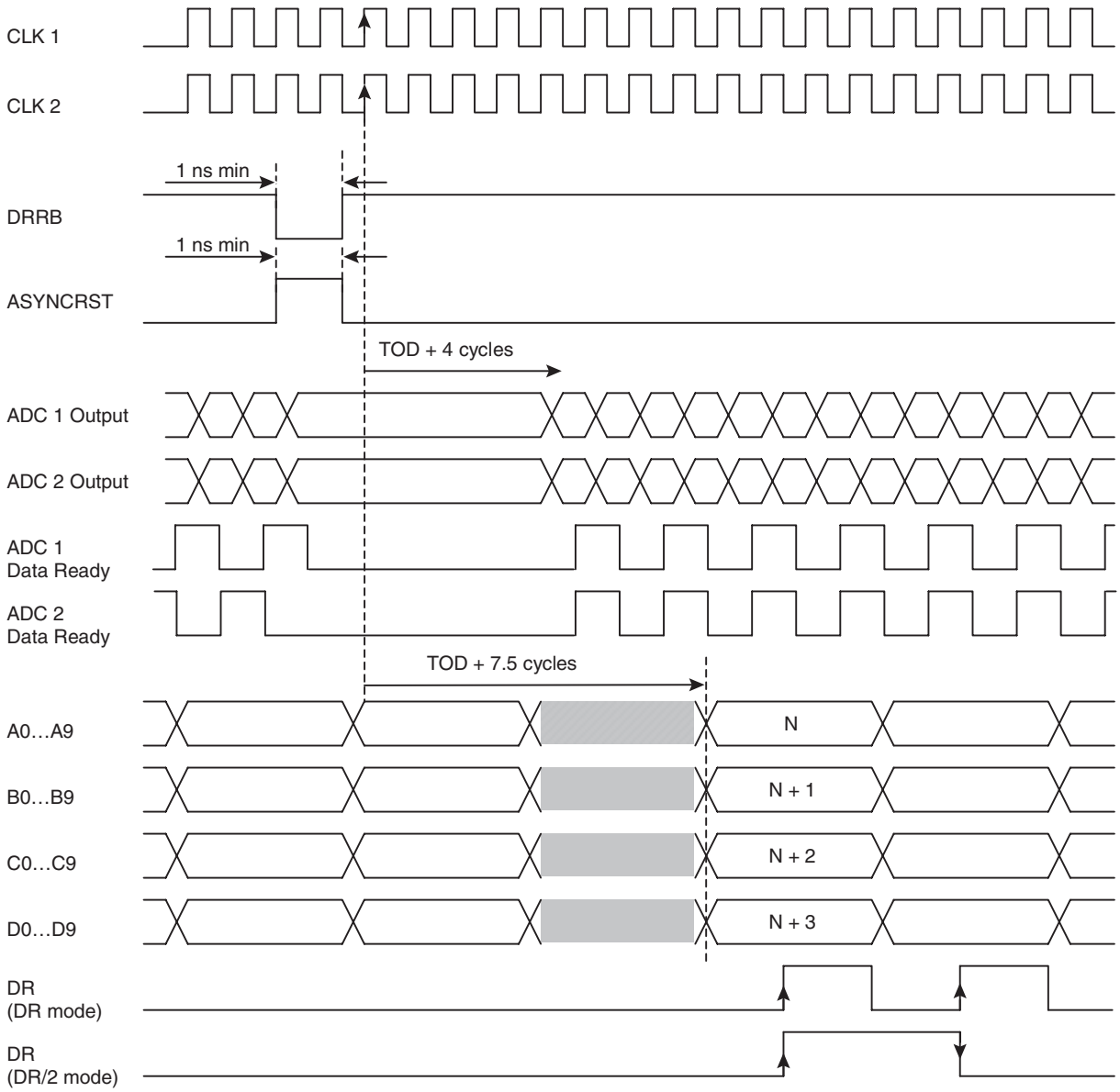
2.3 Reset Sequencing (Input Clock Not Held Low During Reset)

Although we recommend to hold the ADC input clock during reset and as this might be complicated to implement in an application (added jitter on the clock), it is possible to synchronize devices using the reset signals while the input clock is still toggling but there are timing requirements to satisfy very accurately.

In the case when the input clock is not held during reset, the operation between standalone ADC and DMUX and ADC and DMUX in the same device is different.

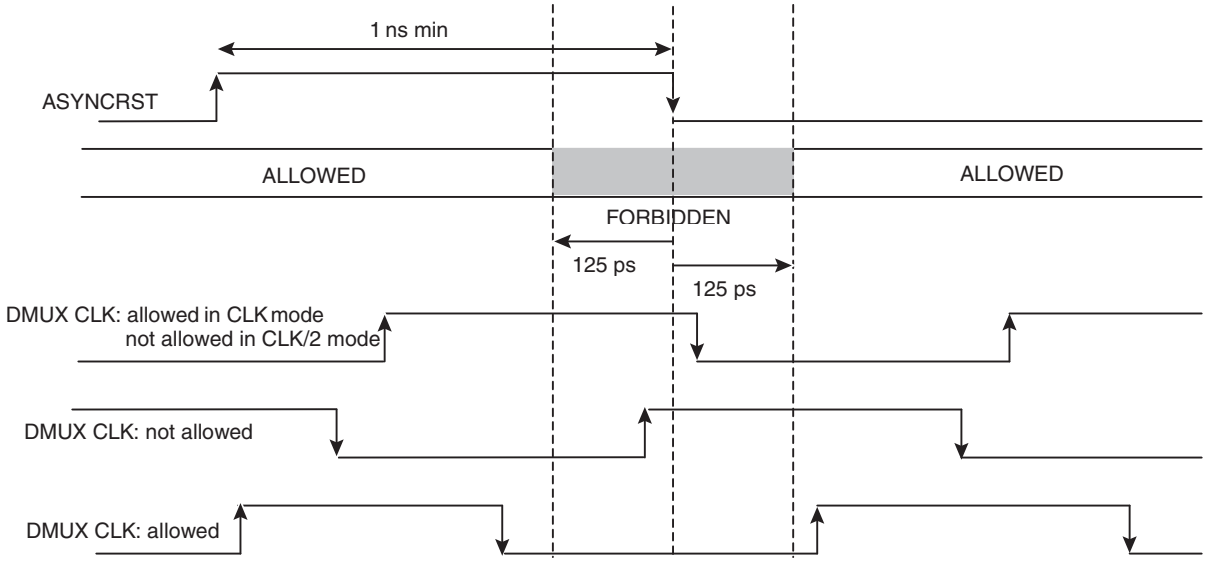
2.3.1 Standalone ADCs and DMUXes

Figure 2-6. DRRB and ASYNCRST Reset Timing Requirements



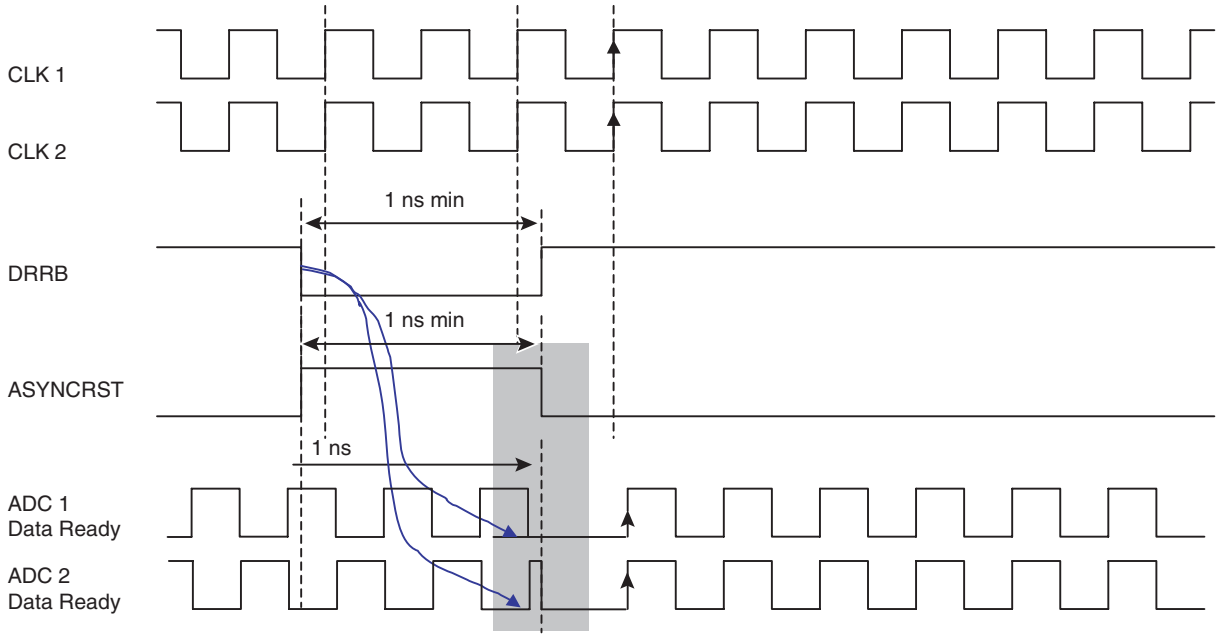
The following timing diagram gives the constraints on the ASYNCRST with respect to the DMUX input clock.

Figure 2-7. DMUX ASYNCRST Reset Timing Requirements



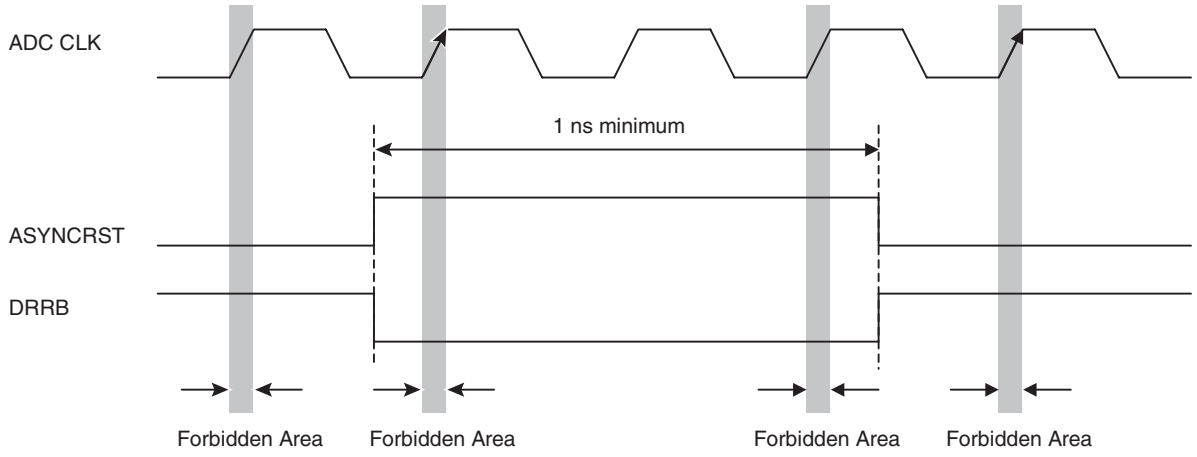
When the ADCs and DMUXes need to be synchronized, the DRRB reset of the ADC is used simultaneously with the ASYNCRST and therefore there is no risk that the DMUX input clock occurs in the forbidden zone defined around the asynchronous reset falling edge.

Figure 2-8. DMUX ASYNCRST Reset Timing Requirements



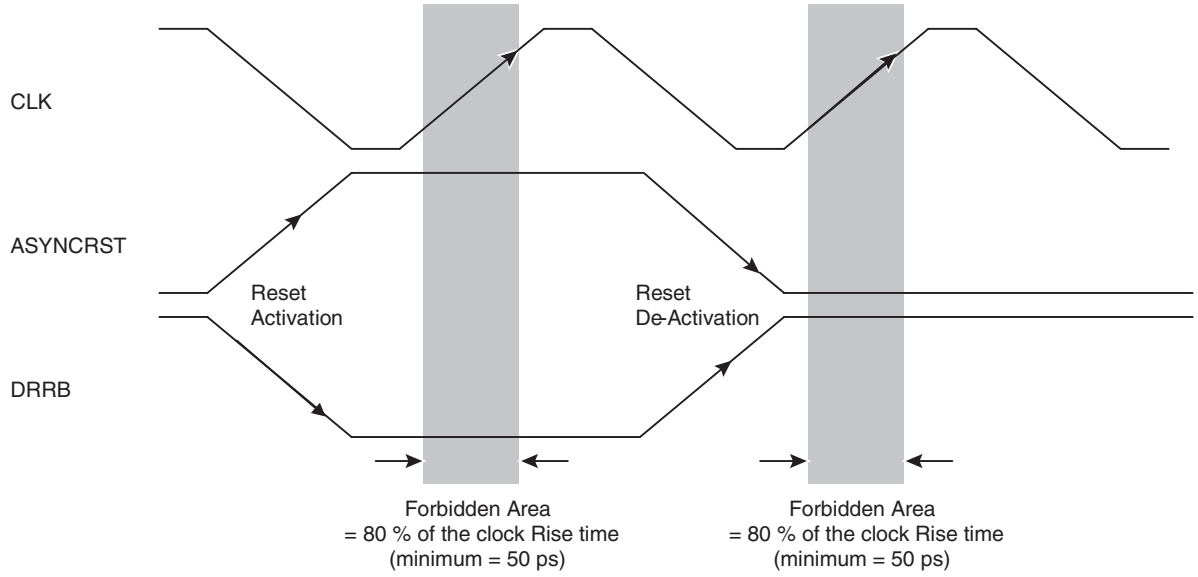
The only constraint is on the ASYNCRST and DRRB timings with respect to the ADC input clock, as described in the following figures.

Figure 2-9. Reset Timing Requirements



The reset (activation or de-activation) is taken into account on the clock edge marked with an arrow. The forbidden area applies for the rising edge of the clock.

Figure 2-10. Reset Forbidden Area



2.3.2 ADC and DMUX in the Same Device

Figure 2-11. Reset Timing Diagram, 1:2 Mode, Simultaneous Mode

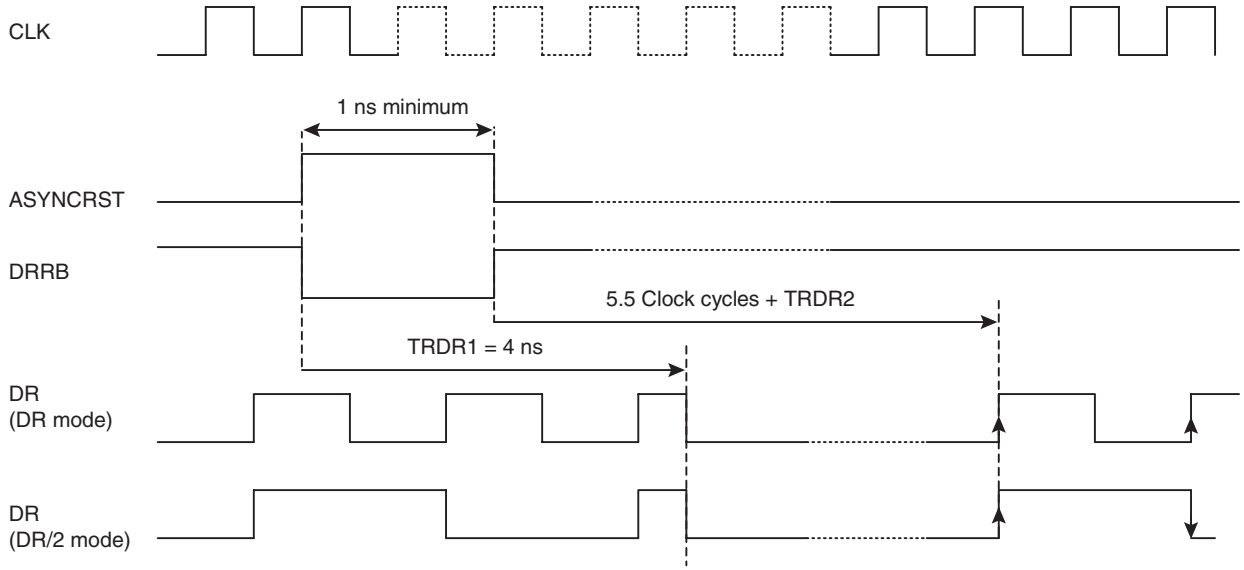


Figure 2-12. Reset Timing Diagram, 1:4 Mode, Simultaneous Mode

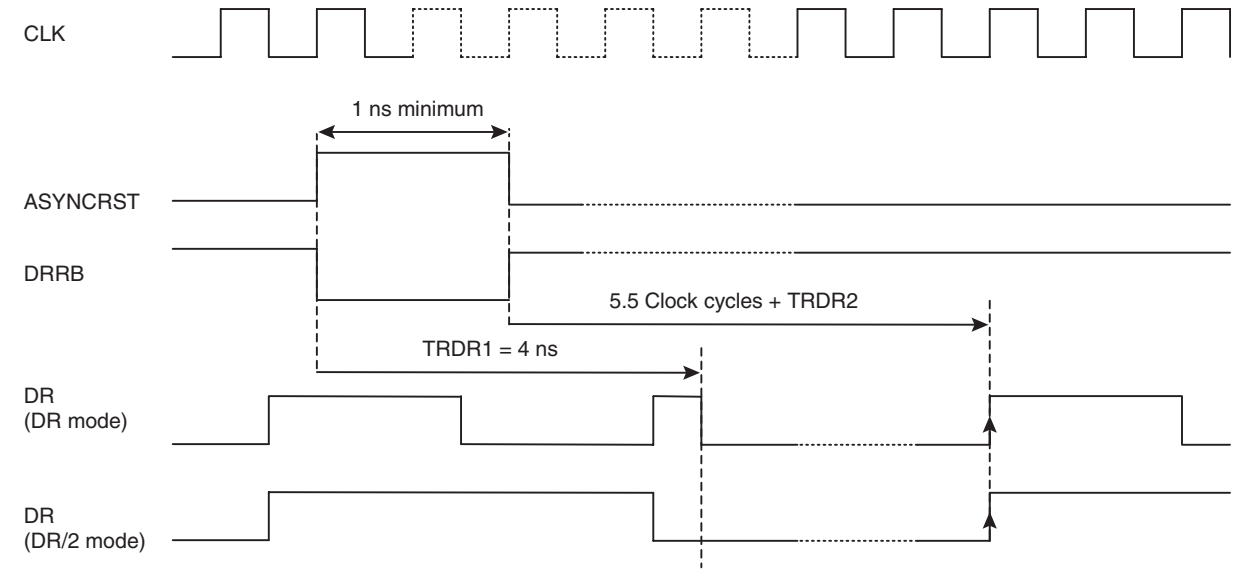
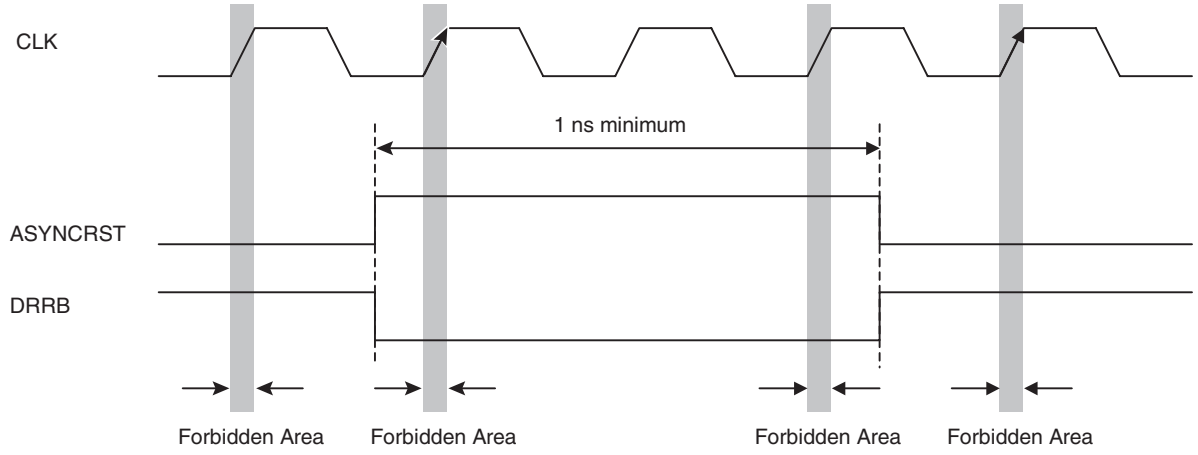
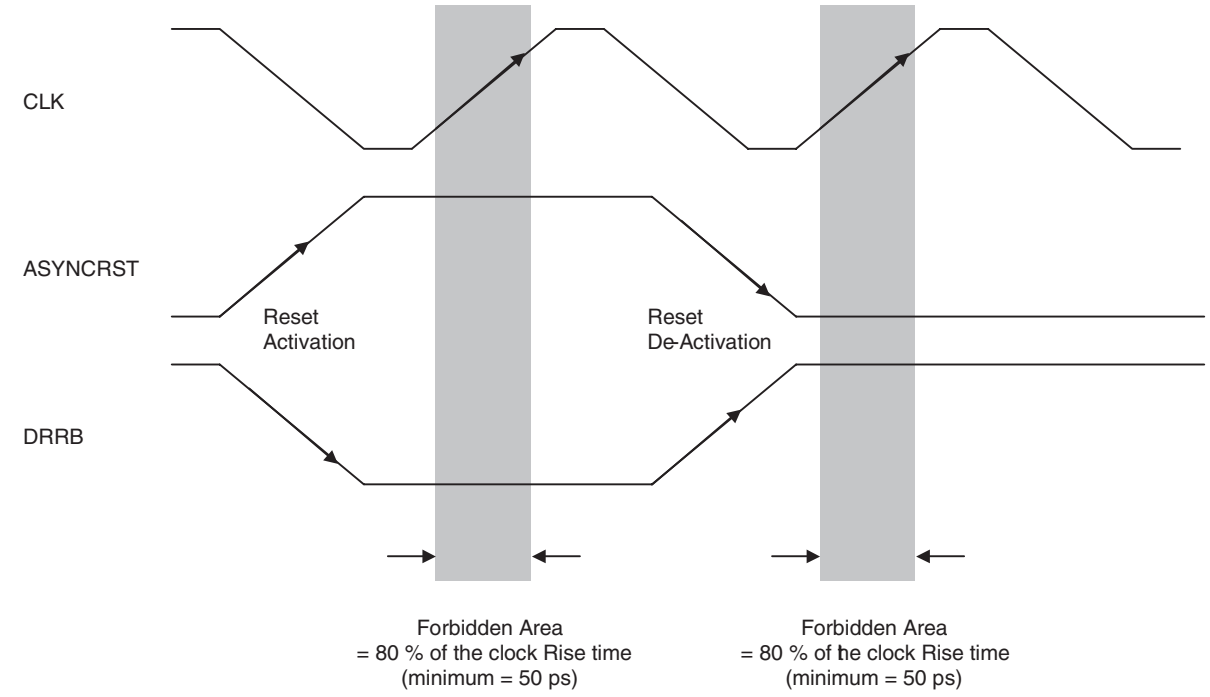


Figure 2-13. Reset Timing Requirements



The reset (activation or de-activation) is taken into account on the clock edge marked with an arrow.

Figure 2-14. Reset Forbidden Area



Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset to Data Ready (Reset activation)	TRDR1		4		ns
Reset to Data Ready (Reset De-activation)	TRDR2	0		6	ns
Forbidden Area		50	80% of the input clock Rise Time		ns
Reset Minimum Pulse Width		1			ns

The main advantage of this method is to avoid adding extra circuitry on the clock (impact of the clock jitter of the clock) but it adds some constraints in the timings between the reset signals and the clock.

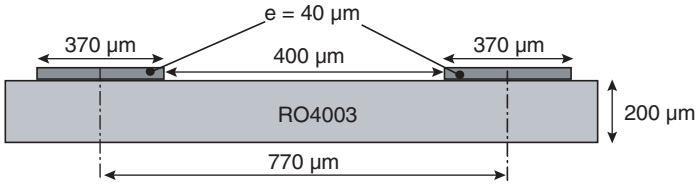
3. Hardware Implementation

3.1 Board Layout Recommendations

First, it is recommended to match all the clock signal and reset signal traces to 50Ω. As the clock signals are differential, it is necessary to match all the differential clock lines and all the reset signal lines to within 1 mm to ensure that the ADCs and DMUXes receive the clock and reset signals simultaneously (limited skew between the clock signals and between the reset signals).

Figure 3-1 on page 11 shows the recommended board layout, as used for Atmel converter evaluation boards using RO4003 dielectric material.

Figure 3-1. 50Ω Matched Line on R04003 Layout (Differential Signal)



3.2 Clock and Reset Drivers

Table 3-1. Differential Buffer/Gates Examples (for Information Only)

Manufacturer	Part Number	Description	Input Compatibility	Output Compatibility	Max Frequency	Propagation Delay
On Semiconductor	MC100LVEP14	Clock Driver	ECL/PECL/HSTL	ECL/PECL	2 GHz	400 ps
Micrel	SY898830	Clock Driver	PECL/LVPECL/ECL/HSTL	PECL	2.5 GHz	450 ps
On Semiconductor	MC10LVEP16	Differential Driver	ECL	ECL	4 GHz	240 ps
On Semiconductor	NB6L11	Differential Driver/translator	ECL	ECL	6 GHz	150 ps
Micrel	SY58012U	Differential Driver/translator	LVPECL/LVDS/CML	LVPECL	5 GHz	260 ps
Micrel	SY89311U	Differential Driver	PECL/LVPECL/ECL	ECL/PECL	3 GHz	300 ps

3.3 Practical Examples (ADC and DMUX in the Same Package)

Figure 3-2. Reset Signals Implementation

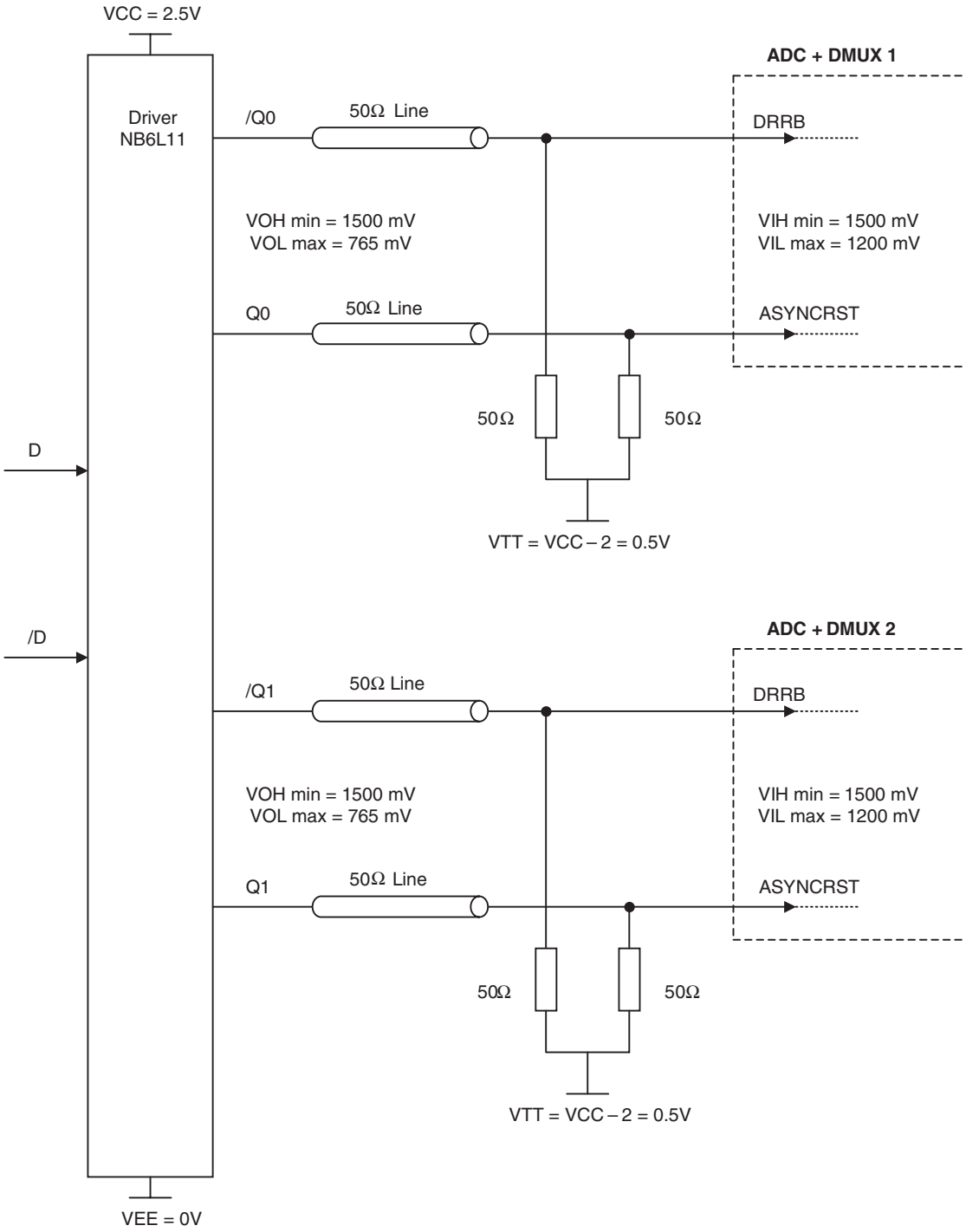
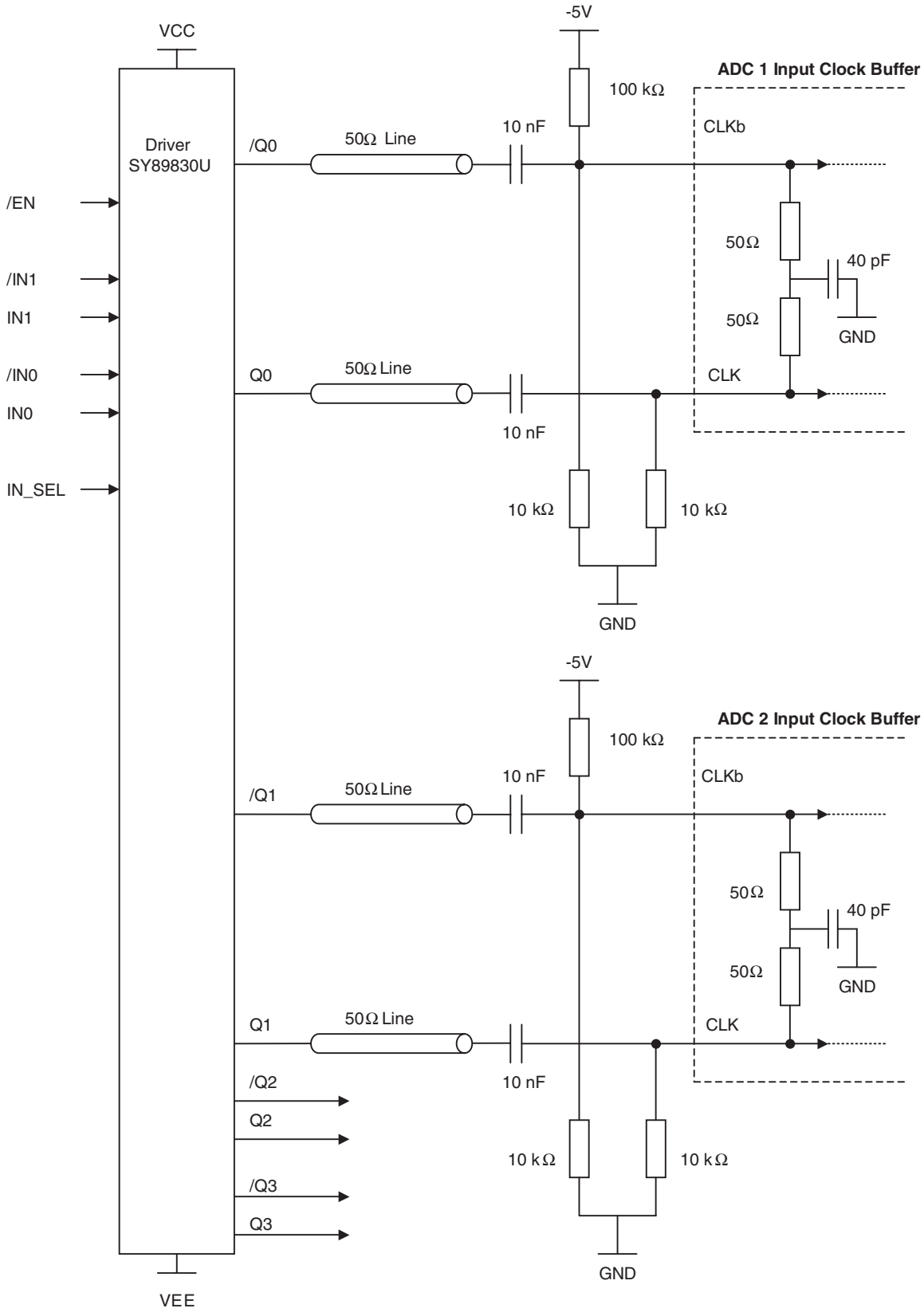


Figure 3-3. Clock Input Implementation (Example)



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