Application Note

Introduction

e2v AT84AS003/4 10-bit 1.5 Gsps or 2 Gsps ADC with 1:2/4 combined DMUX, feature two independent reset signals DRRB and ASYNCRST which must be used to start the device properly. As DRRB and ASYNCRST are not active at the same level (DRRB active low and ASYNCRST active high) they should be applied simultaneously, one possible way to implement both signals is to use the positive and negative signals of a differential pair, thus ensuring that both resets occur simultaneously.

This Application note provides some ideas to implement the reset circuit for the AT84AS003 or AT84AS004 (please refer to the last version available of the device datasheet, reference 0808 and 0829 respectively).

1. AT84AS003 DRRB and ASYNCRST

1.1 Description

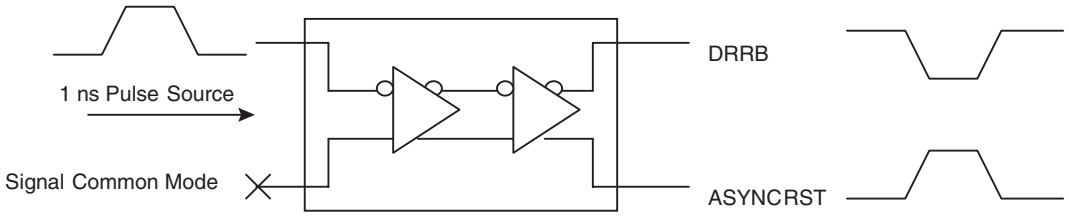
There are two reset signals available for the AT84AS003/4: DRRB and ASYNCRST. These reset signals DRRB and ASYNCRST are required to start the device properly.
It is recommended to apply both reset signals at the same time and to hold the input clock low during reset See “Timing Requirements” on page 4.

- The DRRB / ASYNCRST signal frequency should be 200 MHz maximum
- The reset pulse should be 1 ns minimum
- DRRB is active low while ASYNCRST is active high

As it is recommended to apply both reset signals simultaneously, one possible solution is to use a differential driver so that DRRB and ASYNCRST are generated as the two signals of a differential pair. This would allow for both the simultaneous application of the signals to the device and a simple way to drive both signals.

An example is provided in Figure 1-1 (principle of operation).

Figure 1-1. AT84AS003/4 DRRB and ASYNCRST Driver Scheme



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2. Electrical Characteristics

Table 2-1. DRRB and ASYNCRST Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
ADC reset	DRRB	-0.3 to V_{CCA} + 0.3	V
DMUX asynchronous reset	ASYNCRST	-0.3 to V_{CCD} + 0.3	V

Table 2-2. DRRB and ASYNCRST Recommended Conditions of Use

Parameter	Symbol	Recommended	Unit
ADC reset	DRRB	2.5V ECL, HSTL, LVCMOS levels	V
DMUX asynchronous reset	ASYNCRST	2.5V ECL, HSTL, LVCMOS levels	V

Table 2-3. DRRB and ASYNCRST Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
DRRB					
Logic low		0		1.0	V
Logic high	DRRB	1.6	V_{CCA}		V
Threshold			1.4		
ASYNCRST					
Logic low		0		1.0	V
Logic high	ASYNCRST	1.6	V_{CCD}		V
Threshold			1.4		

3. Case When the Input Clock Is Held Low During Reset

3.1 Timing Diagrams

Figure 3-1. Asynchronous Reset Timing Diagram, 1:2 Mode, Simultaneous Mode, Input Clock Held Low During Reset (Principle of Operation)

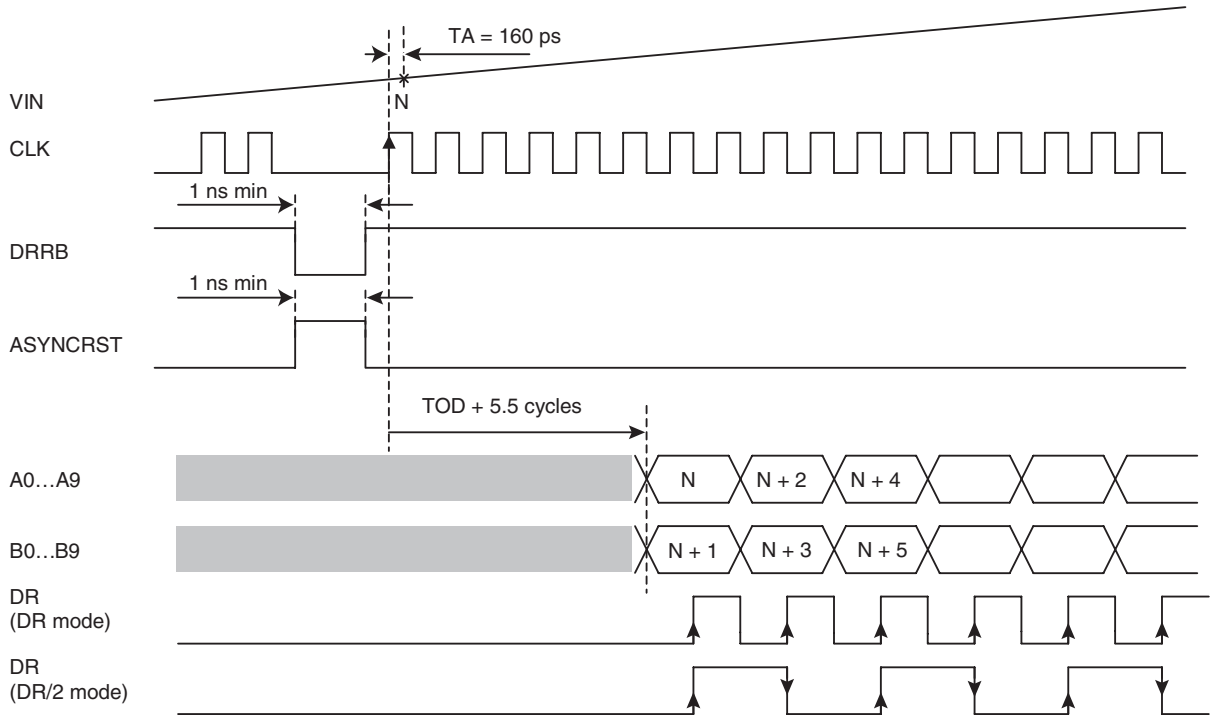
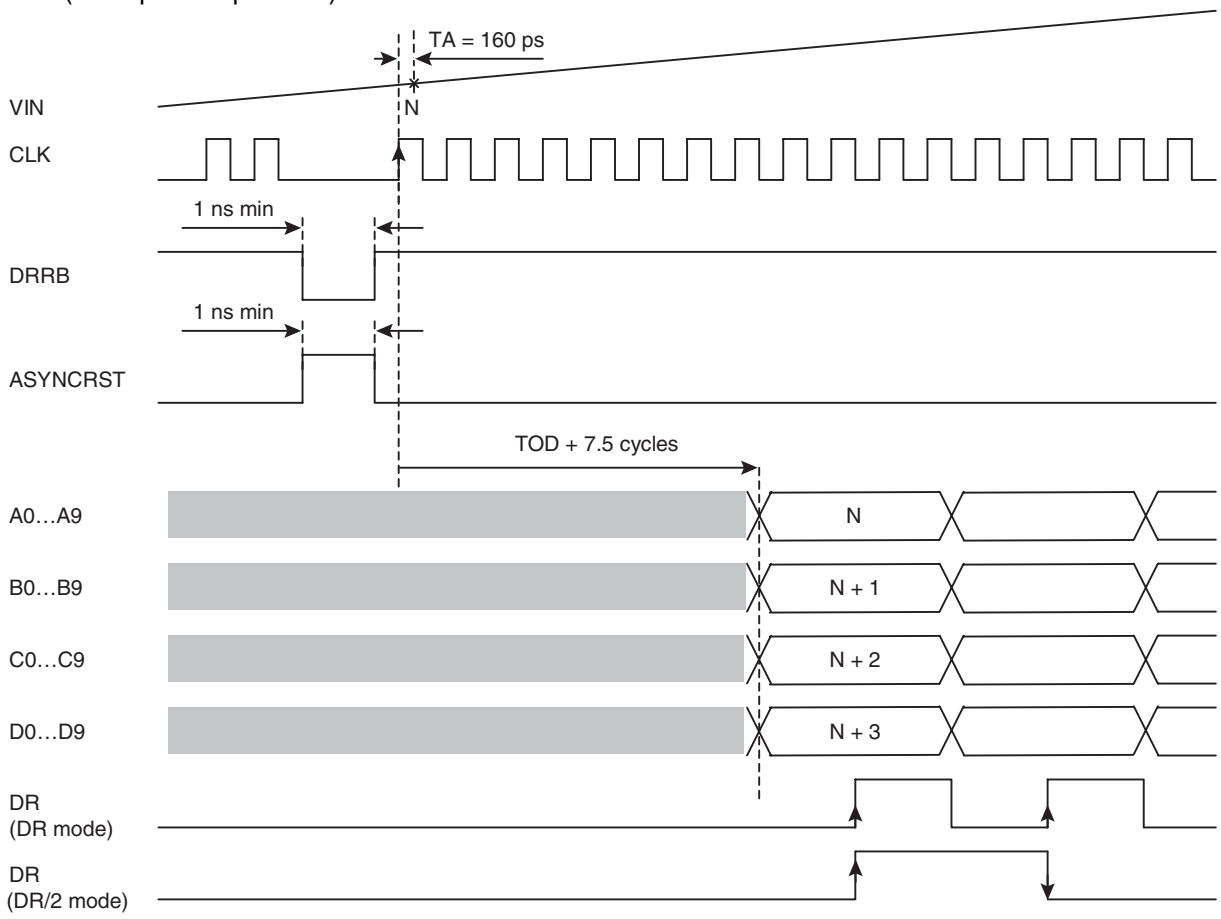


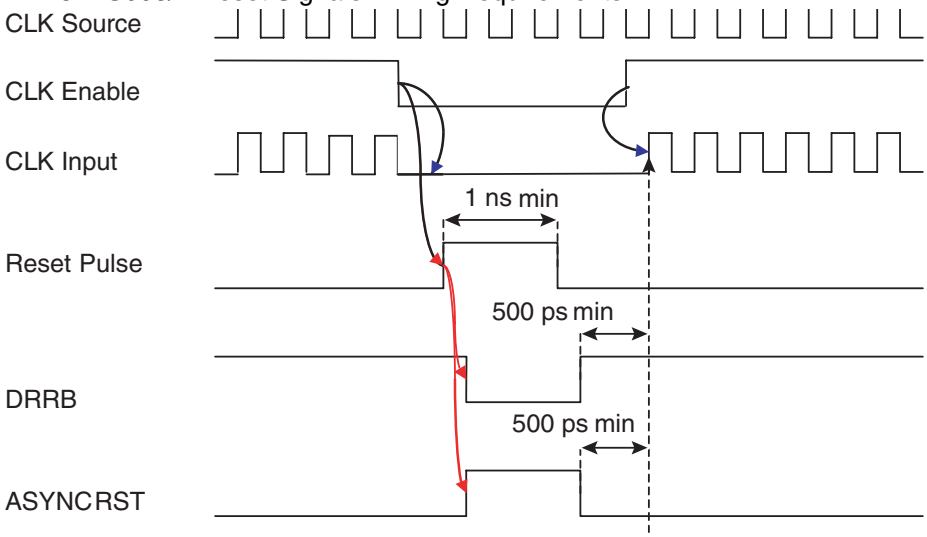
Figure 3-2. Asynchronous Reset Timing Diagram, 1:4 Mode, Simultaneous Mode, Input Clock Held Low During Reset (Principle of Operation)



3.2 Hardware Implementation

3.2.1 Timing Requirements

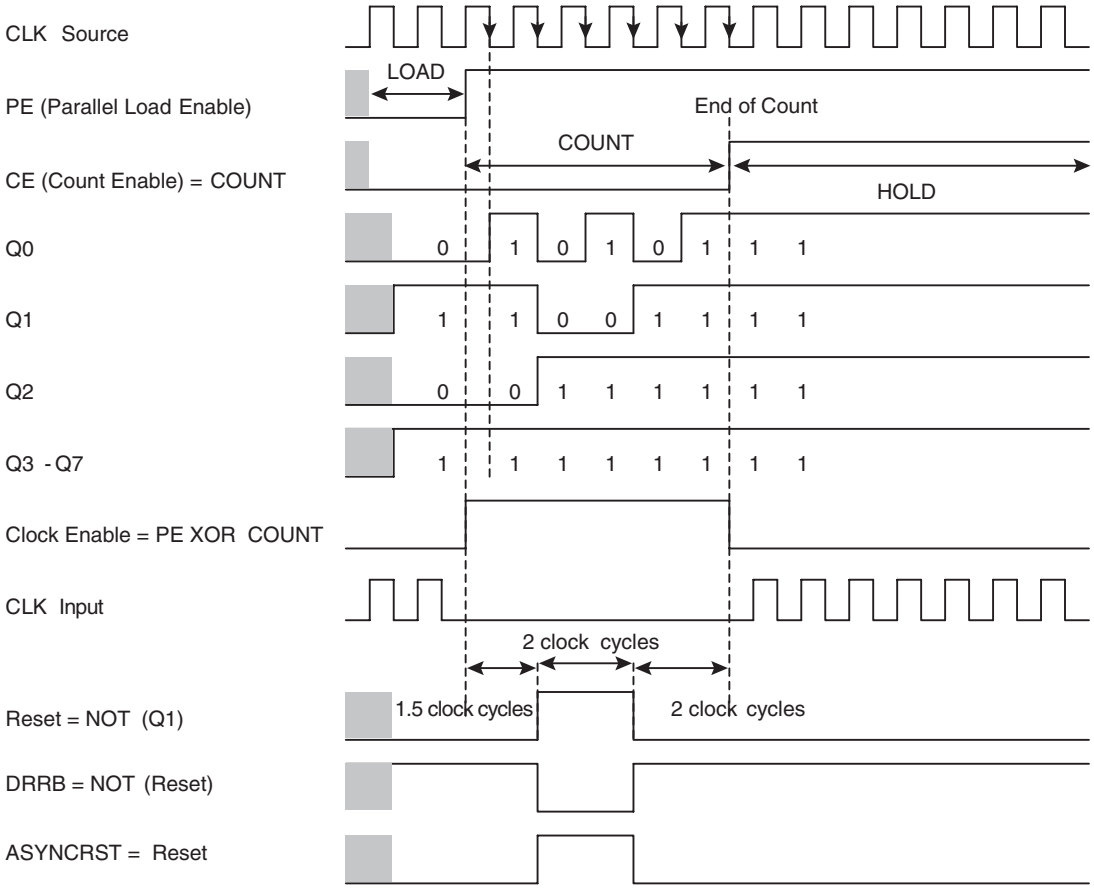
Figure 3-3. AT84AS003/4 Reset Signals Timing Requirements



3.2.2 Example of Synopsis

In the following section, Figure 3-4 on page 5 and Figure 3-5 on page 6 give one alternative solution to implement the clock and reset circuitry using discrete components.

Figure 3-4. AT84AS003/4 Reset Signals Implementation Timing Diagram using a Binary Up Counter



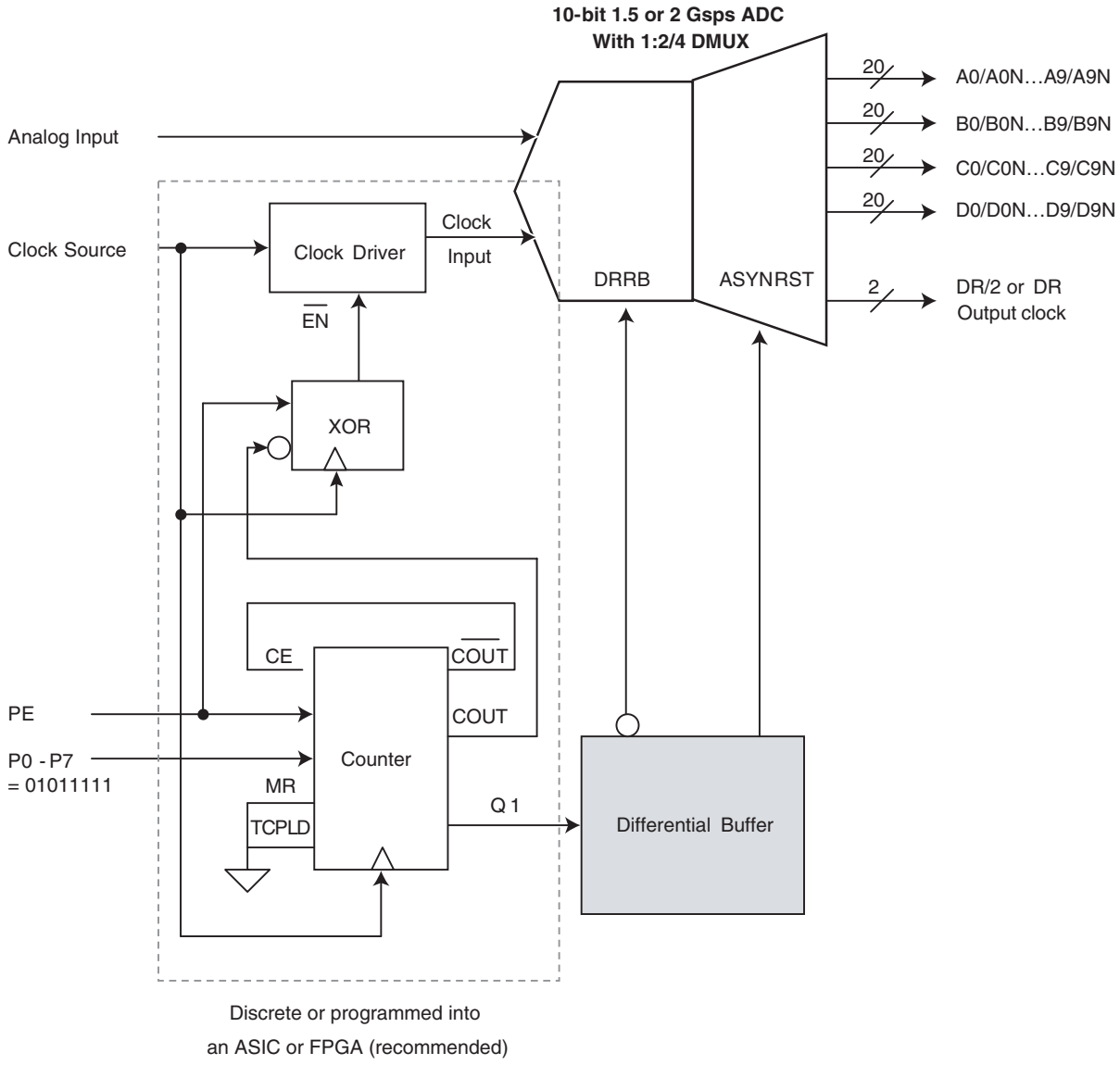
In Figure 3-4 on page 5, the theoretical timing diagram is presented as a possible way to satisfy the timing requirements described in Figure 3-3 on page 4. The idea is to ensure that the reset signals:

1. Are applied only 1.5 clock cycles after the input clock is held low (thanks to an enable signal)
2. Last at least 2 clock cycles (satisfying the requirement of 1 ns minimum since the maximum frequency of operation of the ADC is 2 Gsps, yielding a clock cycle of 500 ps)
3. And are released after 2 clock cycles (satisfying the requirement of 500 ps minimum before the clock restarts)

With the use of one counter, both the reset signals and the enable signal needed for the clock driver are generated.

The example given in Figure 3-5 on page 6 gives a possible implementation. However, the part within the dotted rectangle will not be further explained in the following section as it might be more easily implemented in an FPGA for example. This is why the stress is only led on the differential buffer to be used as the reset signals driver.

Figure 3-5. AT84AS003/4 Reset Signals Implementation Synopsis



Note: References for the XOR gate, the binary up counter and the clock driver are provided in Table 3-1 on page 7. This table is not exhaustive and is only intended to provide examples to help you with the design.

Table 3-1. Differential Buffer/Gates Examples (For Information Only)

Manufacturer	Part Number	Description	Input Compatibility	Output Compatibility	Max Frequency	Propagation Delay	VCC
On Semiconductor	MC100LVEP14	Clock Driver	ECL/PECL/HSTL	ECL/PECL	2 GHz	400 ps	3.3V
Micrel	SY898830	Clock Driver	PECL/LVPECL ECL/HSTL	PECL	2.5 GHz	450 ps	3.3V
On Semiconductor	MC10EP08	XOR Gate	ECL	ECL	3 GHz	250 ps	3.3V
Micrel	SY10EP08	XOR Gate	ECL	ECL	3 GHz	200 ps	3.3V
On Semiconductor	MC10LVEP16	Differential Driver	ECL	ECL	4 GHz	240 ps	3.3V
On Semiconductor	NB6L11	Differential Driver/translator	ECL	ECL	6 GHz	150 ps	2.5V
Micrel	SY58012U	Differential Driver/translator	LVPECL/LVDS/ CML	LVPECL	5 GHz	260 ps	2.5V
Micrel	SY89311U	Differential Driver	PECL/LVPECL/E CL	ECL/PECL	3 GHz	300 ps	3.3V
Micrel	SY8985	Differential Driver/translator	LVPECL/CML/ LVDS	LVPECL	2 GHz	380 ps	2.5V
On Semiconductor	MC100EP016A	Counter	ECL	ECL	1.4 GHz	550 ps	3.3V

4. Case When the Input Clock Is Not Held Low During Reset

4.1 Timing Diagrams

Figure 4-1. Reset Timing Diagram, 1:2 Mode, Simultaneous Mode

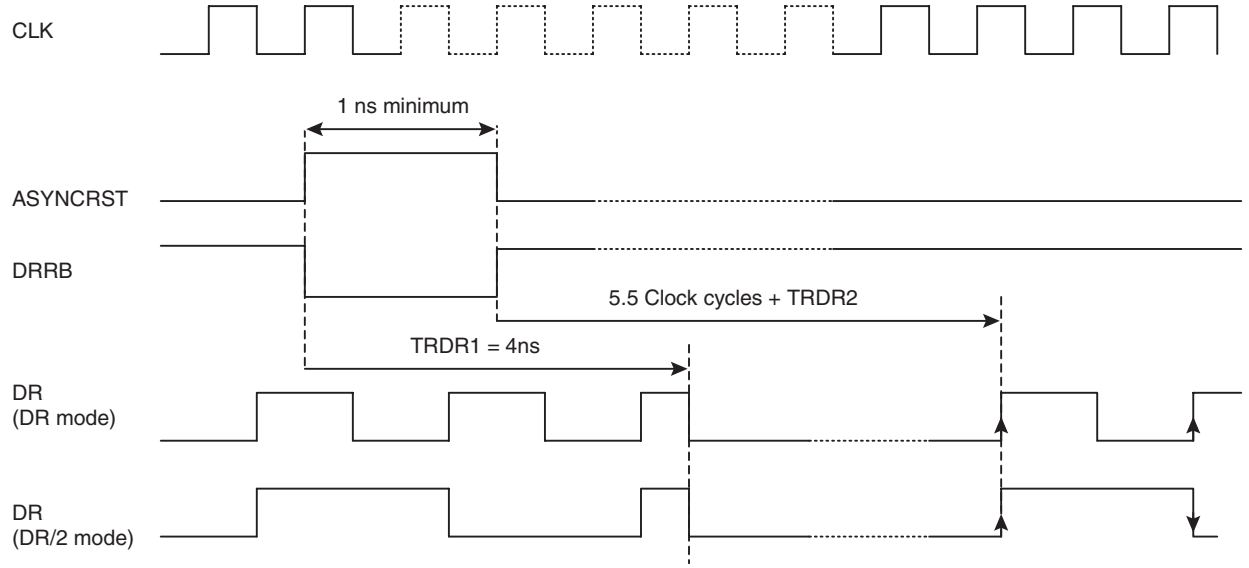


Figure 4-2. Reset Timing Diagram, 1:4 Mode, Simultaneous Mode

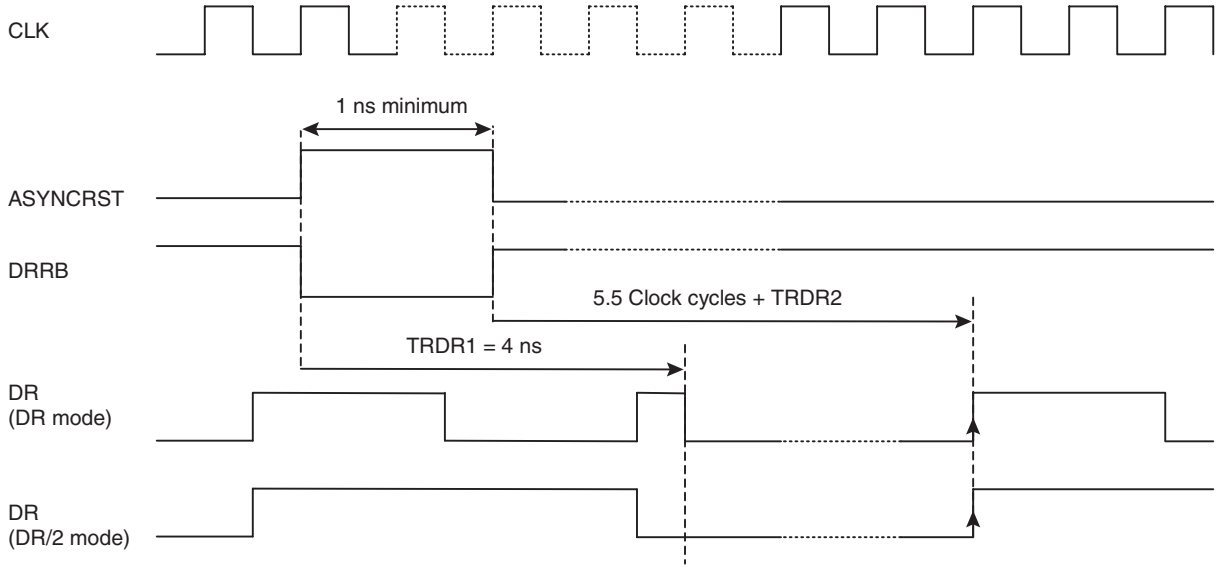
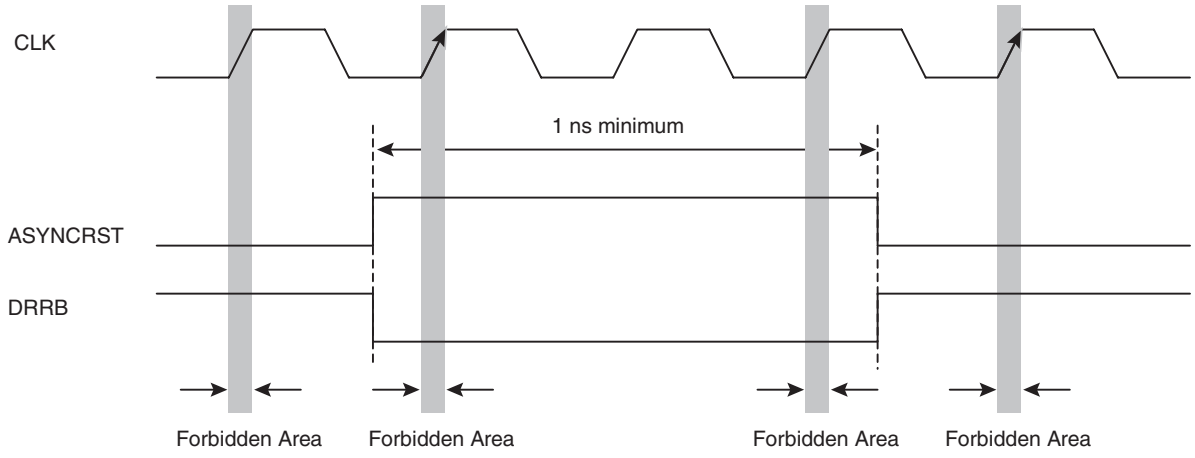


Figure 4-3. Reset Timing Requirements



The reset (activation or de-activation) is taken into account on the clock edge marked with an arrow.

Figure 4-4. Reset Forbidden Area

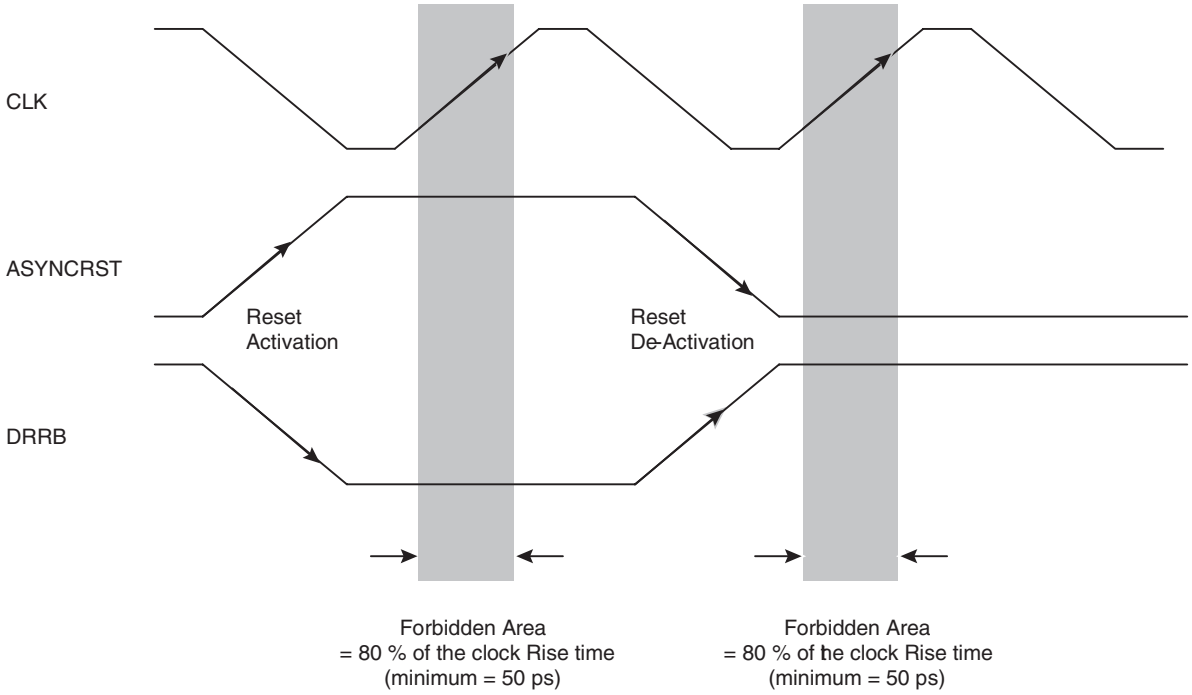


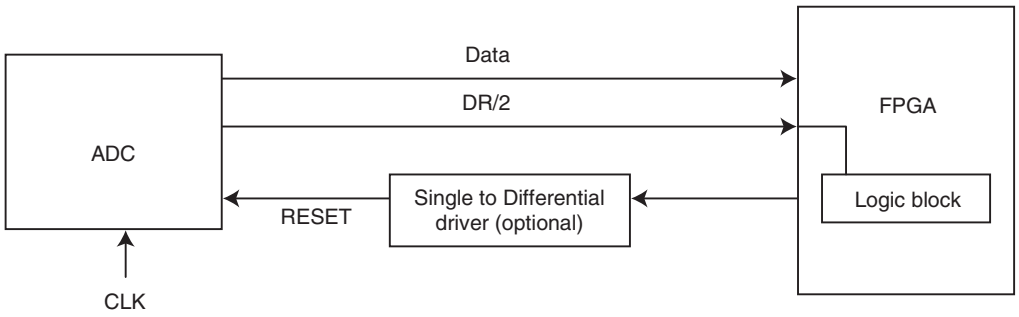
Table 4-1. Reset Timing Characteristics

Table 4-2.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset to Data Ready (Reset activation)	TRDR1		4		ns
Reset to Data Ready (Reset De-activation)	TRDR2	0		6	ns
Forbidden Area		50	80% of the input clock Rise Time		ns
Reset Minimum Pulse Width		1			ns

4.2 Example of Synopsis

Figure 4-5. Proposed Implementation Scheme



The idea is that the reset signal is generated using the output clock of the ADC which has a phase relationship with the input clock.

The reset signals can be generated inside the FPGA using the following sequence:

The Internal Reset goes high on the first rising edge of the Data ready clock and remains high until the next Data Ready rising edge, it then goes low until the next interruption (restart or external interruption) for example.

A driver can be used between the FPGA and the ADC. The same references as mentioned previously in the section dedicated to the reset when the clock is held low apply.

Figure 4-6. Reset Implementation Using the Output Clock (1:4 DMUX, DR/2 Mode) - Principle

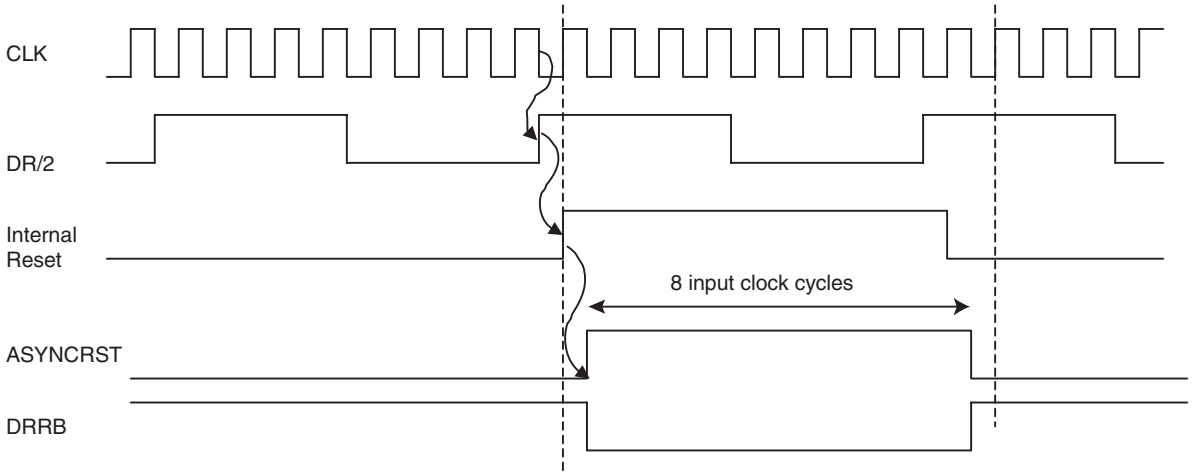
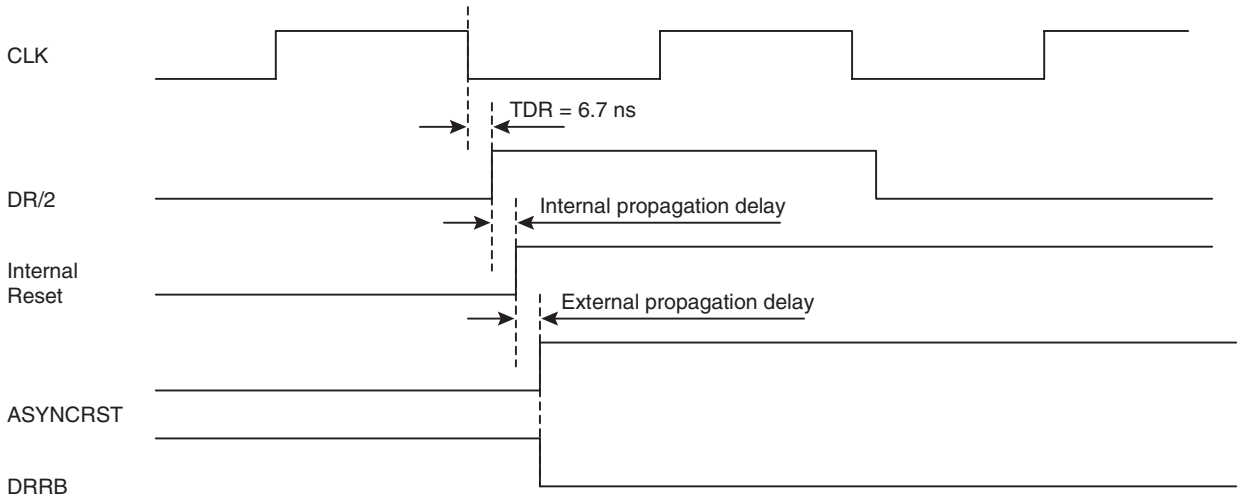


Figure 4-7. Timing Requirements



What is important is to ensure that the total delay between the input clock falling edge and the reset (ASYNCRST) rising edge is different from a multiple of half the clock period so that the reset edge will never occur during a forbidden zone as described previously:

– TDR + Internal propagation delay + External propagation delay $\neq$ N x Tclk/2

– with N integer number (N = 0, 1, 2, ...etc.).

– and TDR = 6.7 ns

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