Application Note

1. Introduction

This application note aims at providing you some recommendations to help you implement the AT84AS003 or AT84AS004 10-bit 1.5 Gsps or 2 Gsps respectively ADC with DMUX in your system. It first presents the ADC with DMUX input/output interface and then provides some recommendations with regards to the device settings and board layout to obtain the best performance of the device.

This document applies to the:

- AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX
- AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX

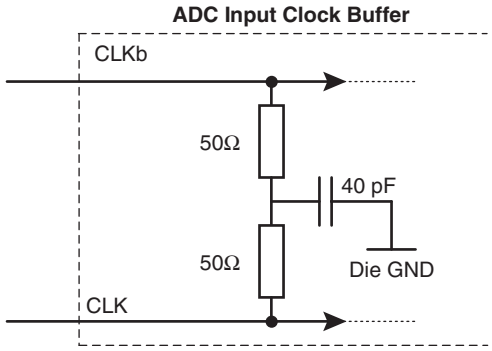
2. AT84AS003/4 ADC-DMUX Input Terminations

2.1 Clock Input

In the case of the AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX and AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX, it is recommended to drive the input clock *differentially*. The differential implementation is preferred to the single-ended fashion for the following reason:

The differential input clock buffer is on-chip terminated by two 50Ω resistors connected to the die ground plane via a 40 pF capacitor (as described in Figure 2-1. If the differential pair is used in a single-ended way (in which case, it would be necessary to terminate one signal of the pair *more likely CLKb* to ground via a 50Ω termination in order to keep the balance within the differential pair), then all the noise induced on the unused signal would affect the die ground directly and thus might degrade significantly the ADC performance. However, this is a recommendation only. Providing a proper decoupling of the ADC power supplies to ground, the difference in performance between a differential and a single-ended use might not be significant.

Figure 2-1. Clock Input Differential Buffer



The clock inputs of the ADC have a 0V common mode and can accept signals with 1V peak maximum and -1V peak minimum.

This means that if the VIH maximum of the signal you would like to drive the ADC clock with is higher than 1V peak or the VIL minimum is lower than -1V peak, then you need to *AC couple* the input signals before applying them to the ADC, this can be done by connecting 100 pF (or 10 nF) capacitors in series with the incoming signals to the ADC. If you do so, then you need also to bias the CLK and CLKb signals as follows:

- CLK or CLKb biased to ground via a 10 kΩ resistor
- CLKb or CLK respectively biased to ground via a 10 kΩ resistor and to V_{EE} via a 100 kΩ resistor

This will ensure that if no signal is applied to the differential pair, this one will not be floating but tied to a low level.

Figure 2-2. Recommended Clock Input AC Coupling Scheme

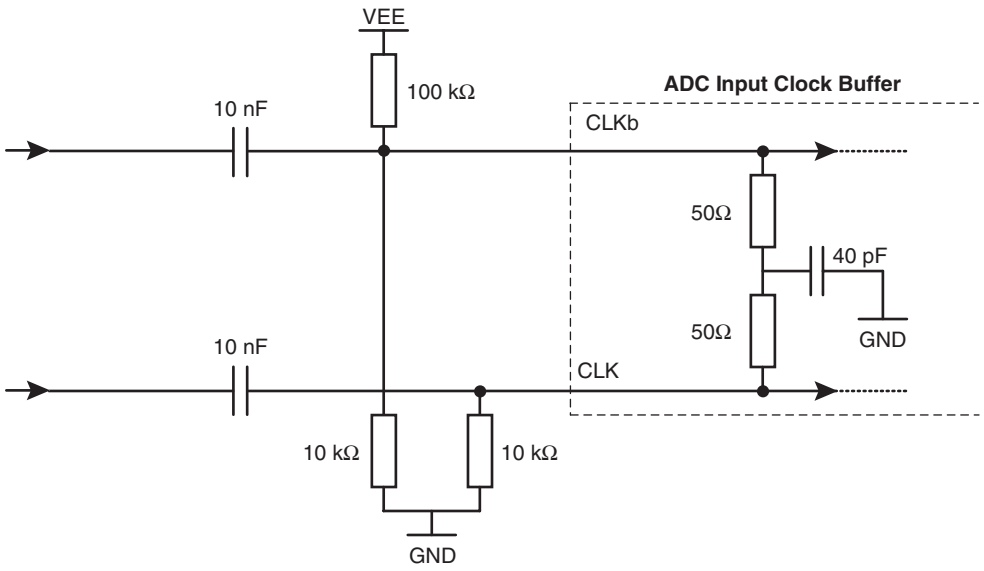


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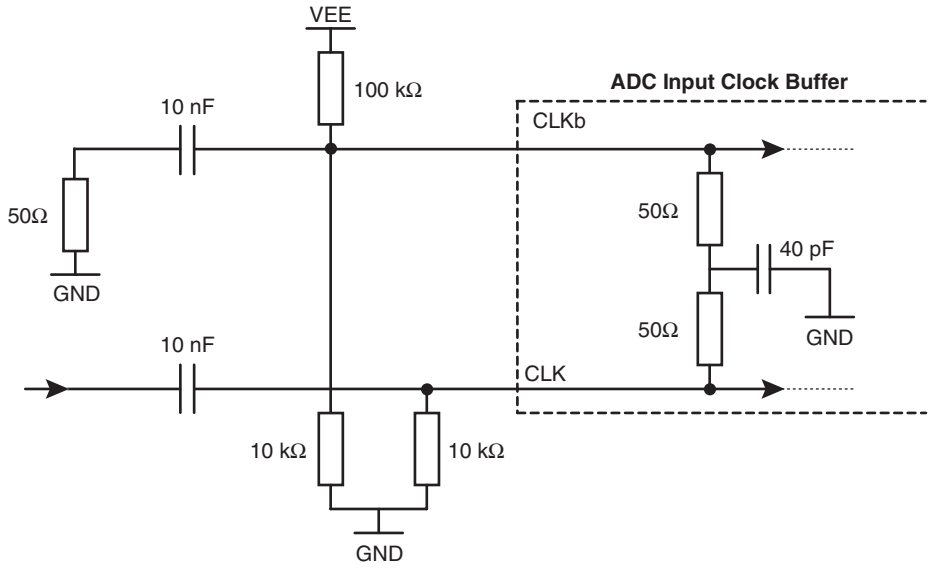
Figure 2-3. Single-ended Scheme (Allowed but not Recommended)



In the case of an application requiring a fixed clock frequency, it is recommended to filter the clock signal for improved jitter performance. The benefits of filtering the clock signal can be quantified to a 1 or 2 dB improvement in the SNR figure and thus in an increase of about 0.1 to 0.2 bit in the ENOB figure.

The filtering can be done using a narrow-band filter but because beyond the stop-band frequency the noise is not filtered out, it might be necessary to have a low-pass filter after the narrow-band filter.

Table 2-1. References for Filters (For Information Only)

Filter Type	Reference	Frequency
Band pass	4DF12-500/X2-MP (Lorch)	500 MHz
Band pass	4DF12-1000/X2-MP (Lorch)	1000 MHz
Band pass	6DF12-1400/X2-MP (Lorch)	1400 MHz
Low pass	4LP7-550X-MP (Lorch)	550 MHz
Low pass	5LP7-1000X-MP (Lorch)	1000 MHz
Low pass	6LP7-1800X-MP (Lorch)	1800 MHz

2.2 Analog Input

Although it is necessary to drive the input clock differentially with the AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX and AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX, the analog input can be indifferently driven single-ended or differential.

On the contrary to the differential input clock buffer, the analog input buffer is not on-chip terminated by two 50Ω resistors connected to the die ground plane but it is terminated externally via 50Ω reverse termination resistors as described in Figure 2-4 on page 4. The analog input can thus be driven either differentially, see Figure 2-5 on page 5 or single-ended, see Figure 2-6 on page 6.

If the differential pair is used in a single-ended way in which case, it would be necessary to terminate one signal of the pair *more likely VINb* to ground via a 50Ω termination in order to keep the balance within the differential pair as shown in Figure 2-6 on page 6, then all the noise induced on the unused signal would not affect the die ground directly.

Figure 2-4. AT84AS003 and AT84AS004 Analog Input Buffer Schematic

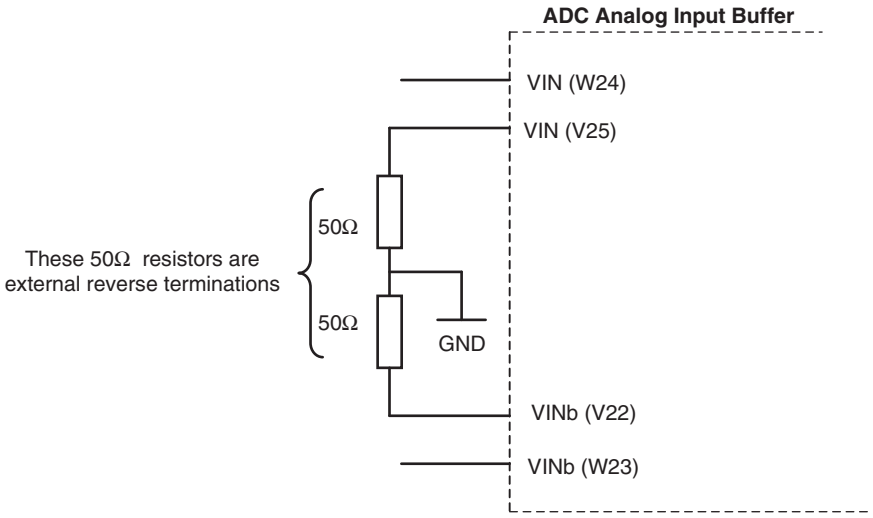


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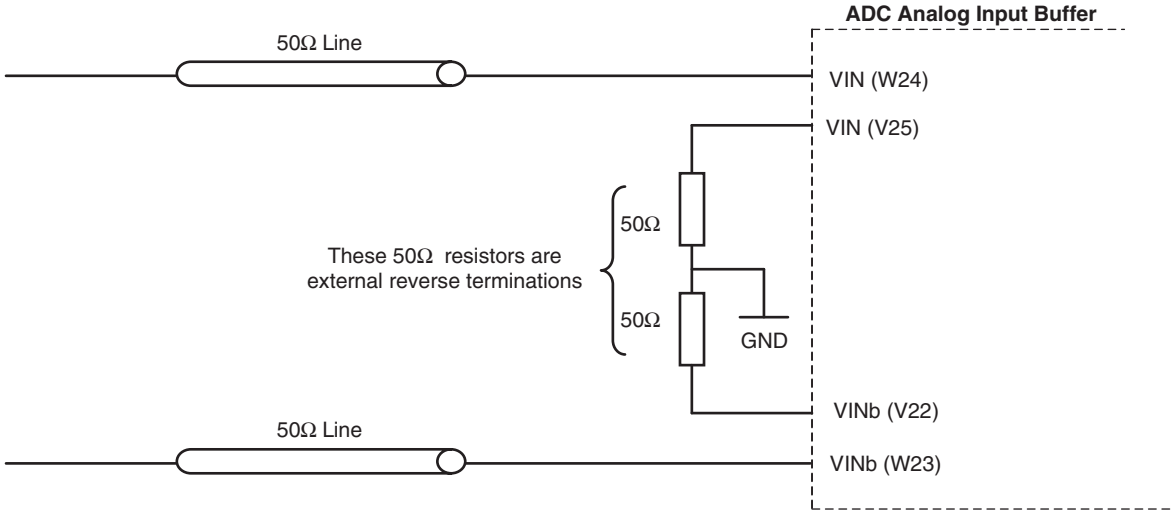
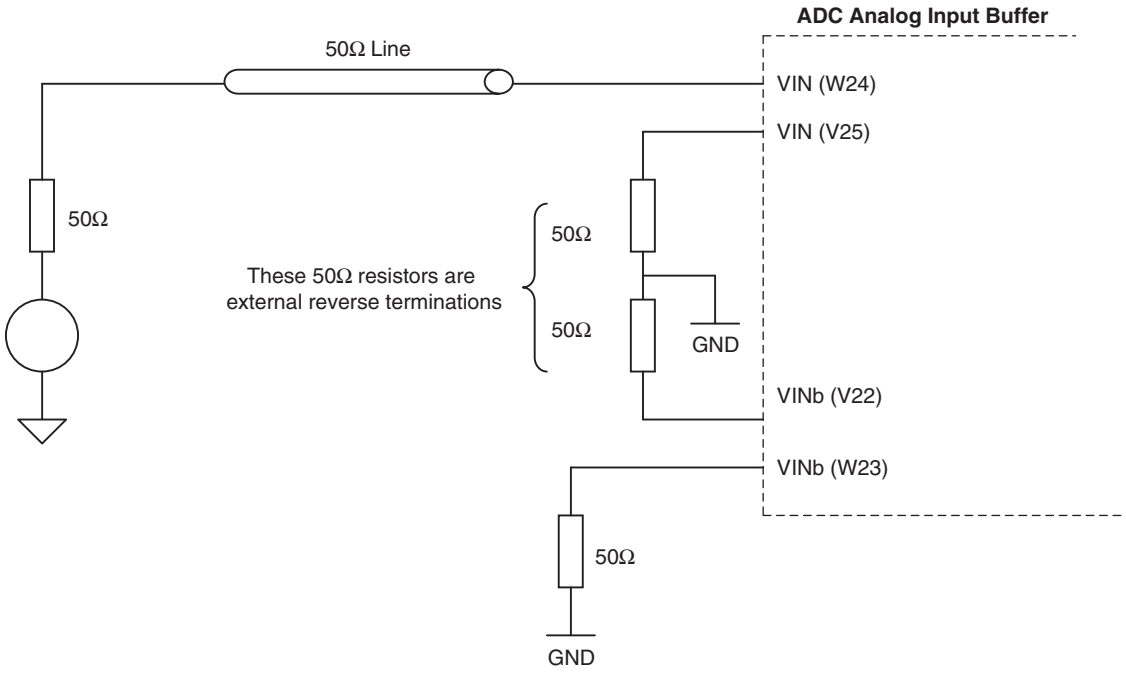
Figure 2-5. AT84AS003 and AT84AS004 Analog Input Termination Scheme (Differential)



For more information concerning the conversion from a single-ended signal to a differential signal using transformers, please refer to the “Single to Differential Conversion in High Frequency Applications” application note, reference 0944.

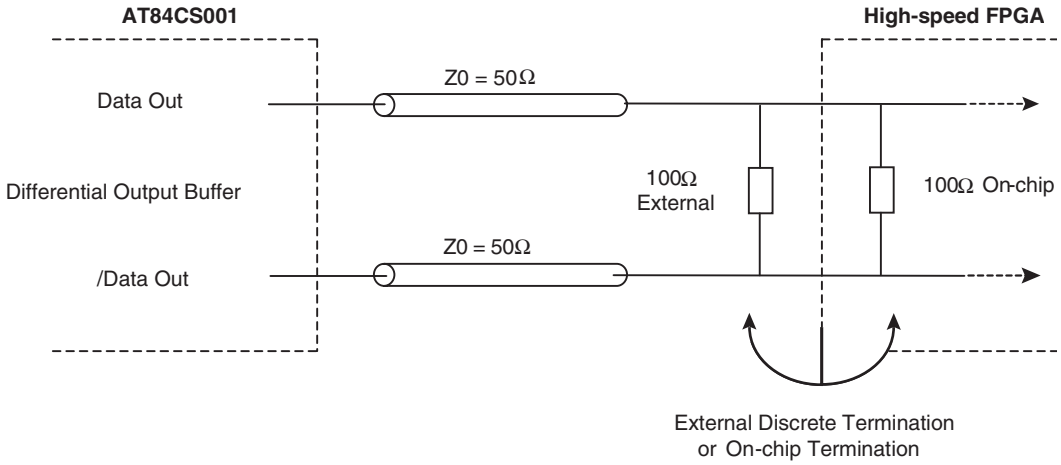
Figure 2-6. AT84AS003 and AT84AS004 Analog Input Termination Scheme (Single-ended)



3. AT84AS003/4 ADC-DMUX Output Terminations

The output data and clock of the AT84AS003 or AT84AS004 ADC with DMUX devices are LVDS and need to be 100Ω terminated (either by discrete 100Ω resistors or inside the FPGA if this feature is available in the FPGA).

Figure 3-1. AT84AS003 and AT84AS004 Output Data and Clock Interface to a High-speed FPGA in LVDS



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4. AT84AS003/4 ADC-DMUX Settings

4.1 ASYNCRST and DRRB Reset signals

There are two reset signals available for the AT84AS003 and the AT84AS004 devices: DRRB and ASYNCRST. These reset signals DRRB and ASYNCRST are required to start the device properly.

- The DRRB/ASYNCRST signal frequency should be 200 MHz maximum
- The reset pulse should be 1 ns minimum
- DRRB is active low while ASYNCRST is active high

As it is recommended to apply both reset signals simultaneously, one possible solution is to use a differential driver so that DRRB and ASYNCRST are generated as the two signals of a differential pair. This would allow for both the simultaneous application of the signals to the device and a simple way to drive both signals.

Please refer to the application note “AT84AS003/4 ADC Reset implementation”, reference 0903.

4.2 CLKTYPE

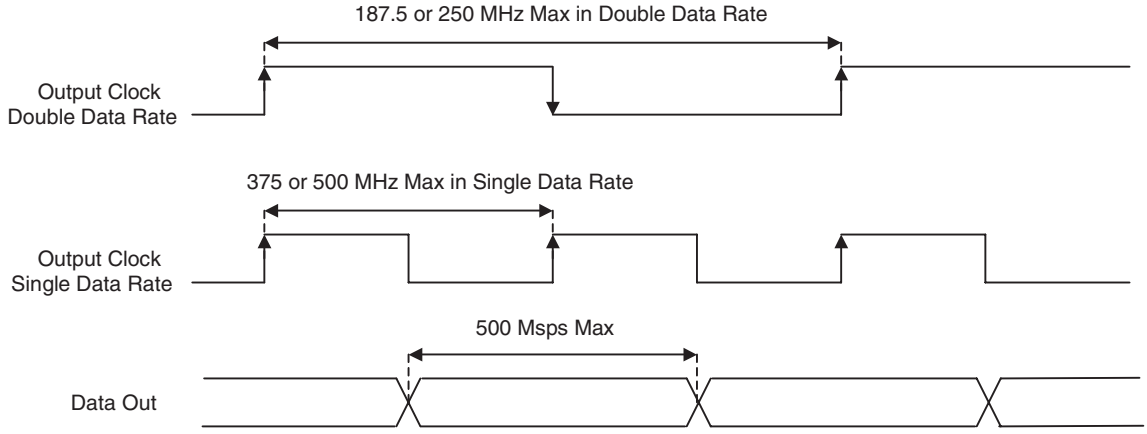
This signal has to be connected to V_{CCD} or left floating or connected to ground via a 10 kΩ resistor.

4.3 DRTYPE

The AT84AS003/4 works either in single data rate (DR mode, DRTYPE connected to V_{CCD} or left floating or connected to ground via a 10 kΩ resistor) or in double data rate (DR/2 mode, DRTYPE connected to ground via 10Ω).

The maximum output data rate is 500 Msps in both 1:2 and 1:4 DMUX ratio in the case of the AT84AS004 (375 Msps in the case of the AT84AS003): 500 MHz (375 MHz with the AT84AS003) output clock in single data rate and 250 MHz output clock (187.5 MHz with the AT84AS003) in double data rate, which makes it compliant with standard high-speed FPGAs.

Figure 4-1. AT84AS003 and AT84AS004 Single or Double Data Rate Timings



4.4 CLKDACTRL

A delay cell is implemented on the DMUX input clock path to allow you to adjust the timings between the data and the clock at the DMUX input. Given a sampling frequency, there are allowed and forbidden values for CLKDACTRL for which the ADC with DMUX device will work properly. The mapping between the clock frequency and the CLKDACTRL value is given in Table 4-1 on page 9. This table shows explicitly the values of CLKDACTRL which ensure a proper operation of the device with respect to a given sampling frequency.

For example, if you intend to use the AT84AS003 device at 1.5 Gsps fixed clock frequency, CLKDACTRL can be set to 1.15V to 2V for proper operation. If you intend to use the AT84AS004 device at 2 Gsps, then CLKDACTRL should be set to 1V to 1.35V or 1.65V to 2V.

Finally, if your application require to sweep the sampling frequency, you might have to use two or more values of CLKDACTRL for given frequency sub-ranges. For example, if you intend to use the ADC with a sampling clock frequency ranging from 200 MHz to 1.5 GHz, then you can set CLKDACTRL to 2V for the operation from 200 MHz to 1 GHz and then to 1.5V for operation from 1 GHz to 1.5 GHz. If you set CLKDACTRL to 1.3V for example and sweep the clock frequency from 200 MHz to 1.5 GHz, you will see a significant degradation of the performance of the ADC between 550 MHz and 750 MHz (not included).

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Table 4-1. CLKDACTRL Operating Range versus the Sampling Clock Frequency (Ambient Temperature and Typical Power Supplies)

	CLKDACTRL (V)	1	1,05	1,1	1,15	1,2	1,25	1,3	1,35	1,4	1,45	1,5	1,55	1,6	1,65	1,7	1,75	1,8	1,85	1,9	1,95	2
Fclock	200 MHz																					
	250 MHz																					
	300 MHz																					
	350 MHz																					
	400 MHz																					
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	1950 MHz																					
	2000 MHz																					
	2050 MHz																					
	2100 MHz																					

Not OK

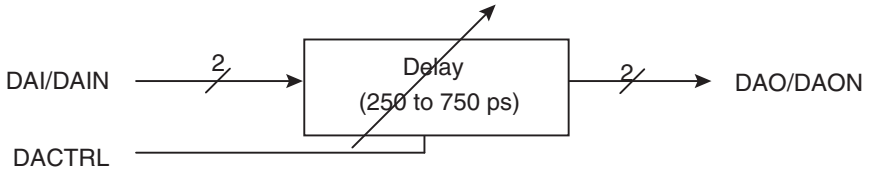
OK

4.5 DACTRL

The AT84AS003 and AT84AS004 feature a standalone delay cell which is only an additional function in case a delay cell might be required in the application (for clock monitoring for example). It is not necessary to use this function in most of the applications. However, if this function is of help, it is very easy to implement:

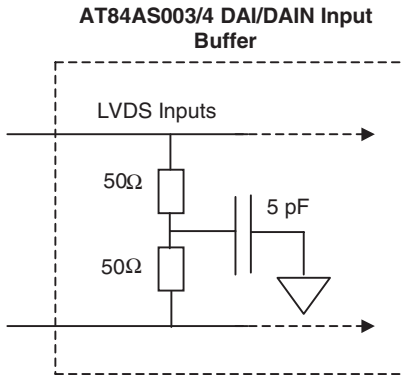
- DAI/DAIN is the differential input (LVDS)
- DACTRL is used to control the delay (from 250 ps to 750 ps for DACTRL varying from V_{CCD} / 3 to (2 x V_{CCD})/3
- DAO/DAON is the differential delayed output signal (LVDS)

Figure 4-2. Standalone Delay Cell Block Diagram



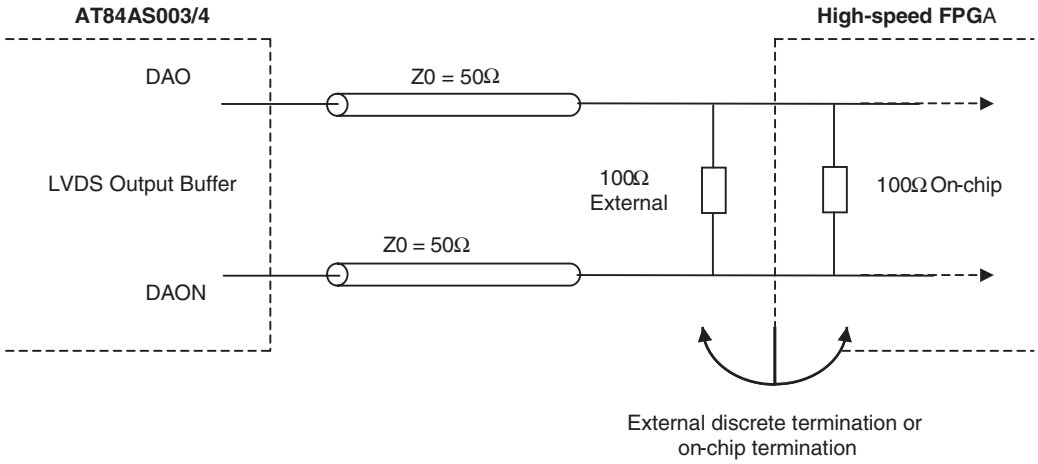
The input buffer for DAI/DAIN is described in Figure 4-3 on page 10. As it is on-chip already +2 x 50Ω terminated the 100Ω LVDS external termination is not required.

Figure 4-3. DAI/DAIN Input Buffer



The output buffer for DAO/DAON is the same as for the output data and clock. As it is LVDS, a 100Ω LVDS external termination is required as described in Figure 4-4 on page 10.

Figure 4-4. DAO/DAON Output Buffer Termination



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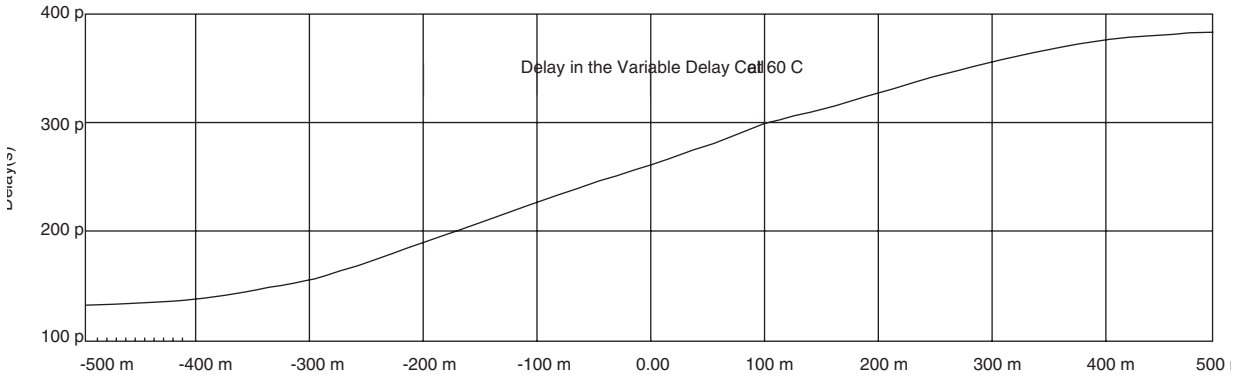
4.6 SDA

The Sampling delay adjust function (SDA pin) allows to fine-tune the sampling ADC aperture delay TAD around its nominal value (160 ps). This functionality is enabled thanks to the SDAEN signal, which is active when tied to V_{EE} and inactive when tied to GND. If SDAEN is connected to ground (SDA function not active), then the ADC aperture delay is the nominal one as specified in the datasheet. This feature is particularly interesting for interleaving ADCs to increase sampling rate. The variation of the delay around its nominal value as a function of the SDA voltage is shown in Figure 4-5 on page 11.

The typical tuning range is ±120 ps for applied control voltage varying between -0.5V to 0.5V on SDA pin.

Figure 4-5. ADC Aperture Delay versus SDA



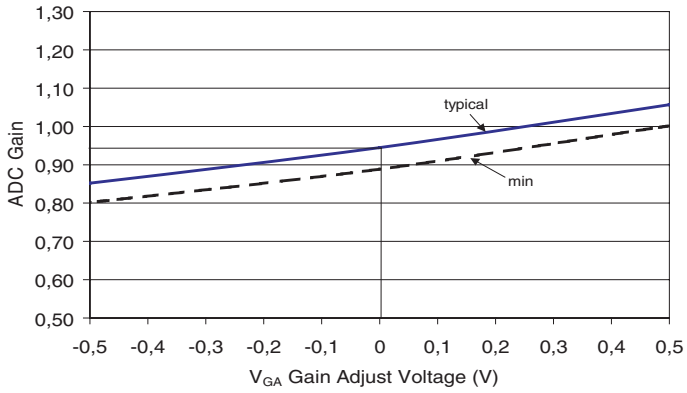
Note: The variation of the delay in function of the temperature is negligible.

4.7 GA

The ADC gain is adjustable by the means of the pin W21 of the EBGA package.

If the GA pin is left floating, then the gain of the ADC will be the nominal gain as specified in the datasheet. The gain adjust transfer function is given in Figure 4-6 on page 12.

Figure 4-6. ADC Gain versus GA Voltage



4.8 SLEEP, STAGG, RS, BIST, B/GB and PGEB

Table 4-2. AT84AS003/4 Mode Settings

Function	Logic Level	Electrical Level	Description
SLEEP	0	10Ω to ground	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10Ω to ground	Normal conversion
		N/C	
STAGG	0	10Ω to ground	Staggered mode
	1	10 KΩ to ground	Simultaneous mode
		N/C	
RS	0	10Ω to ground	1:2 ratio
	1	10 kΩ to ground	1:4 ratio
		N/C	
BIST	0	10Ω to ground	BIST
	1	10 kΩ to ground	Normal conversion
		N/C	
B/GB	0	Floating or Ground	Binary coding
	1	VEE	Gray coding
PGEB	0	Floating or Ground	Normal operation
	1	VEE	Pattern Generator function on the ADC block

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5. Grounding and Power Supplies

5.1 Common Ground Plane

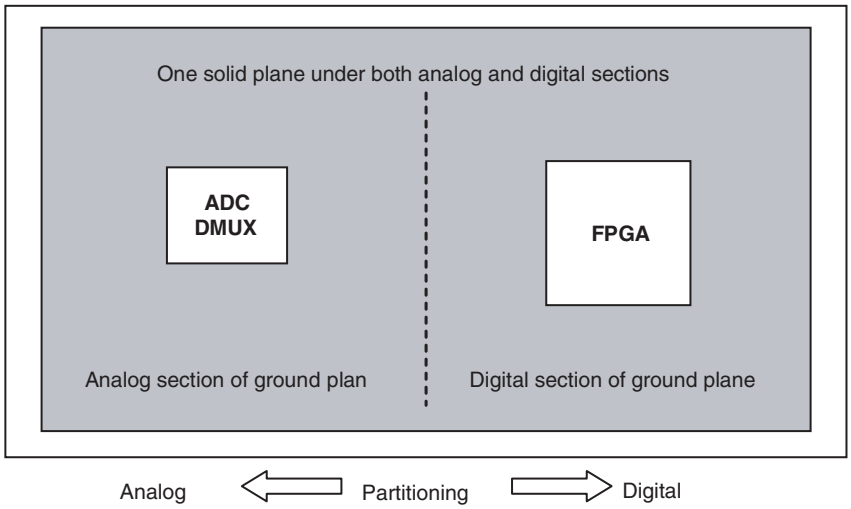
It is recommended to use the same common ground plane for the ADC-DMUX and the digital ground plane used for the digital part of the system (FPGA for example).

- Do not split the ground plane, use one solid plane under both analog and digital sections of the board (see Figure 5-1).

Partition your PCB with separate analog and digital sections. Locate all analog components and lines over the analog power plane and all digital components and lines over the digital power plane.

Note: We recommend a minimum distance of 2 cm between the ADC-DMUX and FPGA

Figure 5-1. Schematic View of the System Board Ground Plane (Example)



5.2 Power Supply Planes

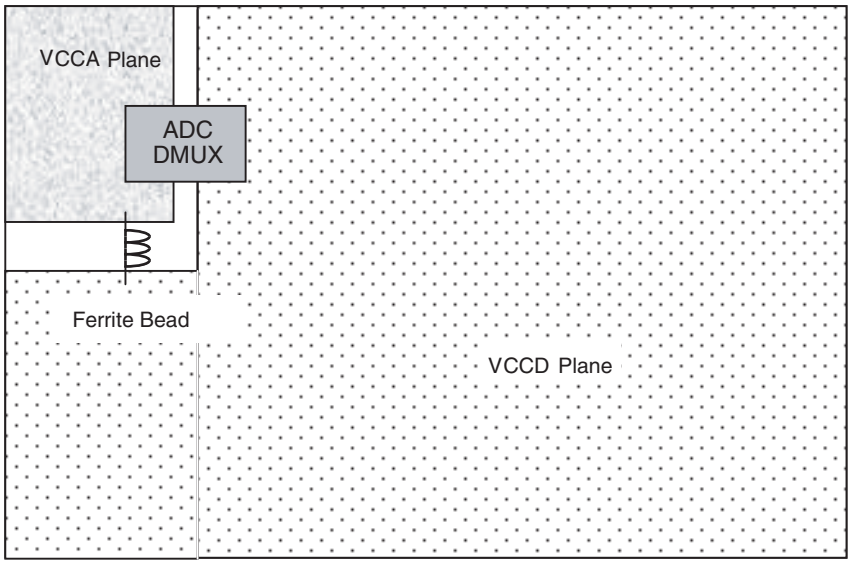
The ADC-DMUX requires four power supplies:

- V_{EE} = -5V analog (same plane used for V_{EE} and SUB)
- V_{MINUSD} = -2.2V digital
- V_{CCA} = 3.3V and V_{CCD} = 3.3V
- V_{PLUSD} = 2.5V

Five different planes are required for the ADC and the DMUX.

It is recommended to use the same layer for both V_{CCA} and V_{CCD} power supplies but using separate planes which can be reunited by a ferrite bead as shown in Figure 5-2 on page 14. As the V_{CCA} plane concerns only the analog part of the AT84AS003/4 device, the less extended it is the better.

Figure 5-2. Schematic View of V_{CCA} and V_{CCD} 3.3V Planes



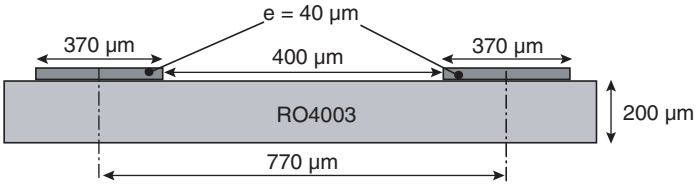
For more information concerning the power supplies decoupling and bypassing, please refer to the device datasheet (reference 0808 and 0829 for the AT84AS003 and AT84AS004 devices respectively).

5.3 Board Layout Recommendations

It is necessary to ensure that all the lines at the input of the ADC and at the output of the DMUX are matched to within 2 mm. As all data lines are differential, it is also necessary that each line of a differential pair is matched in length within 1 mm.

Figure 5-3 on page 14 gives the layout rule used on RO4003 for differential signals.

Figure 5-3. 50Ω Matched Line on RO4003 Layout (Differential Signal)



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How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax: +49 (0) 8142 284547

mailto: enquiries-de@e2v.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline-bdc@e2v.com