Migrating from TS8388B ADC to AT84AD001B ADC

Application Note

1. Introduction

This application note aims at providing you some recommendations to migrate from a design using the TS8388B ADC to the AT84AD001B ADC.

The initial assumptions are the following:

- one AT84AD001B should replace the TS8388B (meaning that one on the two channels of the AT84AD001B will remain unused);
- The 3WSI of the AT84AD001B will remain un-activated;
- this document will not address the board layout issues but will highlight the differences between the two ADCs to ease the migration from the TS8388B to the AT84AD001B.

This document applies to the:

- AT84AD001B Dual 8-bit 1 Gsps ADC
- TS8388BC 8-bit 1 Gsps ADC

BDC-02/07

2. TS8388B vs AT84AD001B

2.1. Electrical characteristics

Table 1. TS8388B vc AT84AD001B electrical characteristics

Parameter	TS8388B	AT84AD001B	Comments
Power supplies			
Analog core	VEE = -5V	VCCA = 3.3V	The main problem here would be to switch from a negative supply to a positive supply
Digital part	VCC = 5V	VCCD = 3.3 V	
Output buffers	VPLUSD = 2.4V (LVDS)	VCCO = 2.25 V	VCCO if the AT84AD001B can support 2.5V (with an increase in the power consumption).
Power dissipation			
Nominal mode	3.6W	1.4W	With the 3WSI of the ADC not activated
Analog inputs	500 mVpp Full Scale	500 mVpp Full Scale	
Clock input	ECL or specified clock input power level in dBm (4 dBm typ.)	PECL, ECL, LVDS providing AC coupling 0 dBm typ.	For the AT84AD001B, also applicable to the DDRB, DDRBN reset.
Digital output data	ECL (VPLUSD = 0V) or LVDS (VPLUSD = 2.4V)	LVDS	

2.2. Timing Parameters

Table 2. TS8388B vc AT84AD001B timing parameters

Parameter	TS8388B	AT84AD001B	Comments
Aperture delay	250 ps (typ.)	1 ns (typ.)	
Output rise/fall time for data	350 ps (typ.)	350 ps (typ.)	
Output rise/fall time for output clock	350 ps (typ.)	350 ps (typ.)	
Pipeline delay	4 cycles	3.5 cycles (DMUX 1:1)	
Data Output to clock delay	1.3 ns (typ.)	3.8 ns (typ.)	
Output clock to clock delay	1.3 ns (typ.) – defined from input clock falling edge	3 ns (typ.) – defined from input clock falling edge	The output clock is well centered on the data for the TS8388B, this may not be the case with the AT84AD001B
Reset to output Clock delay	0.72 ns (typ.)	2 ns (typ.)	

2.3. I/Os

Table 3. TS8388B vc AT84AD001B I/Os

Parameter	TS8388B	AT84AD001B	Comments
Sampling Clock input	Double pads which needs to be reverse terminated to ground via 50Ω resistors (CQFP package)	Double pads which needs to be reverse terminated to ground via 50Ω resistors	The unused channel (Q) can just be left open (CLKQ, CLKQB left open).
Analog input	500 mVpp Full Scale Double pads which needs to be reverse terminated to ground via 50Ω resistors (CQFP package)	500 mVpp Full Scale Double pads which needs to be reverse terminated to ground via 50Ω resistors	The analog input of the unused channel (Q) should be terminated by 50Ω on one signal of the VINQ, VINQB pairs with the other two signals left open. Ie. Pin 48 left open and pin 47 terminated, pin 49 left open and pin 50 terminated.
Digital output data	ECL or LVDS (2 x 75Ω termination)	LVDS (2 x 50Ω termination)	
Digital output clock	ECL or LVDS (2 x 75Ω termination) Differential signal Double data rate	LVDS (2 x 50Ω termination) Differential signal Double data rate	
Reset signal	DRRB (same pin used for DIODE) Active low	DDRB, DDRBN Differential signal Active high	These reset signals are not mandatory if only one ADC is used in the application (no need for synchronization between channels) and when there is no strict requirement on which data will be the first one to be output.
Out of range bits	OR, ORB bits	DOIRI, DOIRIN bits	
Control signals (wrt TS8388B):			
Binary or Gray	GORB pin - binary if VCC - gray if ground	No specific pin (3WSI) but binary by default.	
Gain adjust	GAIN pin	No gain output pin	Equivalence between the two designs if the gain pin in the TS8388B is connected to ground or unused.
Diode	DIODE pin: - needs 2 x 3 external protection diodes (head to tail) - same pin used for DRRB reset!	DIODE pin: needs 2 x 3 external protection diodes (head to tail)	The DIODE characteristics are different between TS8388B and AT84AD001B
Control signals (wrt to AT84AD001B)			
Mode	N/A	Used to activate the 3WSI	Connect to ground to keep the 3WSI

Parameter	TS8388B	AT84AD001B	Comments
			unactivated
CLK	N/A	3WSI clock	Leave open
data	N/A	3WSI data	Leave open
LDN	N/A	3WSI load enable	Leave open
CAL	N/A	3WSI calibration output bit status	Leave open
VtestI, VtestQ	N/A	Pins for internal tests	Leave open

Note: the default settings on the AT84AD001B (when the 3WSI is not activated = connected to ground) are provided below.

- Channel I to I (clock and analog input signal)
- Channel Q to Q (clock and analog input signal)
- 0 dB gain
- 1:1 DMUX mode
- All internal adjustments to 0 value
- Binary output
- Output clock in double data rate

2.4. Other characteristics

Table 4. TS8388B vc AT84AD001B other characteristics

Parameter	TS8388B	AT84AD001B	Comments
Package	CBGA68 (1.27 mm pitch, 15 x 15 mm body) CQFP68 (1,27 mm pitch, 24 x 24 mm body) CQFP68 with Heatspreader (1,27 mm pitch, 24 x 24 mm body)	LQFP 144 (0.5 mm pitch, 20 x 20 mm body) LQFP-ep 144L green (0.5 mm pitch, 20 x 20 mm body)	Not the same footprint on the board and not the same pinout!
Finishes	Lead	Lead (LQFP144) or Green (LQFP-ep 144L)	The AT84AD001B offers green finishes.
Thermal characteristics (thermal resistance from junction to case)	6.7°C/W (CBGA) 4.75°C/W (CQFP68) 1.56°C/W (CQFP68 with Heatspreader)	6.4°C/W (bottom of case) 8.3°C/W (top of case)	Ceramic packages offser better thermal performances (but the AT84AD001B has a lower dissipation)
Moisture sensitivity level	MSL3 (CBGA package) Hermetic (CQFP package)	MSL3	Only the TS8388B offers hermetic packages